

## SVD75N08T-VB Datasheet

### N-Channel 80 V (D-S) MOSFET

#### PRODUCT SUMMARY

$V_{DS}$	80	V
$R_{DS(on)}$ $V_{GS} = 10\text{ V}$	7	$m\Omega$
$R_{DS(on)}$ $V_{GS} = 4.5\text{ V}$	9	$m\Omega$
$I_D$	100	A
Configuration	Single	

#### FEATURES

- Trench Power MOSFET
- 100 %  $R_g$  and UIS Tested

#### APPLICATIONS

- Primary Side Switching
- Synchronous Rectification
- DC/AC Inverters
- LED Backlighting



**RoHS**  
COMPLIANT

TO-220AB



Top View

G D S



N-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	80	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150\text{ }^\circ\text{C}$ )	$I_D$	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 70\text{ }^\circ\text{C}$	
		$T_A = 25\text{ }^\circ\text{C}$	
		$T_A = 70\text{ }^\circ\text{C}$	
Pulsed Drain Current ( $t = 100\text{ }\mu\text{s}$ )	$I_{DM}$	350	A
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	
		$T_A = 25\text{ }^\circ\text{C}$	
Single Pulse Avalanche Current	$I_{AS}$	30	mJ
Single Pulse Avalanche Energy	$E_{AS}$	45	
Maximum Power Dissipation	$P_D$	$T_C = 25\text{ }^\circ\text{C}$	W
		$T_C = 70\text{ }^\circ\text{C}$	
		$T_A = 25\text{ }^\circ\text{C}$	
		$T_A = 70\text{ }^\circ\text{C}$	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)		260	

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	15	18	$^\circ\text{C/W}$
		40	50	
Maximum Junction-to-Case	$R_{thJC}$	0.85	1.1	

#### Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10\text{ s}$ .

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	80			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		37		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 6.1		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0		3.5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	85			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		7		mΩ
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 15 A		7.5		
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		9		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 20 A		60		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, f = 1 MHz		3855		pF
Output Capacitance	C <sub>oss</sub>			1120		
Reverse Transfer Capacitance	C <sub>rss</sub>			376		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		35.5		nC
		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 6 V, I <sub>D</sub> = 10 A		22		
		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		18		
Gate-Source Charge	Q <sub>gs</sub>			5.3		
Gate-Drain Charge	Q <sub>gd</sub>			7.3		
Output Charge	Q <sub>oss</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V		57	86	
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.5	1.3	2	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 40 V, R <sub>L</sub> = 4 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		12	24	ns
Rise Time	t <sub>r</sub>			8	16	
Turn-Off DelayTime	t <sub>d(off)</sub>			32	64	
Fall Time	t <sub>f</sub>			7	14	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 40 V, R <sub>L</sub> = 4 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 6.0 V, R <sub>g</sub> = 1 Ω		14	28	
Rise Time	t <sub>r</sub>			11	22	
Turn-Off DelayTime	t <sub>d(off)</sub>			30	60	
Fall Time	t <sub>f</sub>			8	16	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			75	A
Pulse Diode Forward Current (t = 100 μs)	I <sub>SM</sub>				150	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 5 A		0.76	1.1	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		38	75	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			36	70	nC
Reverse Recovery Fall Time	t <sub>a</sub>			19		ns
Reverse Recovery Rise Time	t <sub>b</sub>			19		

**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

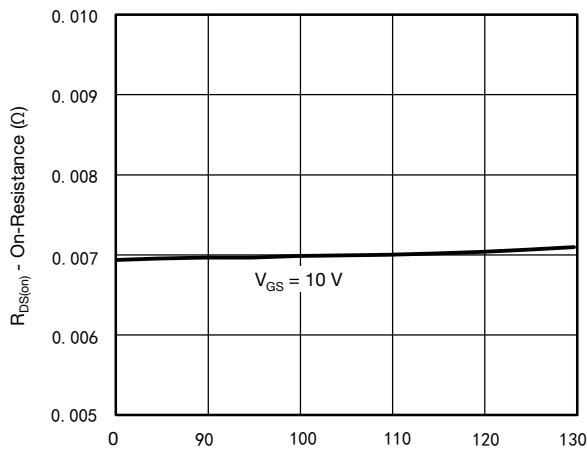
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Output Characteristics



Transfer Characteristics



On-Resistance vs. Drain Current



Capacitance



Gate Charge



On-Resistance vs. Junction Temperature

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



**Current Derating\***



**Power, Junction-to-Case**



**Power, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

## TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118
ECN: X12-0208-Rev. N, 08-Oct-12 DWG: 5471				

**Notes**

\* M = 1.32 mm to 1.62 mm (dimension including protrusion)  
 Heatsink hole for HVM

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