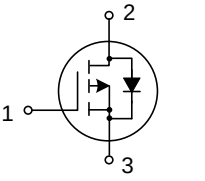
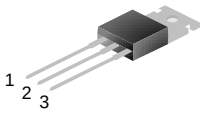
# -12A, -55V P-CHANNEL MOSFET

## GENERAL DESCRIPTION

SVD9Z24NT is a P-channel enhancement mode power MOS field effect transistor which is produced using Silan planar VDMOS process. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. This device is widely used in push-pull amplifier, high-side switching circuit, CMOS power amplifier.




1.Gate 2.Drain 3.Source




TO-220-3L

## FEATURES

- -12A, -55V ,$R_{DS(on)(typ.)}$<175mΩ@$V_{GS}$=-10V
- P channel
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

## ORDERING INFORMATION

| Part No. | Package | Marking | Harzardous Substance Control | Packing Type |
|---|---|---|---|---|
| SVD9Z24NT | TO-220-3L | SVD9Z24N | Pb free | Tube |

## ABSOLUTE MAXIMUM RATINGS ($T_C$=25°C unless otherwise noted)

| Characteristics | | Symbol | Ratings | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -55 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | V |
| Drain Current | $T_C$=25°C | $I_D$ | -12 | A |
| | $T_C$=100°C | | -8.5 | |
| Drain Current Pulsed | | $I_{DM}$ | -48 | A |
| Power Dissipation($T_C$=25°C) | | $P_D$ | 45 | W |
| -Derate above 25°C | | | 0.36 | W/°C |
| Single Pulsed Avalanche Energy (Note 1) | | $E_{AS}$ | 106 | mJ |
| Operation Junction Temperature Range | | $T_J$ | -55～+175 | °C |
| Storage Temperature Range | | $T_{stg}$ | -55～+175 | °C |

## THERMAL CHARACTERISTICS

| Characteristics | Symbol | Ratings | Unit |
|---|---|---|---|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 2.78 | °C/W |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 62.5 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_C$=25°C UNLESS OTHERWISE NOTED)

| Characteristics | Symbol | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Drain -Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V, $I_D$=-250μA | -55 | -- | -- | V |
| Drain-Source Leakage Current | $I_{DSS}$ | $V_{DS}$=-55V, $V_{GS}$=0V | -- | -- | -25 | μA |
| Gate-Source Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V, $V_{DS}$=0V | -- | -- | ±100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS}$=$V_{DS}$, $I_D$=-250μA | -2.0 | -- | -4.0 | V |
| Static Drain-Source On State Resistance | $R_{DS(on)}$ | $V_{GS}$=-10V, $I_D$=-7.2A | -- | -- | 175 | mΩ |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=-25V, $V_{GS}$=0V, f=1.0MHz | -- | 447 | -- | pF |
| Output Capacitance | $C_{oss}$ | | -- | 135 | -- | |
| Reverse Transfer Capacitance | $C_{rss}$ | | -- | 30 | -- | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$=-28V,$V_{GS}$=-10V, $R_G$=24Ω,$I_D$=-7.2A (Note 2,3) | -- | 8.47 | -- | ns |
| Turn-on Rise Time | $t_r$ | | -- | 41.2 | -- | |
| Turn-off Delay Time | $t_{d(off)}$ | | -- | 30 | -- | |
| Turn-off Fall Time | $t_f$ | | -- | 20.2 | -- | |
| Total Gate Charge | $Q_g$ | $V_{DS}$=-44V,$V_{GS}$=-10V, $I_D$=-7.2A (Note 2,3) | -- | 13 | -- | nC |
| Gate-Source Charge | $Q_{gs}$ | | -- | 3.25 | -- | |
| Gate-Drain Charge | $Q_{gd}$ | | -- | 5.3 | -- | |

## SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

| Characteristics | Symbol | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Continuous Source Current | $I_S$ | Integral Reverse P-N Junction Diode in the MOSFET | -- | -- | -12 | A |
| Pulsed Source Current | $I_{SM}$ | | -- | -- | -48 | |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=-7.2A, $V_{GS}$=0V | -- | -- | -1.6 | V |
| Reverse Recovery Time | $T_{rr}$ | $I_S$=-7.2A, $V_{GS}$=0V, $dI_F/dt$=100A/μs (Note 2) | -- | 50.5 | -- | ns |
| Reverse Recovery Charge | $Q_{rr}$ | | -- | 0.11 | -- | μC |

**Notes:**

1. L=3.7mH, $I_{AS}$= -8A, $R_G$=25Ω, starting $T_J$=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

## TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

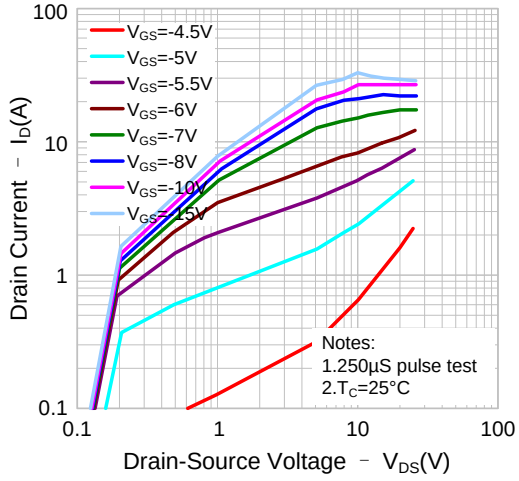



Figure 2. Transfer Characteristics

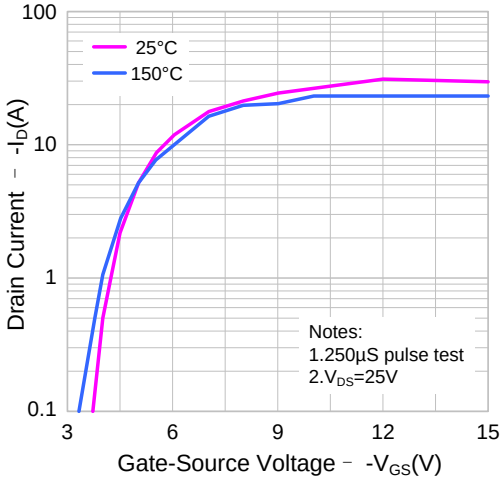



Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

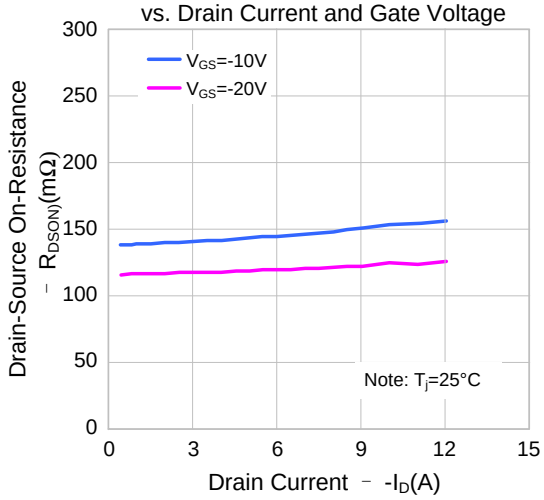



Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

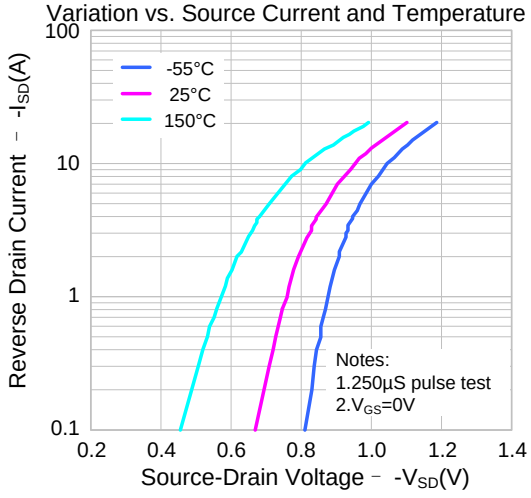



Figure 5. Capacitance Characteristics

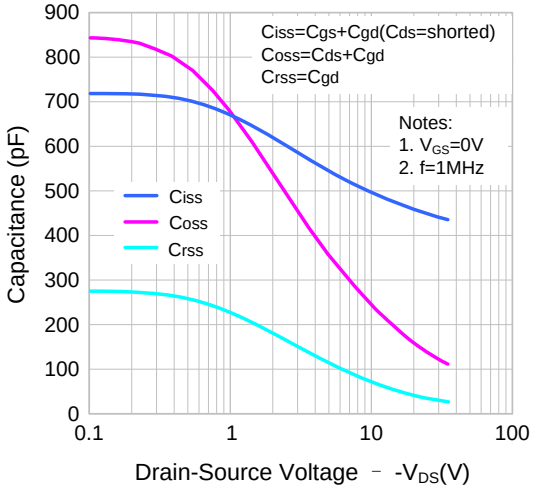
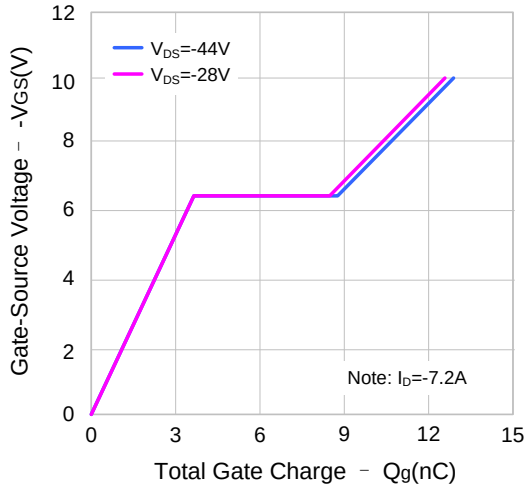



Figure 6. Gate Charge Characteristics



## TYPICAL CHARACTERISTICS (CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

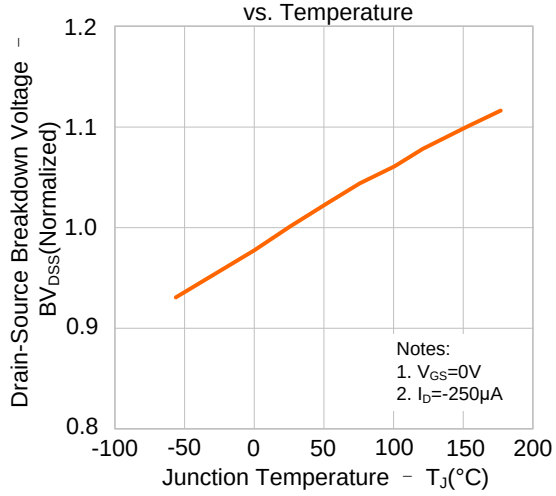



Figure 8. On-resistance Variation vs. Temperature

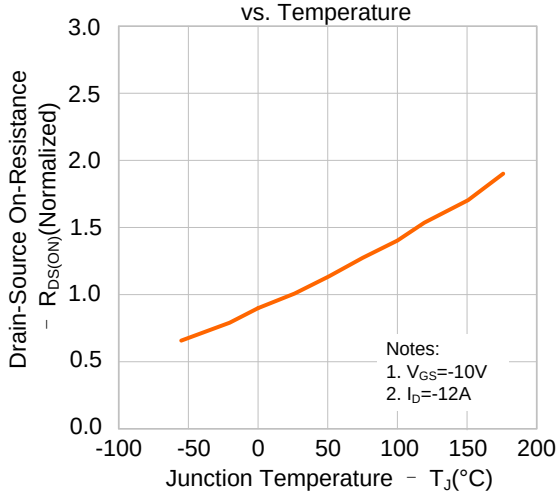



Figure 9. Max. Safe Operating Area

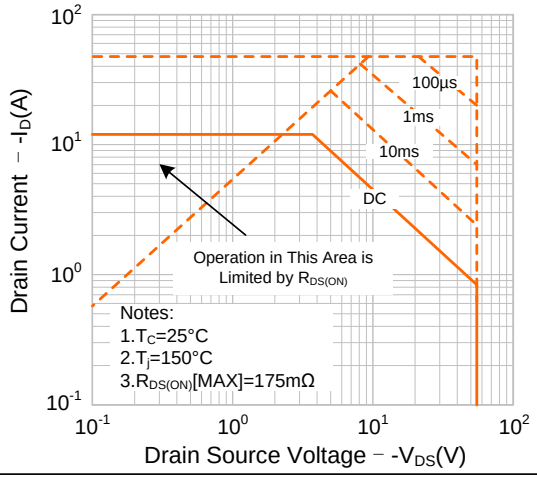
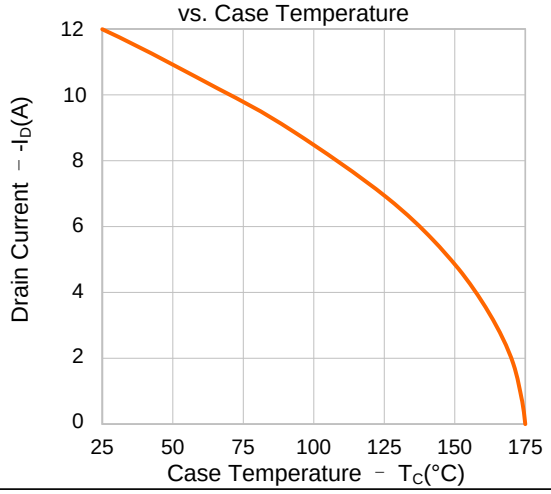
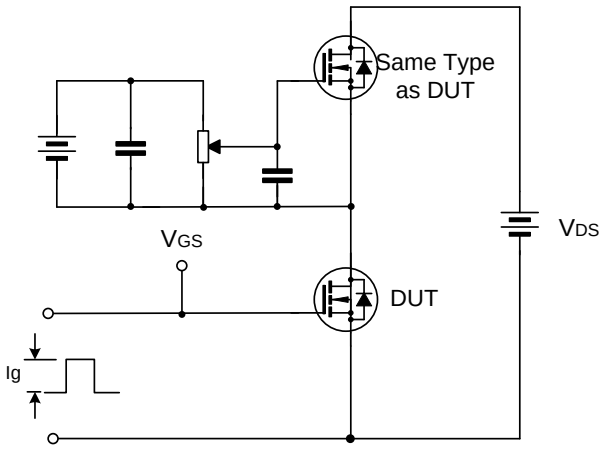


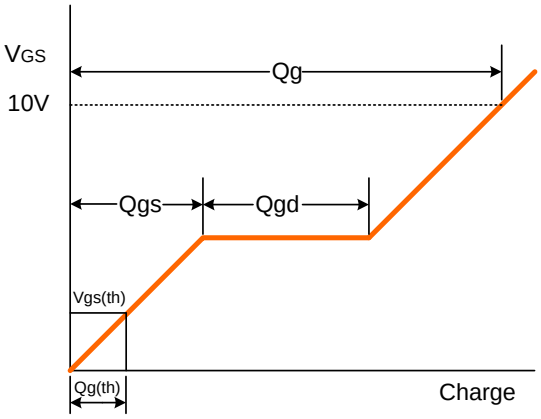

Figure 10. Maximum Drain Current vs. Case Temperature



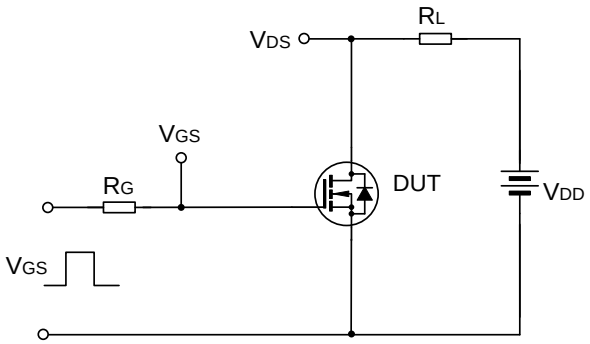
## TYPICAL TEST CIRCUIT

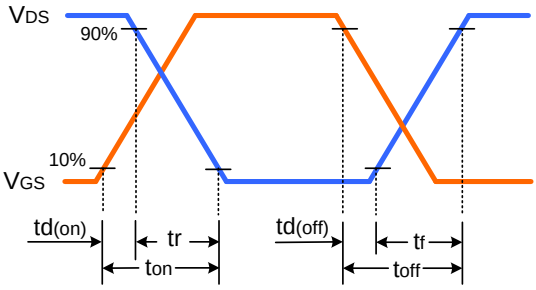
Gate Charge Test Circuit & Waveform



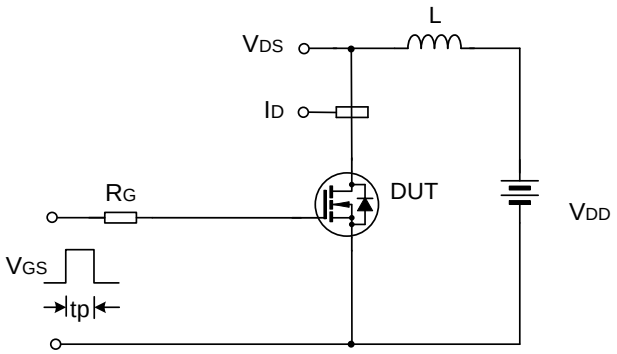




Resistive Switching Test Circuit & Waveform

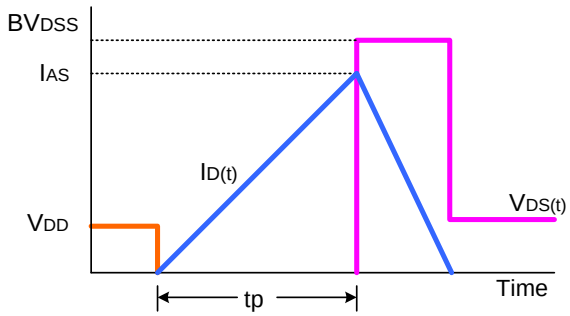



Unclamped Inductive Switching Test Circuit & Waveform

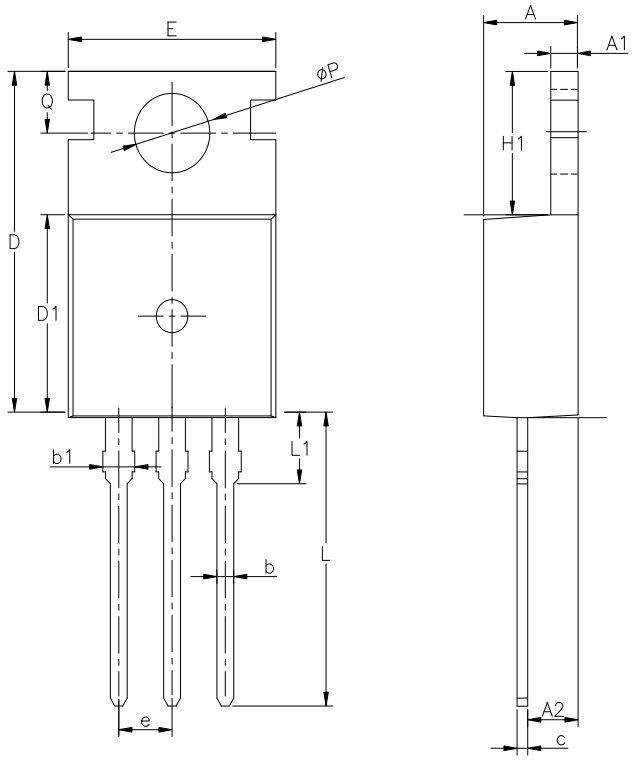



$$E_{AS} = \frac{1}{2} LI_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



## PACKAGE OUTLINE

**TO-220-3L** **UNIT: mm**




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 4.30 | 4.50 | 4.70 |
| A1 | 1.00 | 1.30 | 1.50 |
| A2 | 1.80 | 2.40 | 2.80 |
| b | 0.60 | 0.80 | 1.00 |
| b1 | 1.00 | — | 1.60 |
| c | 0.30 | — | 0.70 |
| D | 15.10 | 15.70 | 16.10 |
| D1 | 8.10 | 9.20 | 10.00 |
| E | 9.60 | 9.90 | 10.40 |
| e | 2.54BSC | | |
| H1 | 6.10 | 6.50 | 7.00 |
| L | 12.60 | 13.08 | 13.60 |
| L1 | — | — | 3.95 |
| ϕP | 3.40 | 3.70 | 3.90 |
| Q | 2.60 | — | 3.20 |

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Rev.: 1.4

Revision History:

1. Modify marketing
2. Modify the template of datasheet

Rev.: 1.3

Revision History:

1. Modify $V_{GS}$ to -10V
2. Modify the Electrical diagram
3. Modify Fig 1
4. Modify TYPICAL TEST CIRCUIT（take the Chinese version as the standard）

Rev.: 1.2

Revision History:

1. Modify the
2. Modify the source-drain diode ratings and characteristics
3. Modify the electrical characteristics

Rev.: 1.1

Revision History:

1. Modify the package information of TO-220-3L

Rev.: 1.0

Revision History:

1. First release