

13A, 500V N-CHANNEL MOSFET

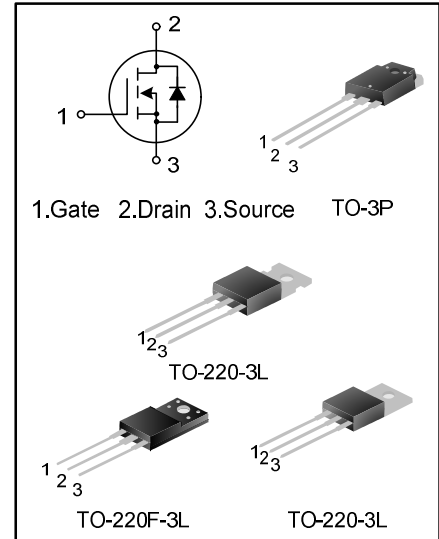
GENERAL DESCRIPTION

SVF13N50T/F/PN is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

This device is widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- ◆ 13A, 500V, $R_{DS(on)(typ.)} = 0.44\Omega @ V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low Crss
- ◆ Fast switching
- ◆ Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVF13N50F	TO-220F-3L	SVF13N50F	Pb free	Tube
SVF13N50T	TO-220-3L	SVF13N50T	Pb free	Tube
SVF13N50PN	TO-3P	13N50	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_c=25°C, unless otherwise noted)

Characteristics	Symbol	Ratings			Unit
		SVF13N50T	SVF13N50F	SVF13N50PN	
Drain-Source Voltage	V _{DS}	500			V
Gate-Source Voltage	V _{GS}	±30			V
Drain Current	I _D	T _C =25°C			A
		T _C =100°C			
Drain Current Pulsed	I _{DM}	52			A
Power Dissipation(T _C =25°C) - Derate above 25°C	P _D	190	51	218	W
		1.52	0.41	1.74	W/°C
Single Pulsed Avalanche Energy (Note 1)	E _{AS}	663			mJ
Operation Junction Temperature Rating	T _J	-55~+150			°C
Storage Temperature Rating	T _{stg}	-55~+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings			Unit
		SVF13N50T	SVF13N50F	SVF13N50PN	
Thermal Resistance, Junction-to-Case	R _{θJC}	0.66	2.45	0.57	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	62.5	50	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain –Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	500	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =500V, V _{GS} =0V	--	--	1	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} =V _{DS} , I _D =250μA	2.0	--	4.0	V
On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =6.5A	--	0.44	0.52	Ω
Input Capacitance	C _{iSS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHZ	--	1340	--	pF
Output Capacitance	C _{oss}		--	170	--	
Reverse Transfer Capacitance	C _{rSS}		--	13.0	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =250V, I _D =13A, R _G =4.7Ω, V _{GS} =10V (Note 2,3)	--	25.53	--	ns
Turn-on Rise Time	t _r		--	48.80	--	
Turn-off Delay Time	t _{d(off)}		--	72.33	--	
Turn-off Fall Time	t _f		--	40.27	--	
Total Gate Charge	Q _g	V _{DS} =400V, I _D =13A, V _{GS} =10V (Note 2,3)	--	29.5	--	nC
Gate-Source Charge	Q _{gs}		--	8.00	--	
Gate-Drain Charge	Q _{gd}		--	12.3	--	

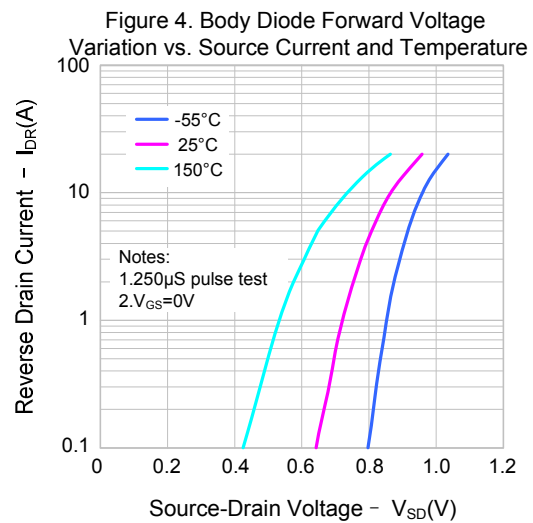
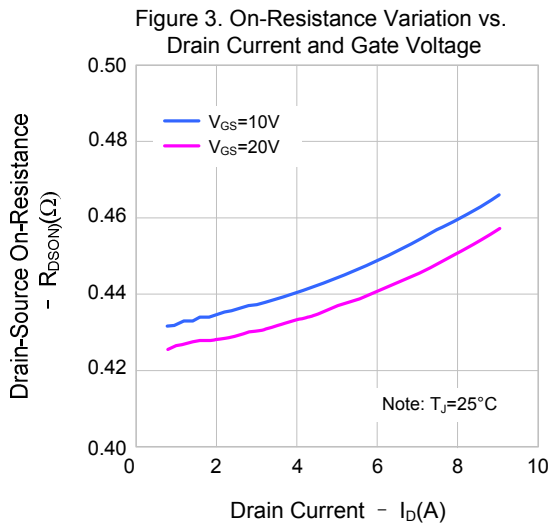
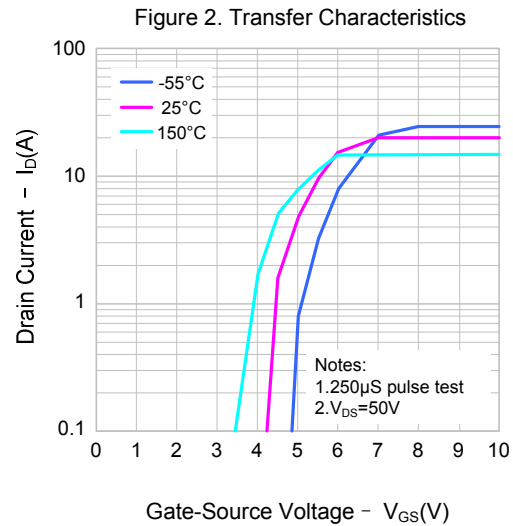
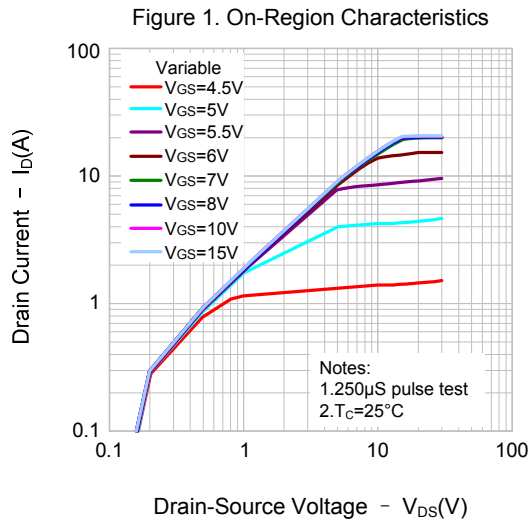
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction	--	--	13	A
Pulsed Source Current	I_{SM}	Diode in the MOSFET	--	--	52	
Diode Forward Voltage	V_{SD}	$I_S=13A, V_{GS}=0V$	--	--	1.3	V
Reverse Recovery Time	T_{rr}	$I_S=13A, V_{GS}=0V,$	--	495	--	ns
Reverse Recovery Charge	Q_{rr}	$dl_f/dt=100A/\mu S$ (Note 2)	--	5.0	--	μC

Notes:

1. $L=30mH, I_{AS}=7.5A, V_{DD}=100V, R_G=25\Omega,$ starting $T_J=25^\circ C;$
2. Pulse Test: Pulse width $\leq 300\mu s,$ Duty cycle $\leq 2\%;$
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS(continued)

Figure 5. Capacitance Characteristics

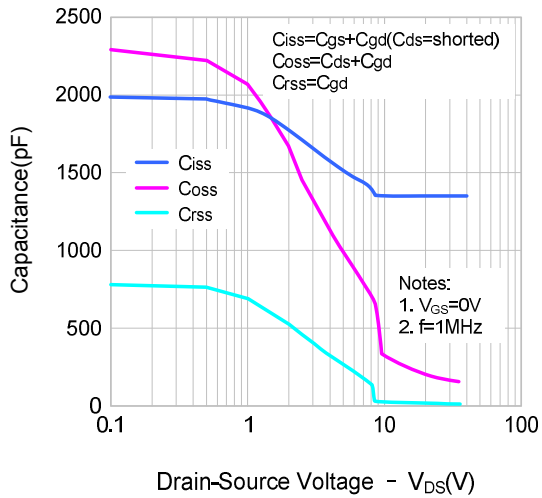


Figure 6. Gate Charge Characteristics

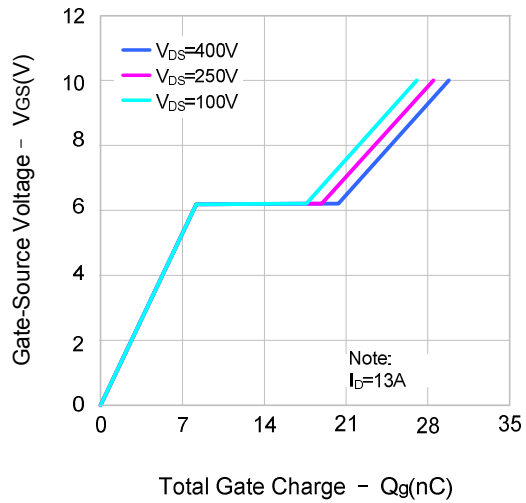


Figure 7. Breakdown Voltage Variation vs. Temperature

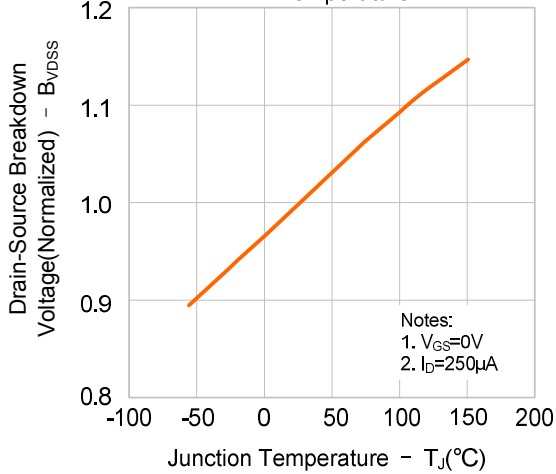


Figure 8. On-resistance Variation vs. Temperature

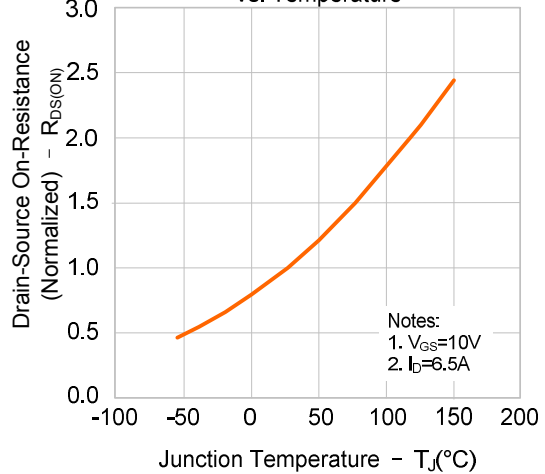


Figure 9-1. Max. Safe Operating Area(SVF13N50T)

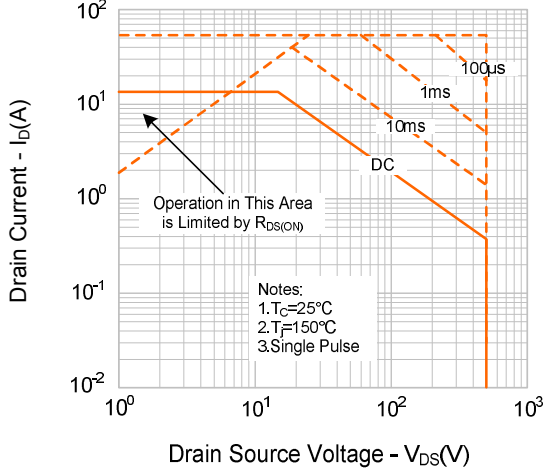
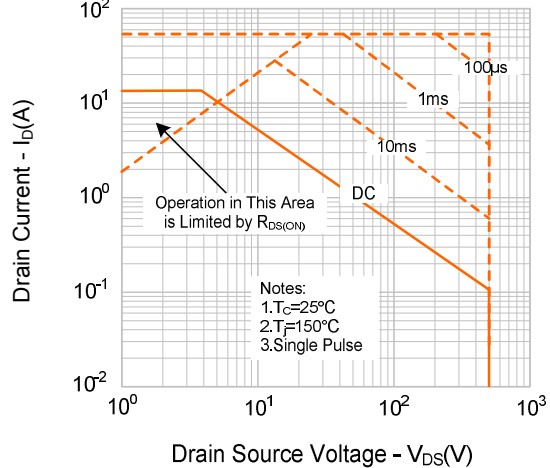
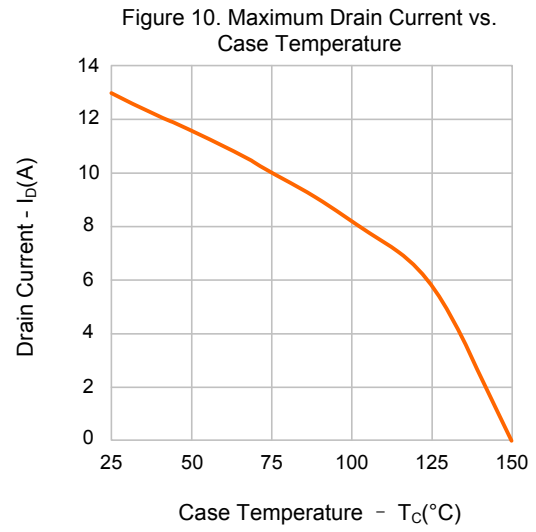
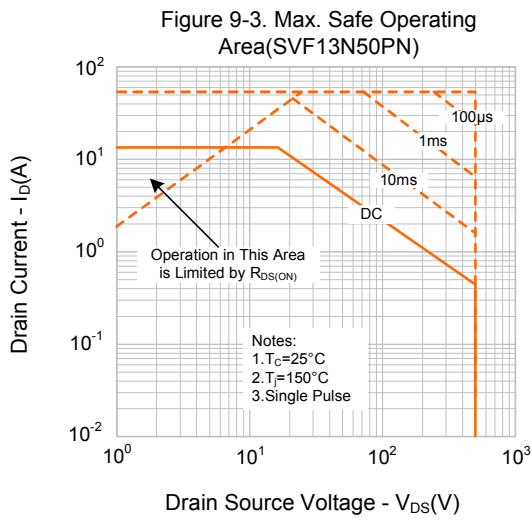


Figure 9-2. Max. Safe Operating Area(SVF13N50F)

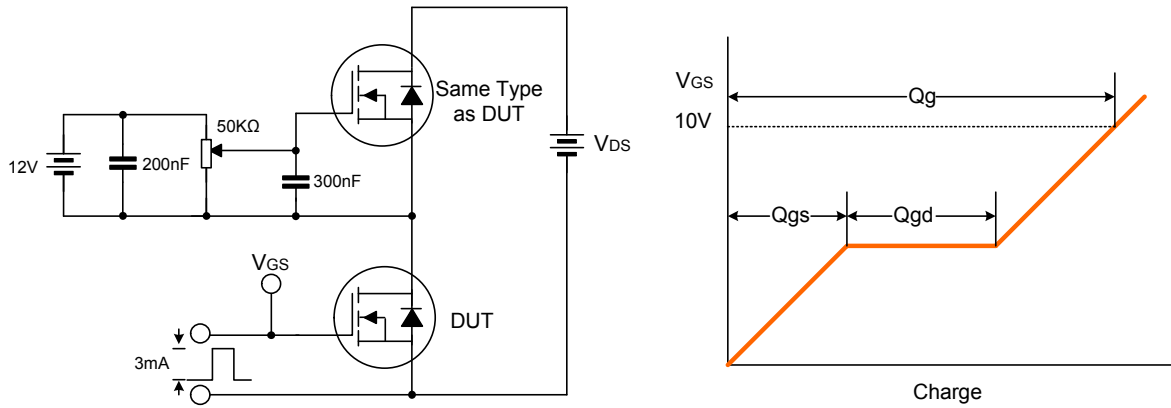


TYPICAL CHARACTERISTICS(continued)

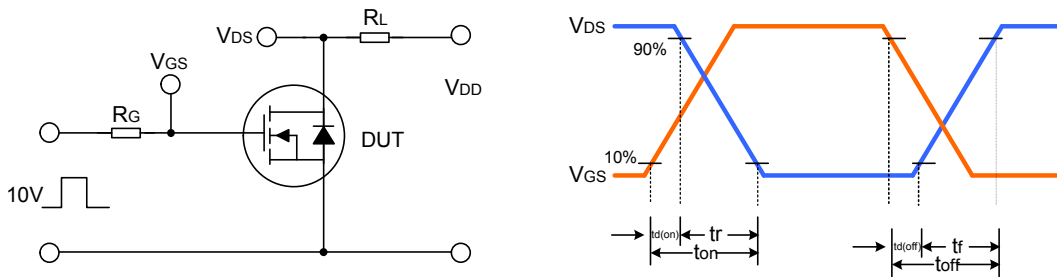


TYPICAL TEST CIRCUIT

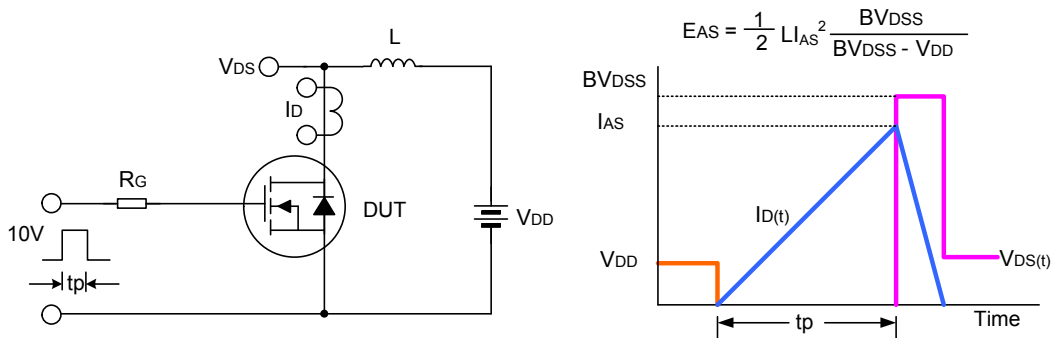
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

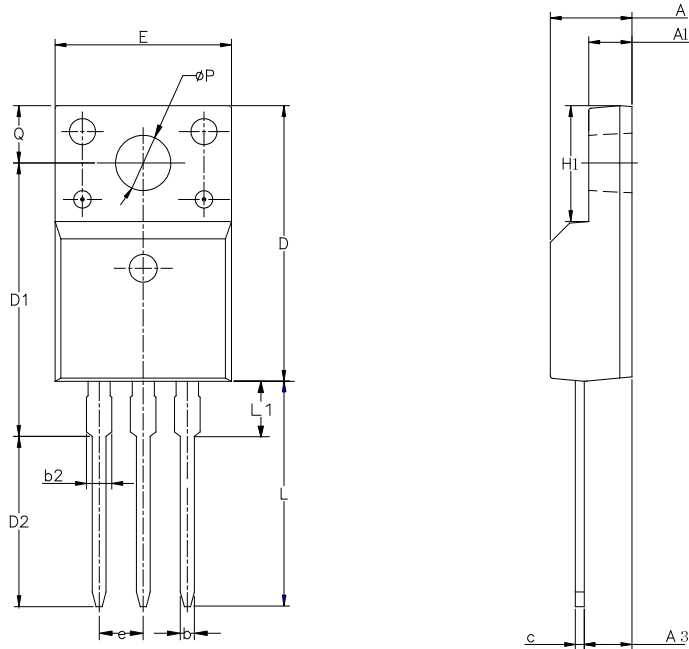


Unclamped Inductive Switching Test Circuit & Waveform



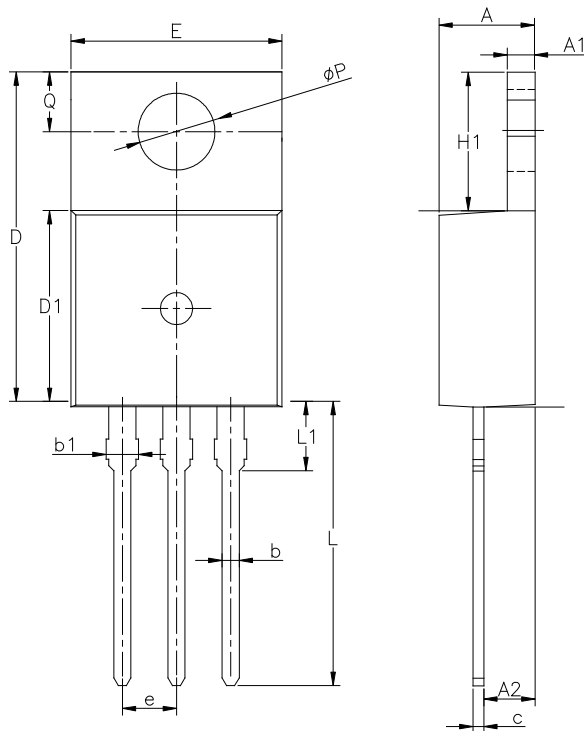
PACKAGE OUTLINE

TO-220F-3L UNIT: mm



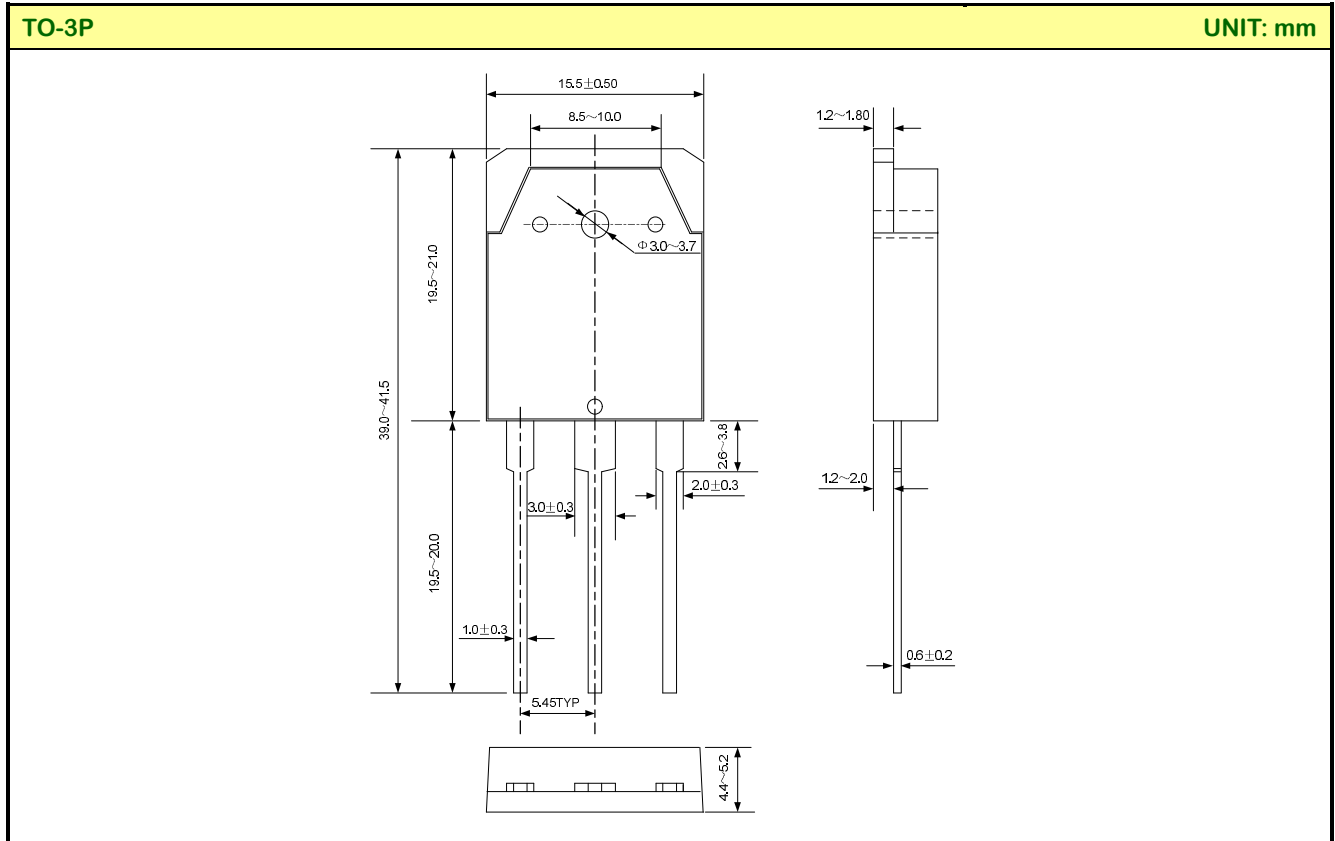
SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

TO-220-3L 单位: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ϕP	3.40	3.70	3.90
Q	2.60	—	3.20

PACKAGE OUTLINE



Disclaimer :

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without prior notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
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Rev.: 2.0

Revision History:

1. Add another solid figure of TO-220-3L
-

Rev.: 1.9

Revision History:

1. Modify the Electrical characteristics
-

Rev.: 1.8

Revision History:

1. Modify the package information of TO-220F-3L
 2. Modify the package information of TO-220-3L
-

Rev.: 1.7

Revision History:

1. Modify the thermal characteristics
-

Rev.: 1.6

Revision History:

1. Modify the ordering information
-

Rev.: 1.5

Revision History:

1. Change the schematic diagram of MOS
-

Rev.: 1.4

Revision History:

1. Modify "ELECTRICAL CHARACTERISTICS"
-

Rev.: 1.3

Revision History:

1. Modify the values of T_{rr} and Q_{rr}
-

Rev.: 1.2

Revision History:

1. Add the halogen free information of SVF13N50F
-

Rev.: 1.1

Revision History:

1. Modify "PACKAGE OUTLINE"
-

Rev.: 1.0

Revision History:

1. Original
-
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