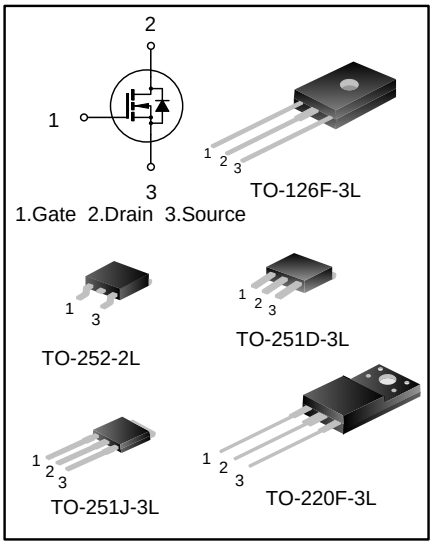
2A, 600V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF2N60M(MJ)(NF)(F)(D) is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 2A,600V,$R_{DS(on)(typ.)}$=3.7Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package Type	Marking	Hazardous substance control	Packing Type
SVF2N60M	TO-251D-3L	SVF2N60M	Halogen free	Tube
SVF2N60MJ	TO-251J-3L	SVF2N60MJ	Halogen free	Tube
SVF2N60NF	TO-126F-3L	SVF2N60NF	Pb free	Tube
SVF2N60F	TO-220F-3L	SVF2N60F	Pb free	Tube
SVF2N60DTR	TO-252-2L	SVF2N60D	Halogen free	Tape&Reel

ABSOLUTE MAXIMUM RATINGS (T_A=25°C UNLESS OTHERWISE NOTED)

Characteristics		Symbol	Ratings				Unit
			SVF2N 60NF	SVF2N 60M/D	SVF2N 60MJ	SVF2N 60F	
Drain-Source Voltage		V_{DS}	600				V
Gate-Source Voltage		V_{GS}	±30				V
Drain Current	T_C=25°C	I_D	2.0				A
	T_C=100°C		1.3				
Drain Current Pulsed		I_{DM}	8.0				A
Power Dissipation(T_C=25°C)		P_D	16	34	35	23	W
-Derate above 25°C			0.13	0.27	0.28	0.18	W/°C
Single Pulsed Avalanche Energy(Note1)		E_{AS}	115				mJ
Operation Junction Temperature Range		T_J	-55～+150				°C
Storage Temperature Range		T_{stg}	-55～+150				°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings				Unit
		SVF2N 60NF	SVF2N 60M/D	SVF2N 60MJ	SVF2N 60F	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	7.81	3.7	3.57	5.56	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	120	62.0	62.0	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C UNLESS OTHERWISE NOTED)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	600	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=600V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=1.0A	--	3.7	4.2	Ω
Input Capacitance	R_g	f=1.0MHz	--	3.5	--	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHz		233		pF
Output Capacitance	C_{oss}		--	32	--	
Reverse Transfer Capacitance	C_{rss}		--	2.8	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=300V,I_D=2.0A, R_G=25Ω (Note 2,3)	--	8.9	--	ns
Turn-on Rise Time	t_r		--	23	--	
Turn-off Delay Time	$t_{d(off)}$		--	23	--	
Turn-off Fall Time	t_f		--	25	--	
Total Gate Charge	Q_g	V_{DS}=480V,I_D=2.0A, V_{GS}=10V (Note 2,3)	--	8.2	--	nC
Gate-Source Charge	Q_{gs}		--	1.6	--	
Gate-Drain Charge	Q_{gd}		--	4.4	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	2.0	A
Pulsed Source Current	I_{SM}		--	--	8.0	
Diode Forward Voltage	V_{SD}	I_S=2.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=2.0A,V_{GS}=0V, dI_F/dt=100A/μs	--	326	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.9	--	μC

Notes:

1. L=30mH, I_{AS}=2.52A, V_{DD}=100V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

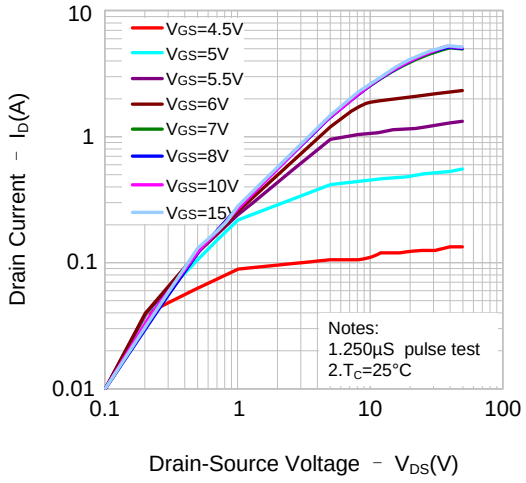


Figure 2. Transfer Characteristics

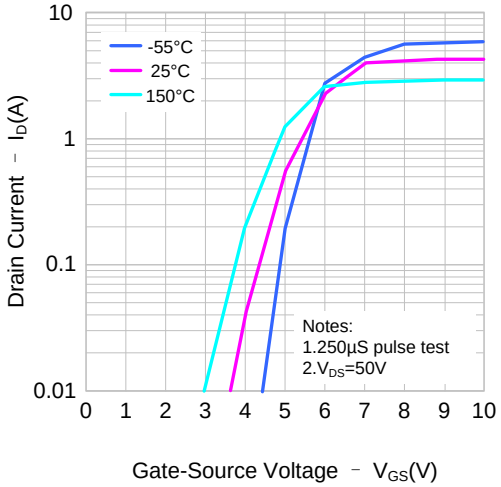


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

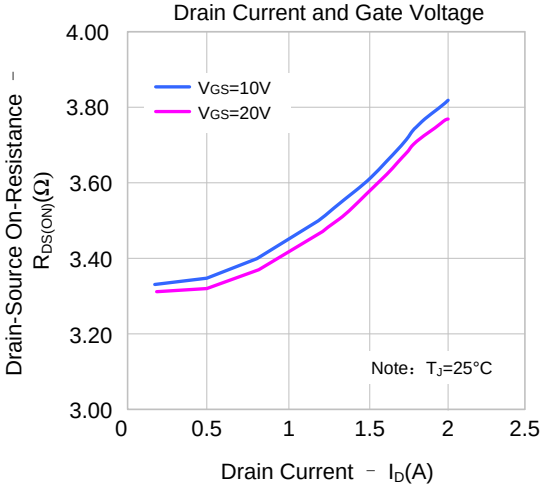


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

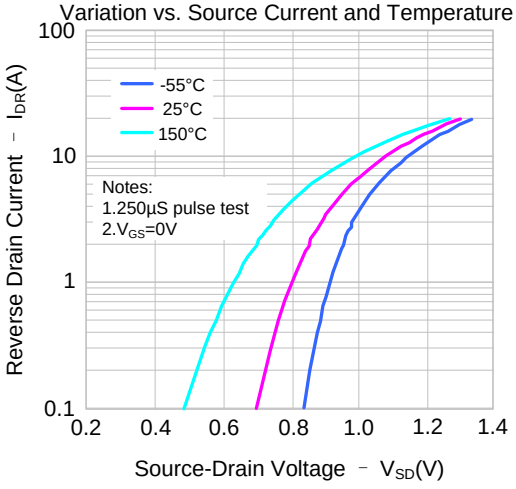


Figure 5. Capacitance Characteristics

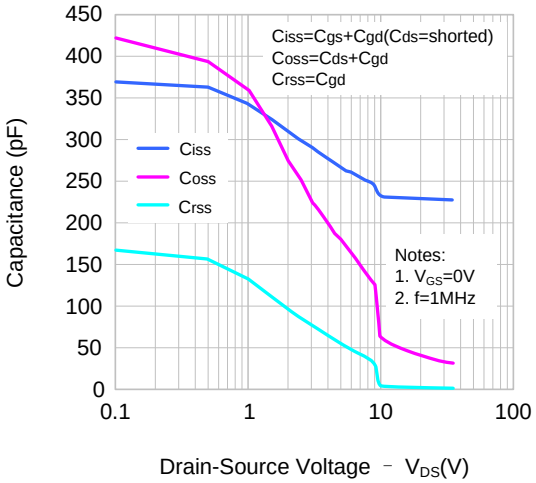
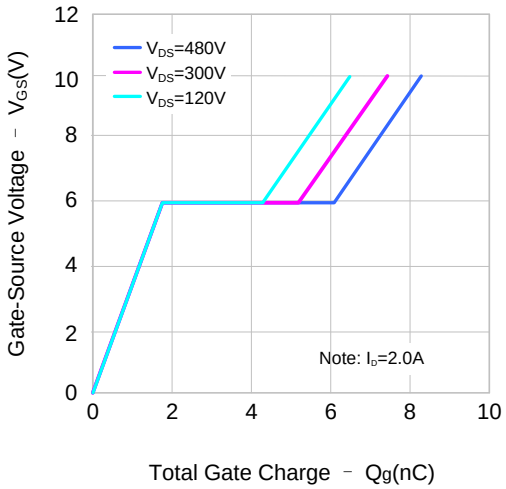


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

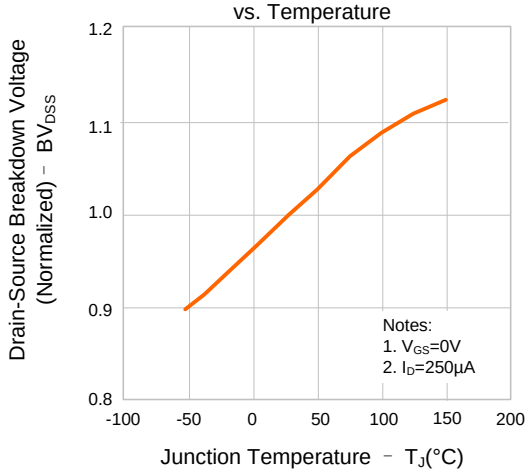


Figure 8. On-resistance vs. Temperature

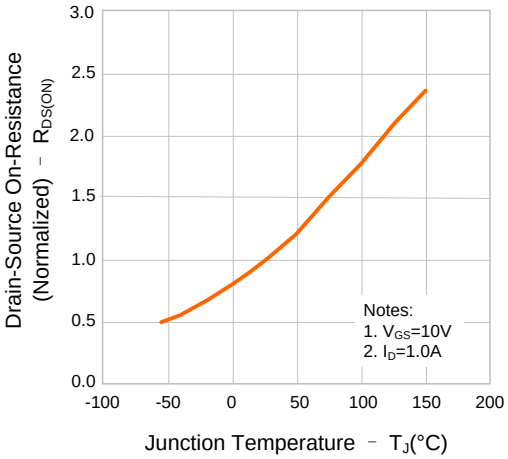


Figure 9-1. Max. Safe Operating Area(SVF2N60F)

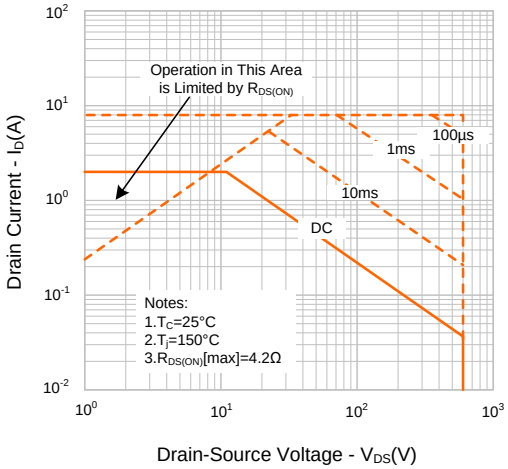


Figure 9-2. Max. Safe Operating Area(SVF2N60NF)

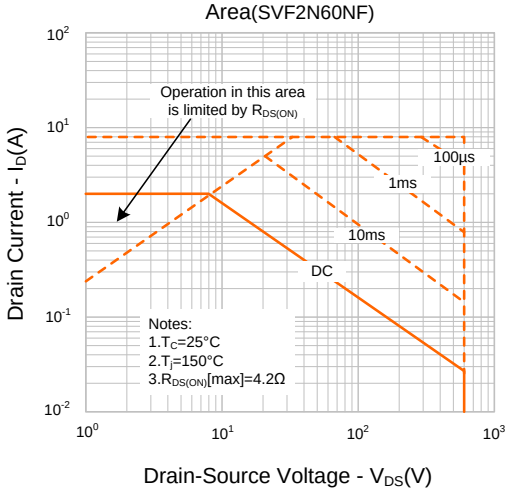


Figure 9-3. Max. Safe Operating Area(SVF2N60M/D)

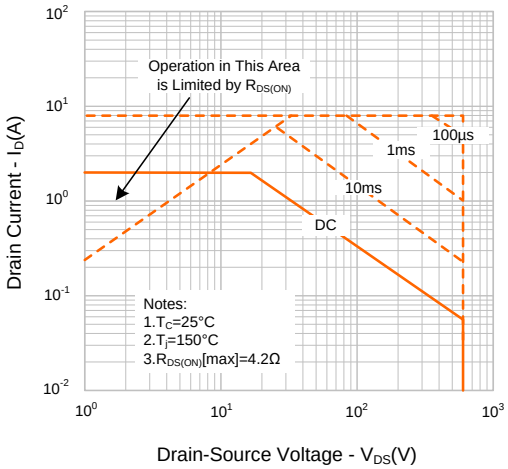
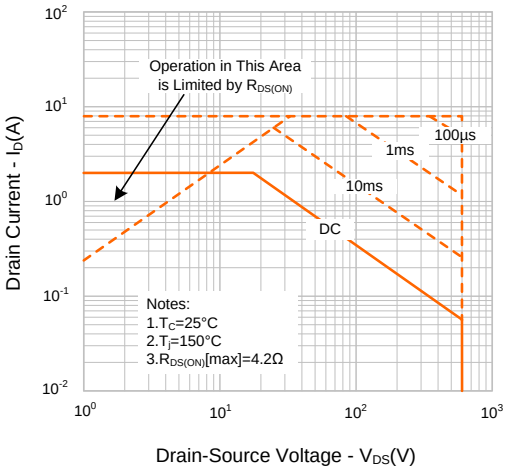
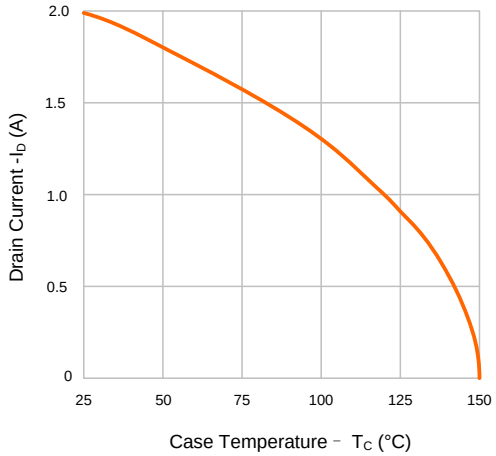


Figure 9-4. Max. Safe Operating Area(SVF2N60MJ)

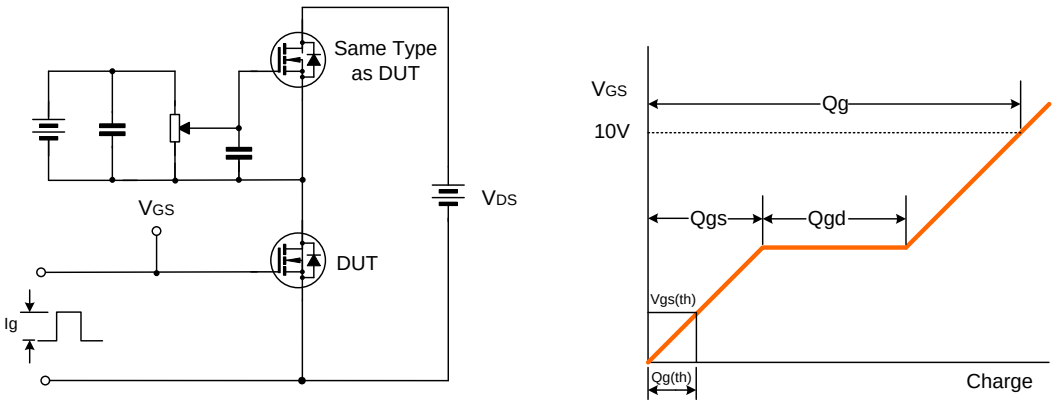


TYPICAL CHARACTERISTICS(CONTINUED)

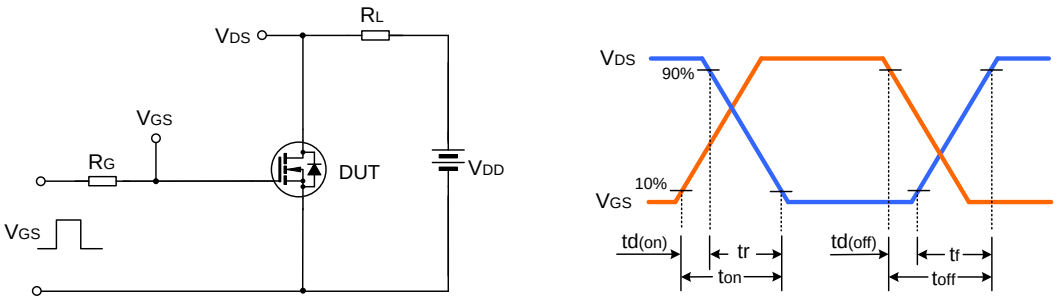
Figure 10. Max. Drain Current vs. Case Temperature



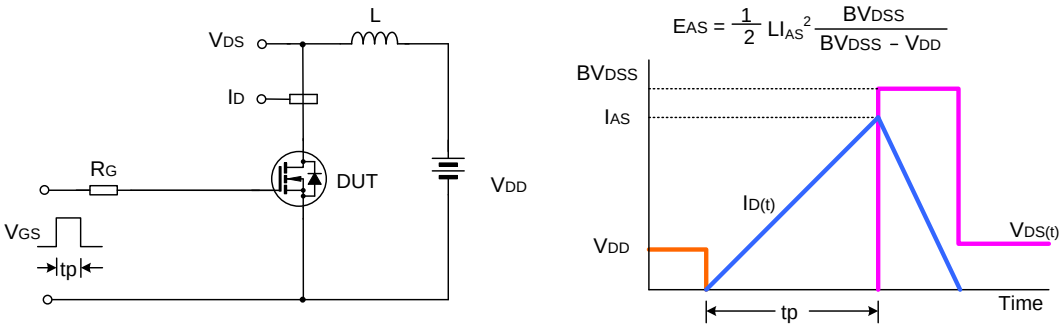
TYPICAL TEST CIRCUIT



Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

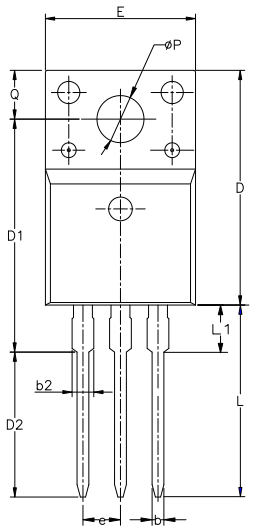


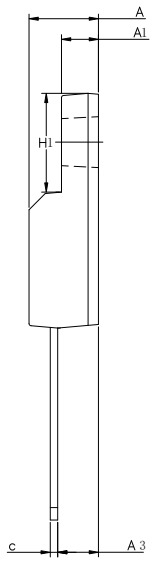
Unclamped Inductive Switching Test Circuit & Waveform

PACKAGE OUTLINE

TO-220F-3L

单位：毫米

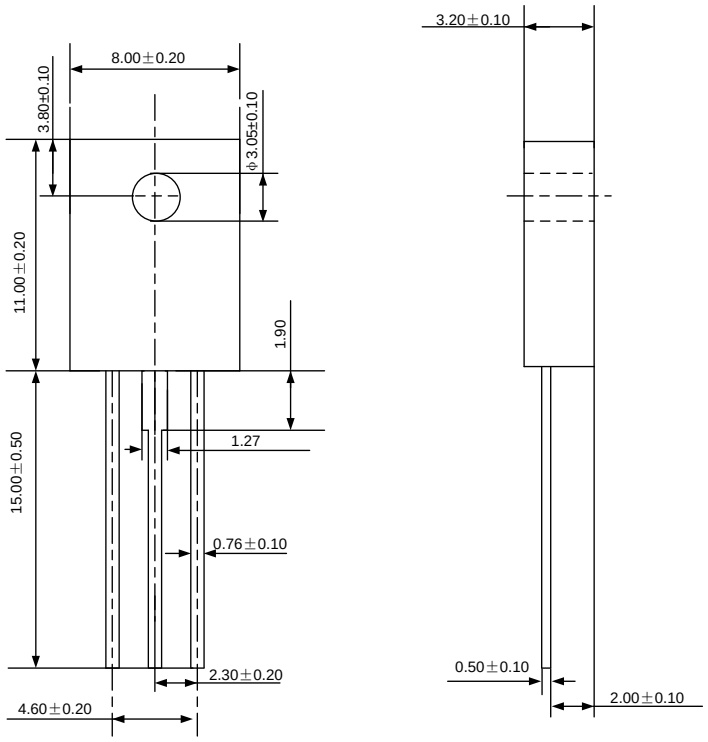




SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e		2.54BCS	
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
ØP	3.00	3.18	3.40
Q	3.05	3.30	3.55

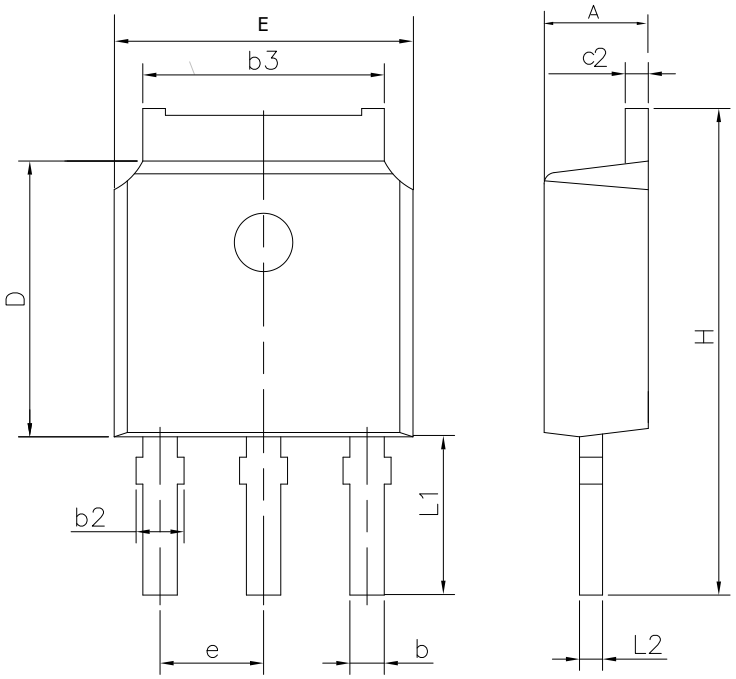
TO-126F-3L

UNIT: mm



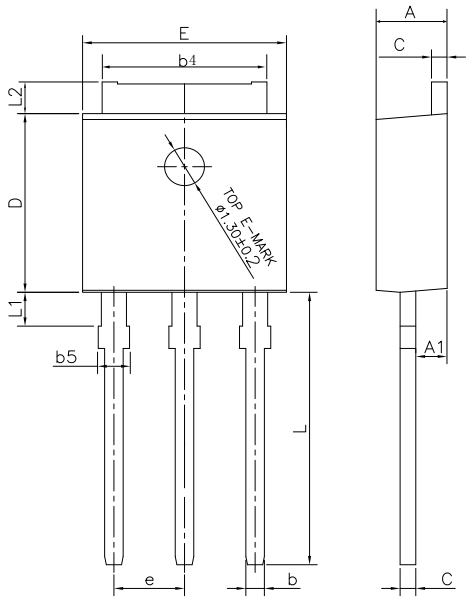
PACKAGE OUTLINE(CONTINUED)

TO-251D-3L **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.40
b	0.66	---	0.86
b2	0.72	---	0.90
b3	5.10	5.33	5.46
c2	0.46	---	0.60
D	6.00	6.10	6.20
E	6.50	6.60	6.70
e	2.186	2.286	2.386
H	10.40	10.70	11.00
L1	3.50 REF		
L2	0.508 BSC		

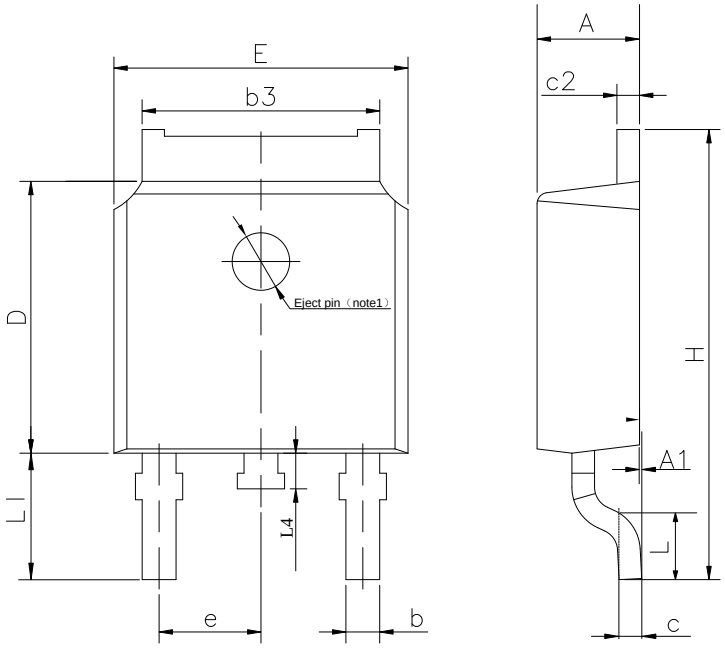
TO-251J-3L **UNIT: mmc**



SYMBOL	MIN	NOM	MAX
A	2.18	2.30	2.39
A1	0.89	1.00	1.14
b	0.56	---	0.89
b4	4.95	5.33	5.46
b5	---	---	1.05
c	0.46	---	0.61
D	5.97	6.10	6.27
E	6.35	6.60	6.73
e	2.29 BCS		
L	8.89	9.30	9.65
L1	0.95	---	1.50
L2	0.89	---	1.27

PACKAGE OUTLINE(CONTINUED)

TO-252-2L **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e		2.30TYP	
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1		2.90REF	
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

Important notice:

- **The instructions are subject to change without notice！ Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.**
- **Our products are consumer electronic products, and / or civil electronic products.**
- **When using our products, please do not exceed the maximum rating of the products, otherwise the reliability of the whole machine will be affected. There is a certain possibility of failure or malfunction of any semiconductor product under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design, sample and whole machine manufacturing, so as to avoid potential failure risk that may cause personal injury or property loss.**
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Part No.:	SVF2N60M/MJ/NF/F/D	Document Type:	Datasheet
Copyright:	HANGZHOU SILAN MICROELECTRONICS CO.,LTD	Website:	http: //www.silan.com.cn

Rev.: 3.6

Revision History:

1. Modify Electrical schematic and TYPICAL TEST CIRCUIT
2. Modify some errors

Rev.: 3.5

Revision History:

1. Delete the package outline of TO-220-3L
2. Delete the package outline of TO-126-3L

Rev.: 3.4

Revision History:

1. Update the package outline of TO-251J-3L
2. Delete the package outline of TO-220F-3L(2)

Rev.: 3.3

Revision History:

1. Update characteristics

Rev.: 3.2

Revision History:

1. Modify the Ordering information

Rev.: 3.1

Revision History:

1. Modify the package outline of TO-126-3L
2. Modify the package outline of TO-251 D -3L

Rev.: 3.0

Revision History:

1. Modify the package information of TO-220-3L

Rev.: 2.9

Revision History:

1. Modify the package of TO-220F-3L;Modify the package of TO-252-2L;

Rev.: 2.8

Revision History:

1. Modify the thermal characteristics

Rev.: 2.7

Revision History:

1. Modify the note 1

Rev.: 2.6

Revision History:

1. Add the pin No.

Rev.: 2.5

Revision History:

1. Modify the package outline of TO-251J-3L

Rev.: 2.4

Revision History:

1. Modify the ordering information

Rev.: 2.3

Revision History:

1. Modify the package outline of TO-126-3L
1. Change the schematic diagram of MOS

Rev.: 2.1

Revision History:

1. Modify the package outline of TO-251D-3L; Add the value of forward transconductance

Rev.: 2.0

Revision History:

1. Add the halogen free information of SVF2N60M

Rev.: 1.9

Revision History:

1. Modify “PACKAGE OUTLINE”

Rev.: 1.8

Revision History:

1. Add the package of TO-126-3L(2)

Rev.: 1.7

Revision History:

1. Add the package of TO-126F-3L

Rev.: 1.6

Revision History:

1. Modify the values of T_{rr} and $Q_{rr;}$ Update the package outline of TO-251D-3L

Rev.: 1.5

Revision History:

1. Add the halogen free information of SVF2N60F

Rev.: 1.4

Revision History:

1. Delete the package of TO-251-3L

Rev.: 1.3

Revision History:

1. Modify “PACKAGE OUTLINE”

Rev.: 1.2

Revision History:

1. Add the package of TO-251D-3L, TO-251J-3L, TO-126-3L

Rev.: 1.1

Revision History:

1. Modify “TYPICAL CHARACTERISTICS”, “PACKAGE OUTLINE”, the template of Datasheet

Rev.: 1.0

Revision History:

1. Original