

2A, 600V N-CHANNEL MOSFET

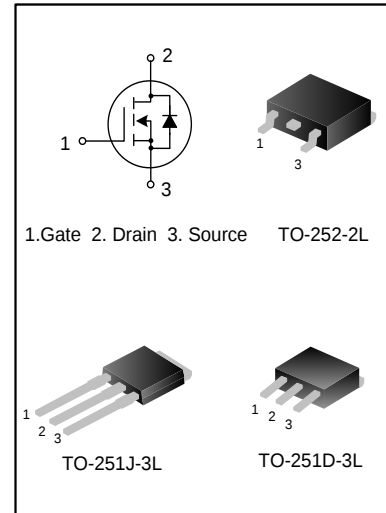
GENERAL DESCRIPTION

SVF2N60RD/M/MJ is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

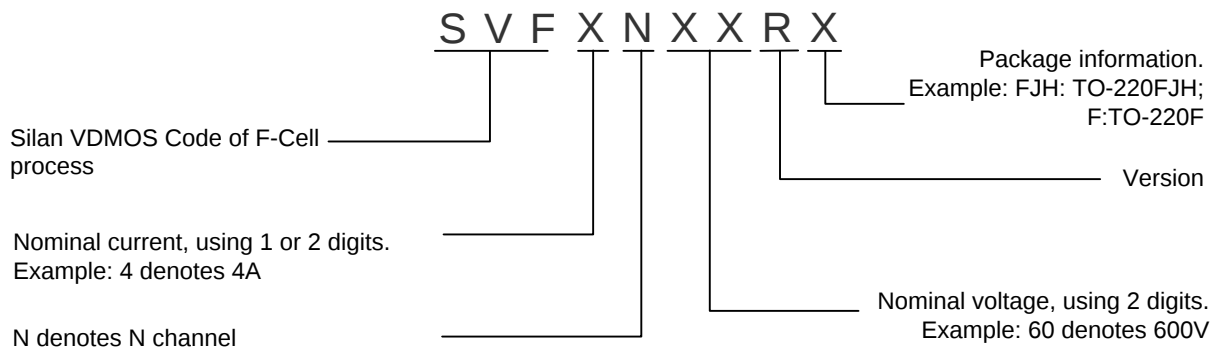
These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- * 2A, 600V, $R_{DS(on)(typ)} = 3.7\Omega @ V_{GS} = 10V$
- * Low gate charge
- * Low C_{rss}
- * Fast switching
- * Improved dv/dt capability



NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVF2N60RDTR	TO-252-2L	2N60RD	Halogen free	Tape&Reel
SVF2N60RM	TO-251D-3L	2N60RM	Halogen free	Tube
SVF2N60RMJ	TO-251J-3L	2N60RMJ	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (T_c=25°C unless otherwise noted)

Characteristics	Symbol	Rating	Unit
		SVF2N60RM/D/MJ	
Drain-Source Voltage	V _{DS}	600	V
Gate-Source Voltage	V _{GS}	±30	V
Drain Current	I _D	T _C =25°C	2.0
		T _C =100°C	1.3
Drain Current Pulsed	I _{DM}	8.0	A
Power Dissipation(T _C =25°C) -Derate above 25°C	P _D	34	W
		0.27	W/°C
Single Pulsed Avalanche Energy (Note 1)	E _{AS}	115	mJ
Reverse Diode dv/dt (Note 2)	dv/dt	4.5	V/ns
MOSFET dv/dt Ruggedness (Note 3)	dv/dt	50	V/ns
Operation Junction Temperature Range	T _J	-55~+150	°C
Storage Temperature Range	T _{stg}	-55~+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Rating	Unit
		SVF2N60RM/D/MJ	
Thermal Resistance, Junction-to-Case	R _{θJC}	3.7	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	600	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =600V, V _{GS} =0V	--	--	1.0	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =1.0A	--	3.7	4.2	Ω
Input Capacitance	R _g	f=1.0MHz	--	3.1	--	Ω
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	--	250	--	pF
Output Capacitance	C _{oss}		--	30	--	
Reverse Transfer Capacitance	C _{rss}		--	2.7	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =300V, I _D =2.0A, R _G =25Ω (Note4, 5)	--	8.04	--	ns
Turn-on Rise Time	t _r		--	22.7	--	
Turn-off Delay Time	t _{d(off)}		--	17.1	--	
Turn-off Fall Time	t _f		--	23.6	--	
Total Gate Charge	Q _g	V _{DS} =480V, I _D =2.0A, V _{GS} =10V (Note 4, 5)	--	8.92	--	nC
Gate-Source Charge	Q _{gs}		--	2.48	--	
Gate-Drain Charge	Q _{gd}		--	4.42	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I _S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	2.0	A
Pulsed Source Current	I _{SM}		--	--	8.0	
Diode Forward Voltage	V _{SD}	I _S =2.0A, V _{GS} =0V	--	--	1.4	V
Reverse Recovery Time	T _{rr}	I _S =2.0A, V _{GS} =0V, dI _F /dt=100A/μS (Note 4,)	--	330	--	ns
Reverse Recovery Charge	Q _{rr}		--	0.87	--	μC

Notes:

- L=30mH, I_{AS}=2.52A, V_{DD}=100V, R_G=25Ω, starting temperature T_J=25°C;
- V_{DS}=0~400V, I_{SD}≤2A, T_J=25°C;
- V_{DS}=0~480V;
- Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
- Essentially independent of operating temperature.



TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

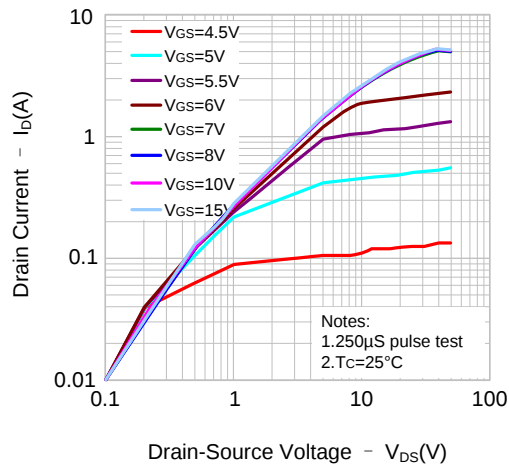


Figure 2. Transfer Characteristics

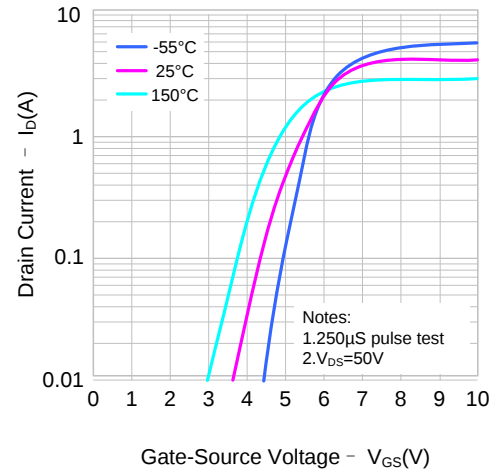


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

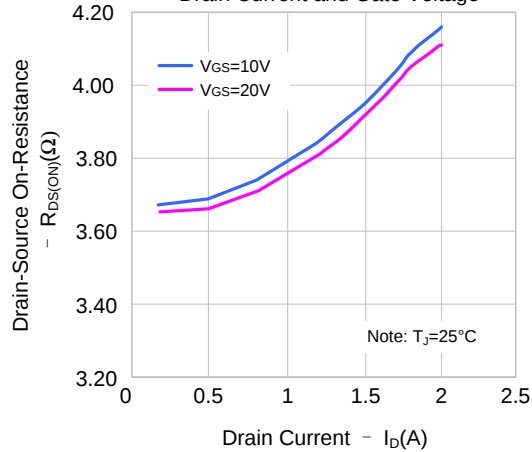
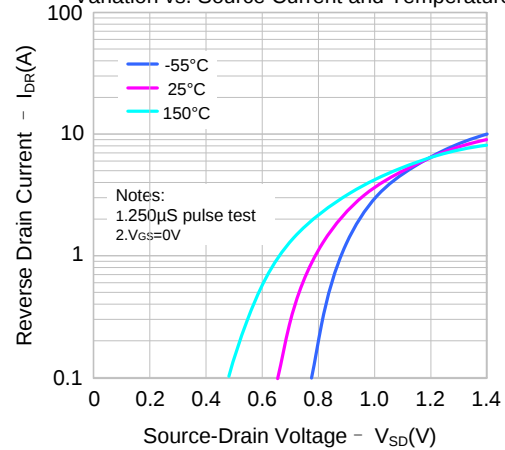


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature





TYPICAL CHARACTERISTICS (continued)

Figure 5. Capacitance Characteristics

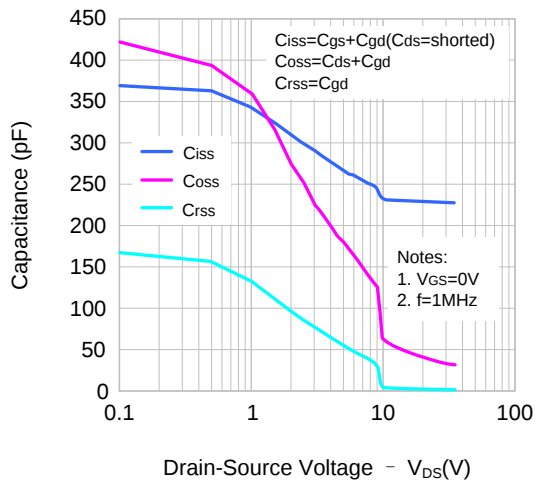


Figure 6. Gate Charge Characteristics

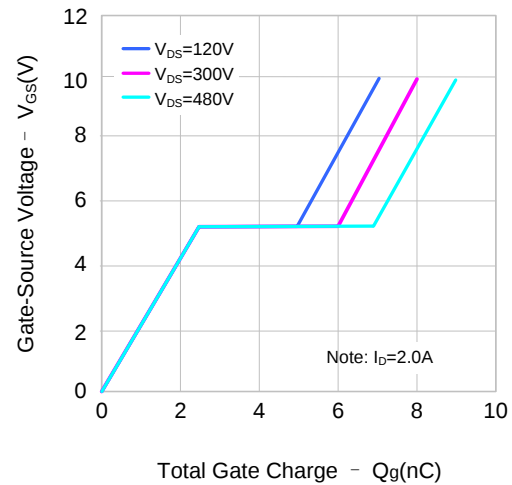


Figure 7. Breakdown Voltage Variation vs. Temperature

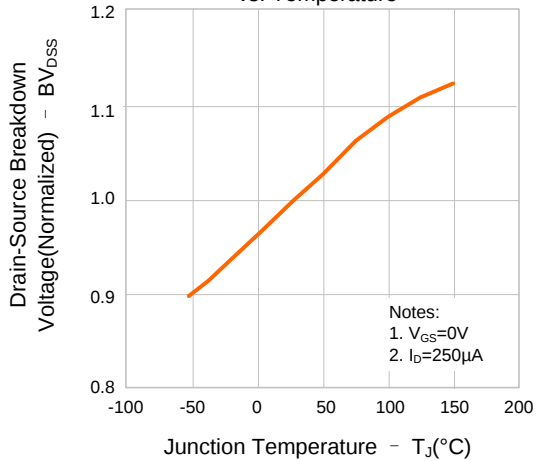


Figure 8. On-resistance Variation vs. Temperature

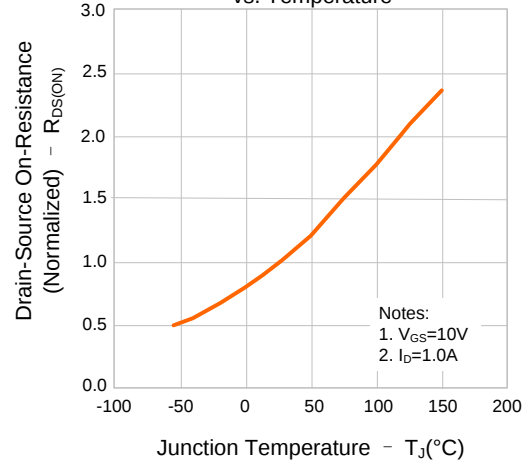


Figure 9. Max. Safe Operating Area (SVF2N60RD/M/MJ)

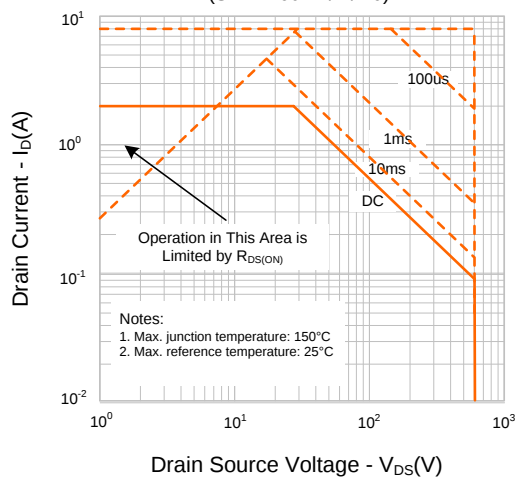
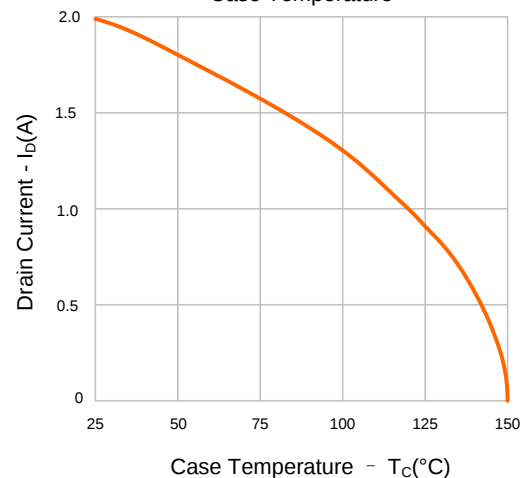
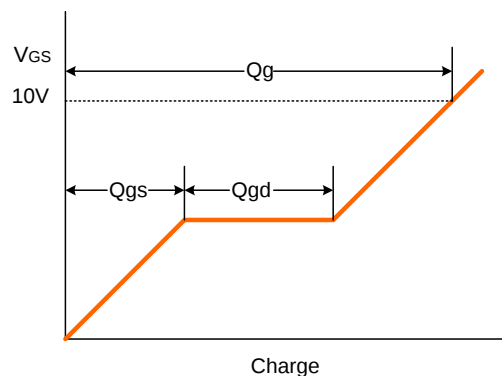
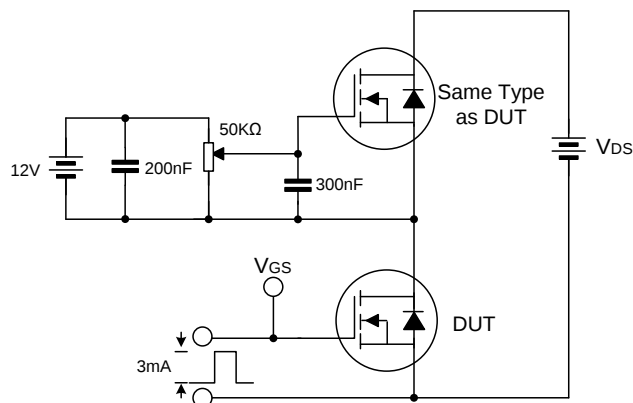


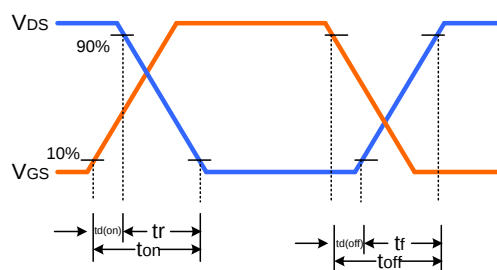
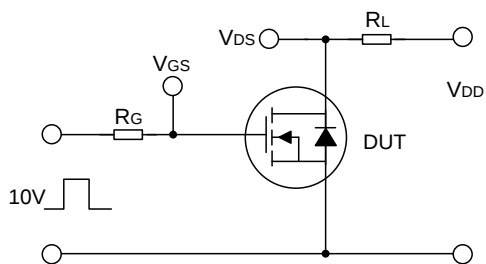
Figure 10. Maximum Drain Current vs. Case Temperature



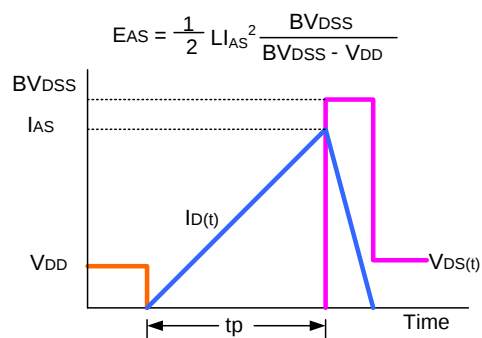
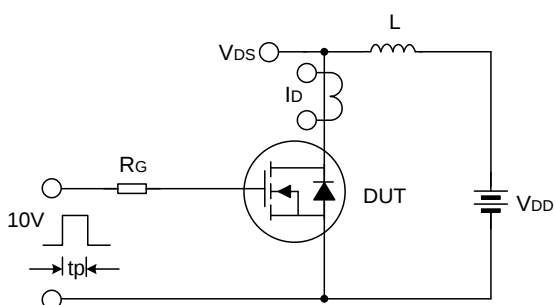
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



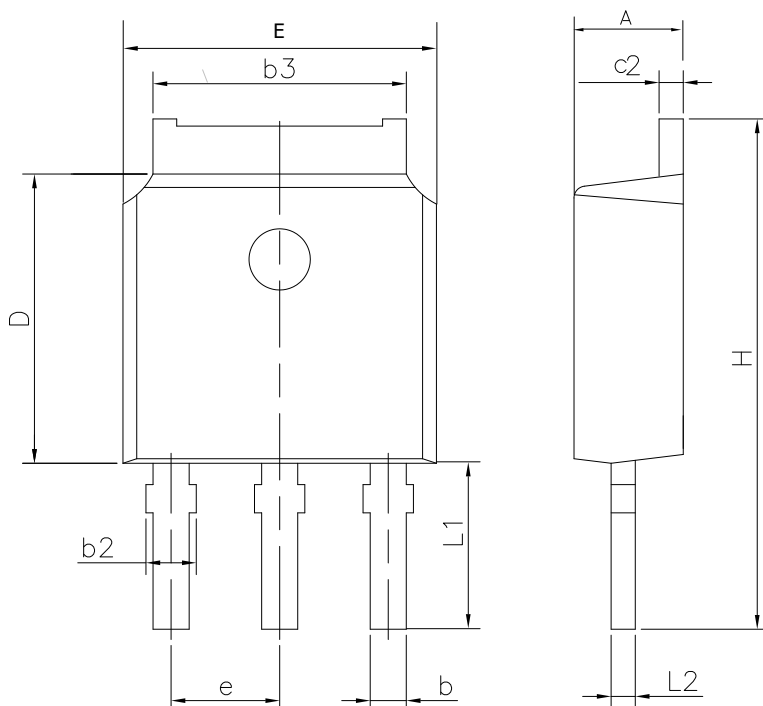
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-251D-3L

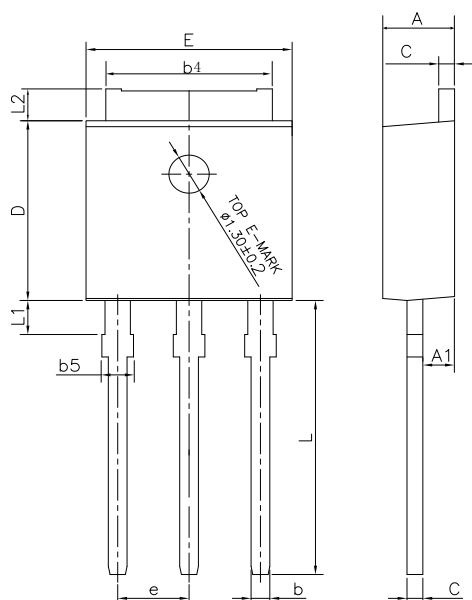
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.40
b	0.66	---	0.86
b2	0.72	---	0.90
b3	5.10	5.33	5.46
c2	0.46	---	0.60
D	6.00	6.10	6.20
E	6.50	6.60	6.70
e	2.186	2.286	2.386
H	10.40	10.70	11.00
L1	3.50 REF		
L2	0.508 BSC		

TO-251J-3L

UNIT: mm

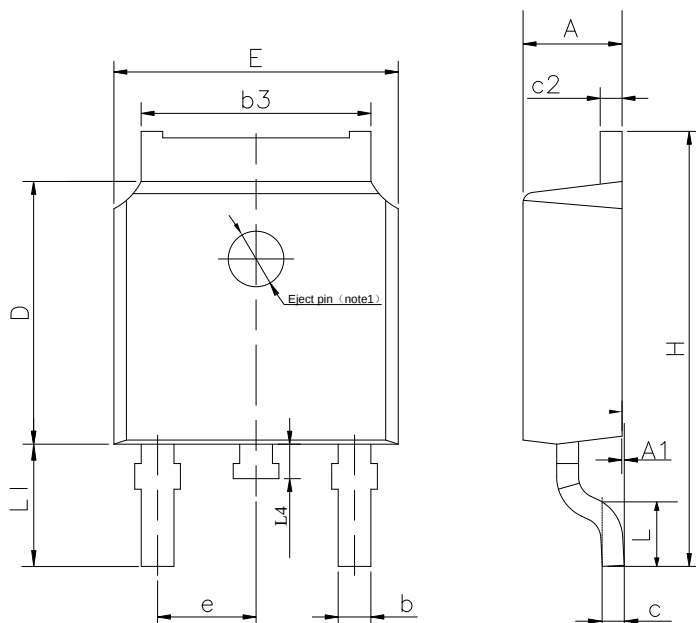


SYMBOL	MIN	NOM	MAX
A	2.18	2.30	2.39
A1	0.89	1.00	1.14
b	0.56	---	0.89
b4	4.95	5.33	5.46
b5	---	---	1.05
c	0.46	---	0.61
D	5.97	6.10	6.27
E	6.35	6.60	6.73
e	2.29 BCS		
L	8.89	9.30	9.65
L1	0.95	---	1.50
L2	0.89	---	1.27

PACKAGE OUTLINE (continued)

TO-252-2L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

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- Silan will supply the best possible product for customers!

Part No.: SVF2N60RD/M/MJ

Document Type: Datasheet

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Rev.: 1.2

Revision History:

1. Add characteristics of dv/dt, Rg
2. Update SOA

Rev.: 1.1

Revision History:

1. Modify the package outline of TO-251D-3L

Rev.: 1.0

Revision History:

1. First release