

2A, 700V N-CHANNEL MOSFET

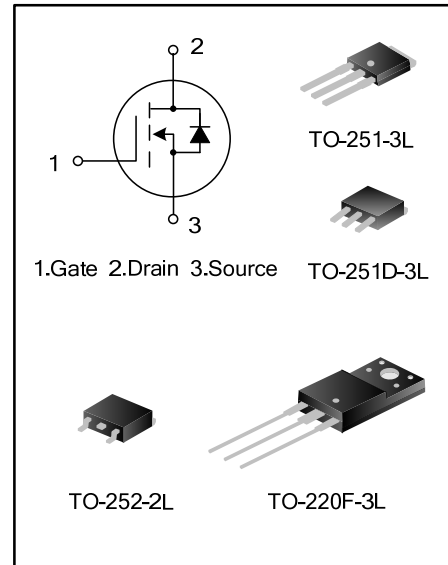
GENERAL DESCRIPTION

SVF2N70M/F/D is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

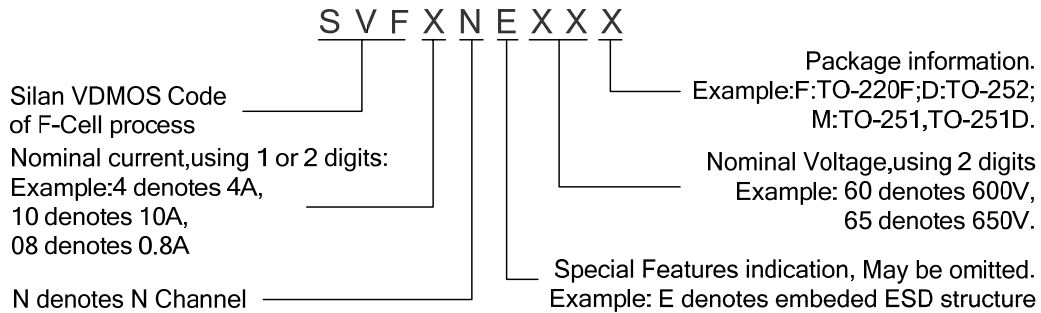
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- * 2A,700V, $R_{DS(on)(typ.)}=5.0\Omega@V_{GS}=10V$
- * Low gate charge
- * Low C_{rss}
- * Fast switching
- * Improved dv/dt capability



NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVF2N70M	TO-251-3L	SVF2N70M	Pb free	Tube
SVF2N70M	TO-251D-3L	SVF2N70M	Pb free	Tube
SVF2N70F	TO-220F-3L	SVF2N70F	Pb free	Tube
SVF2N70D	TO-252-2L	SVF2N70D	Pb free	Tube
SVF2N70DTR	TO-252-2L	SVF2N70D	Pb free	Tape & Reel

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics		Symbol	Rating		Unit
			SVF2N70M/D	SVF2N70F	
Drain-Source Voltage		V _{DS}	700		V
Gate-Source Voltage		V _{GS}	±30		V
Drain Current	T _C =25°C	I _D	2.0		A
	T _C =100°C		1.3		
Drain Current Pulsed		I _{DM}	8.0		A
Power Dissipation(T _C =25°C)		P _D	39	28	W
-Derate above 25°C			0.31	0.22	W/°C
Single Pulsed Avalanche Energy (Note 1)		E _{AS}	118		mJ
Operation Junction Temperature Range		T _J	-55~+150		°C
Storage Temperature Range		T _{stg}	-55~+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Rating		Unit
		SVF2N70M/D	SVF2N70F	
Thermal Resistance, Junction-to-Case	R _{θJC}	3.21	4.46	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	110	120	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B _{VDSS}	V _{GS} =0V, I _D =250μA	700	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =700V, V _{GS} =0V	--	--	1.0	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =1.0A	--	5.0	6.5	Ω
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	--	260.1	--	pF
Output Capacitance	C _{oss}		--	32.2	--	
Reverse Transfer Capacitance	C _{rss}		--	1.3	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =350V, I _D =2.0A, R _G =25Ω (Note 2,3)	--	8.73	--	ns
Turn-on Rise Time	t _r		--	22.27	--	
Turn-off Delay Time	t _{d(off)}		--	12.53	--	
Turn-off Fall Time	t _f		--	21.07	--	
Total Gate Charge	Q _g	V _{DS} =560V, I _D =2.0A, V _{GS} =10V (Note 2,3)	--	5.96	--	nC
Gate-Source Charge	Q _{gs}		--	1.77	--	
Gate-Drain Charge	Q _{gd}		--	2.08	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	2.0	A
Pulsed Source Current	I_{SM}		--	--	8.0	
Diode Forward Voltage	V_{SD}	$I_S=2.0A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=2.0A, V_{GS}=0V,$ $dI_F/dt=100A/\mu S$	--	190	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.53	--	μC

Notes:

1. $L=30mH, I_{AS}=2.58A, V_{DD}=95V, R_G=25\Omega$, starting $T_J=25^\circ C$;
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

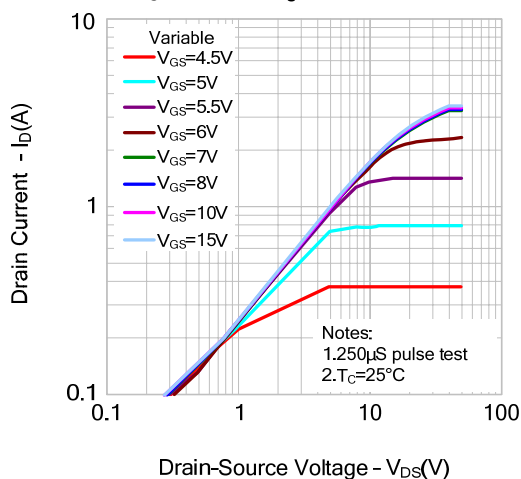


Figure 2. Transfer Characteristics

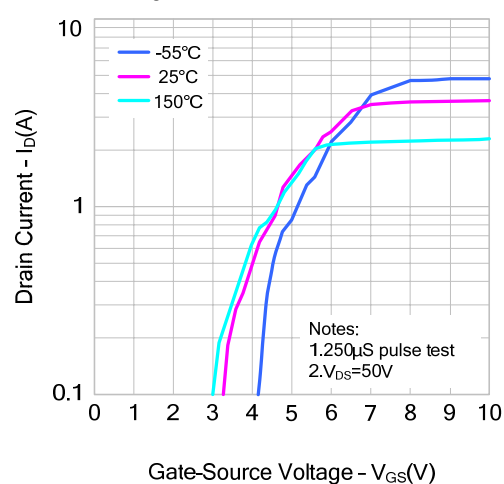


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

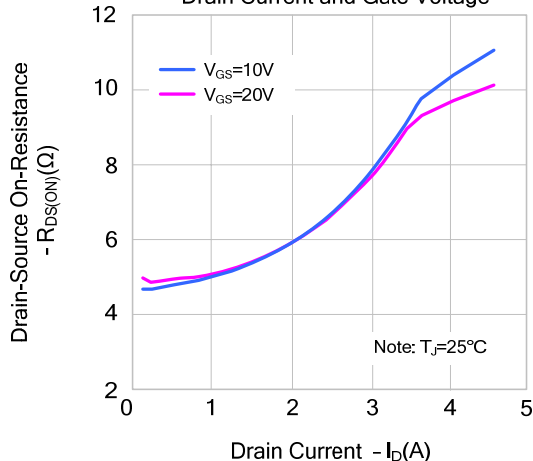


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

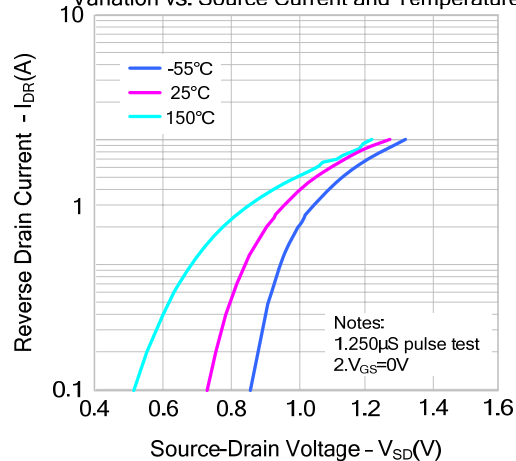


Figure 5. Capacitance Characteristics

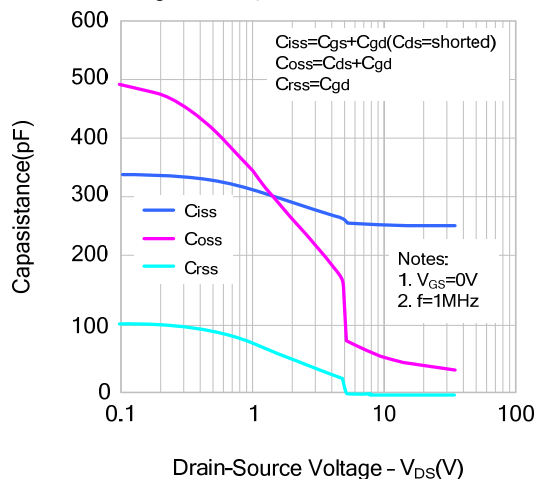
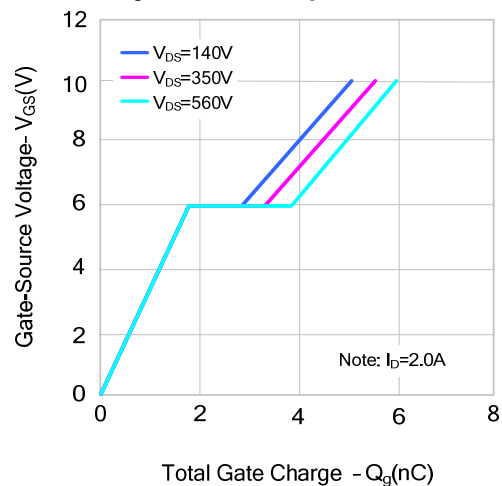


Figure 6. Gate Charge Characteristics





TYPICAL CHARACTERISTICS (continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

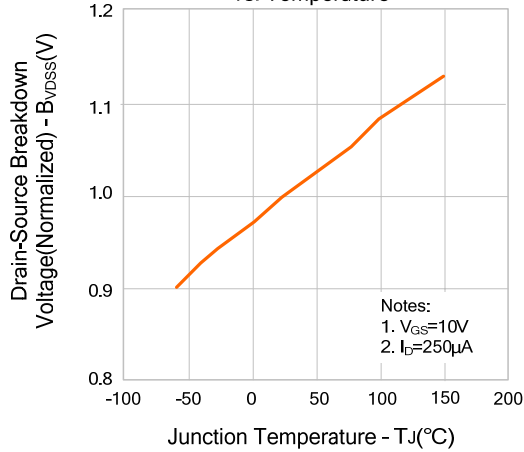


Figure 8. On-resistance Variation vs. Temperature

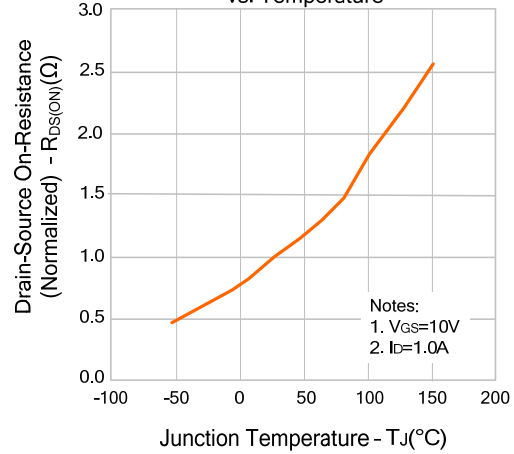


Figure 9-1. Max. Safe Operating Area(SVF2N70M/D)

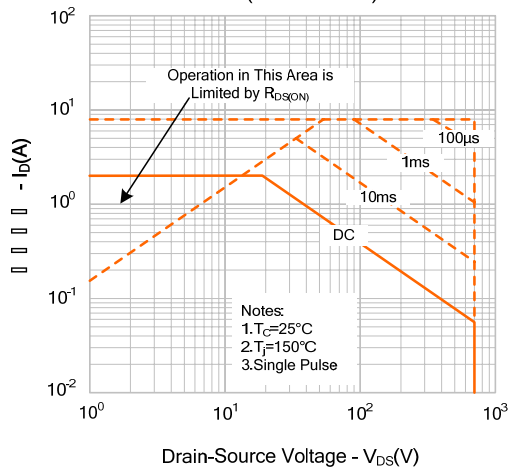


Figure 9-2. Max. Safe Operating Area(SVF2N70F)

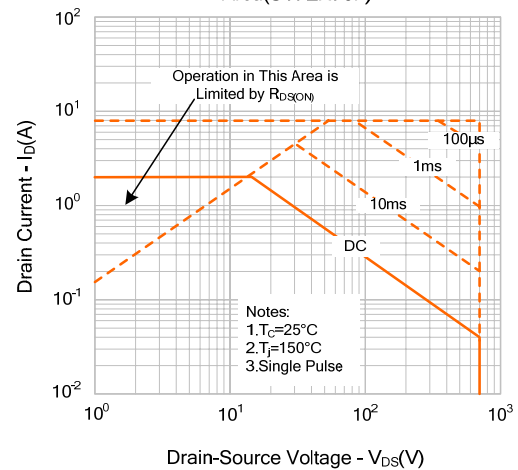
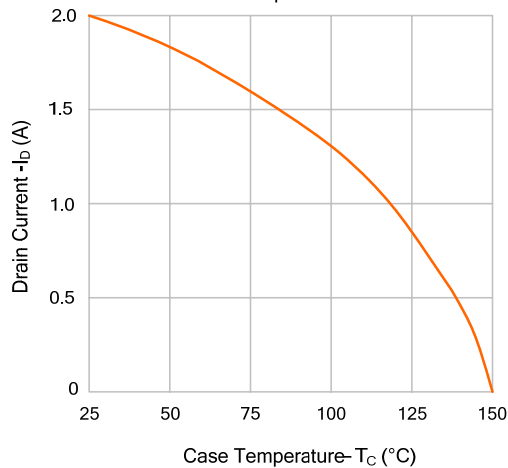
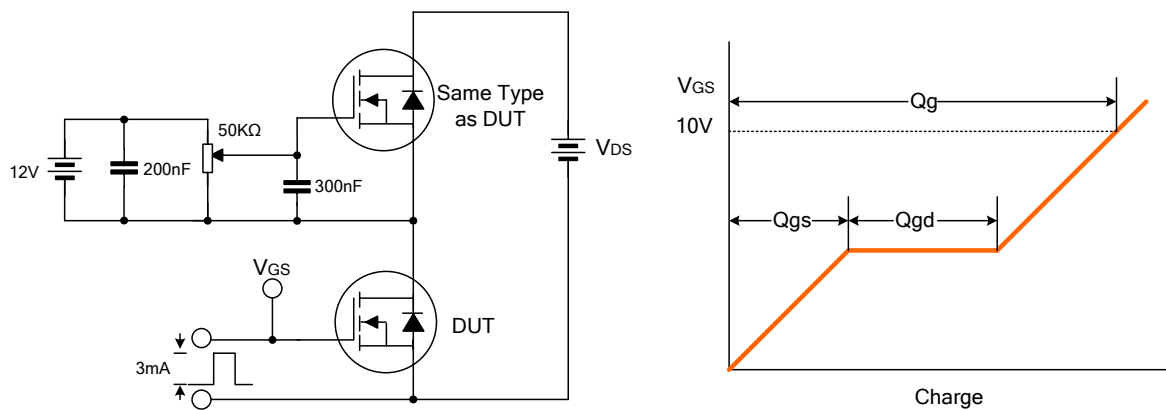


Figure 10. Max. Drain Current vs. Case Temperature

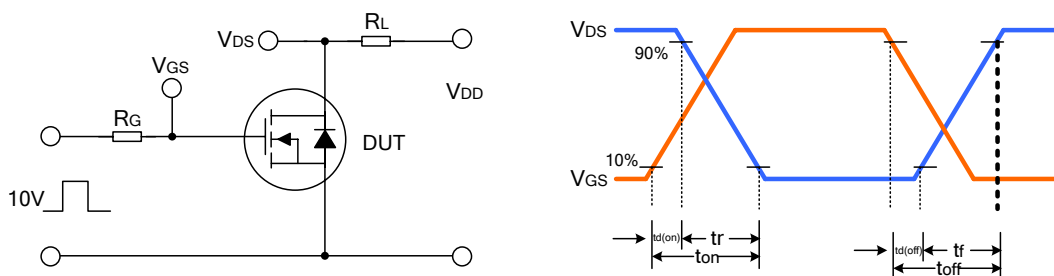


TYPICAL TEST CIRCUIT

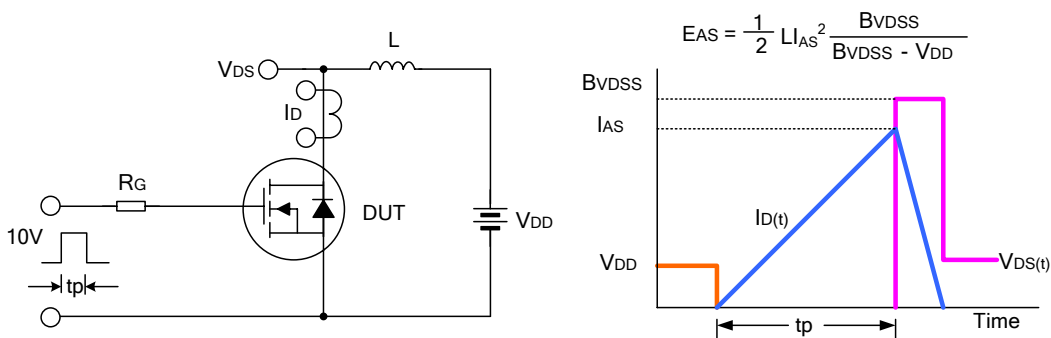
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



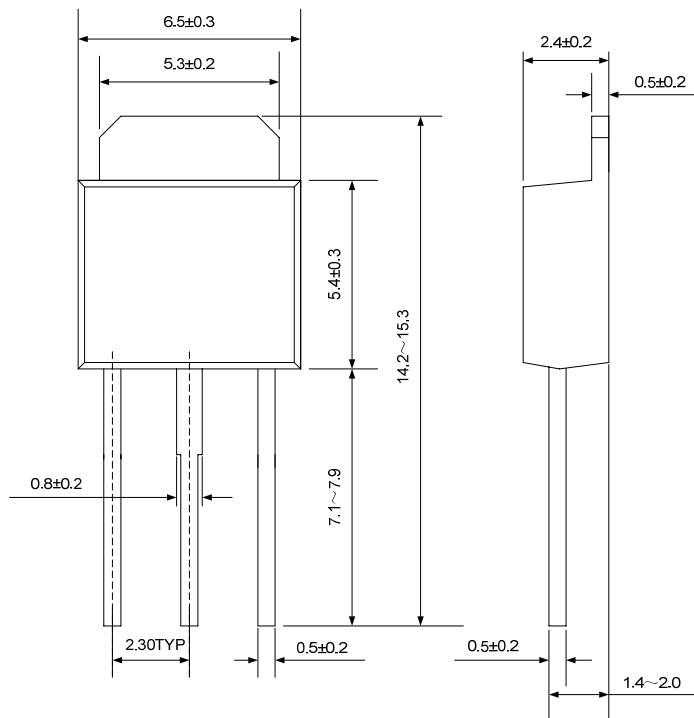
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

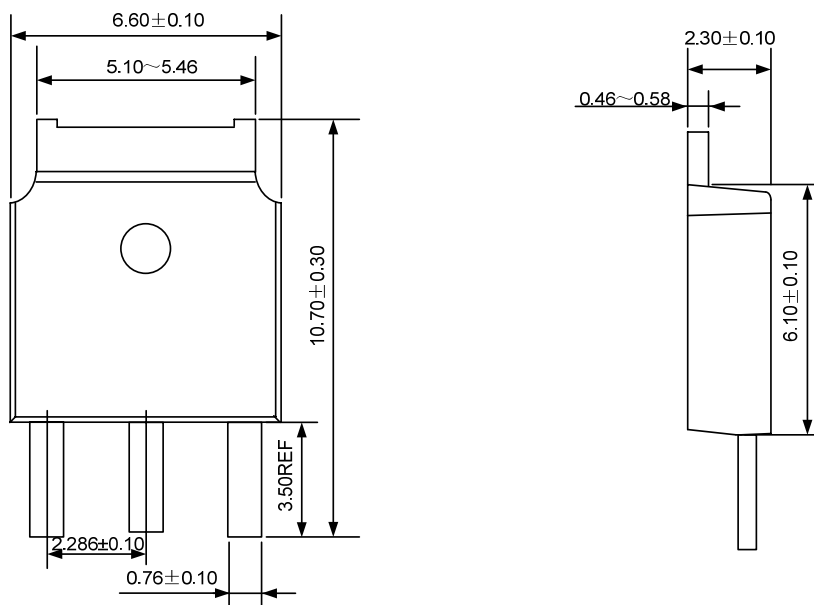
TO-251-3L

UNIT: mm



TO-251D-3L

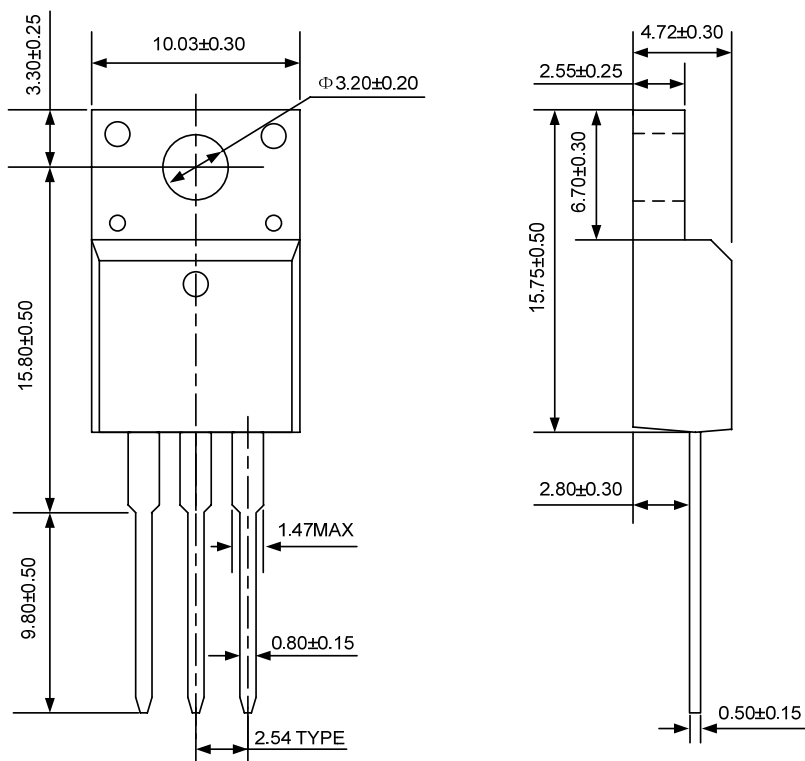
UNIT: mm



PACKAGE OUTLINE (continued)

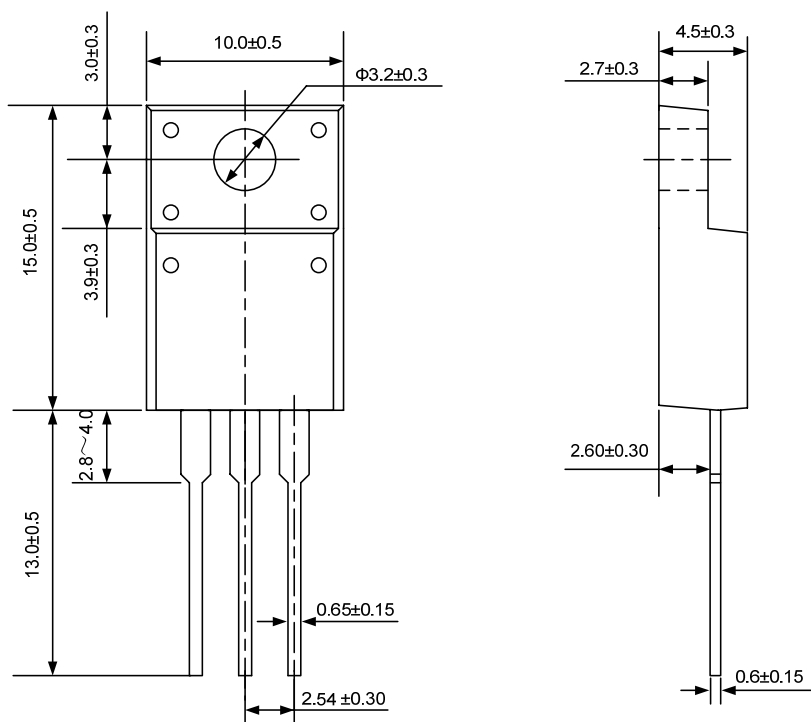
TO-220F-3L(One)

UNIT: mm



TO-220F-3L(Two)

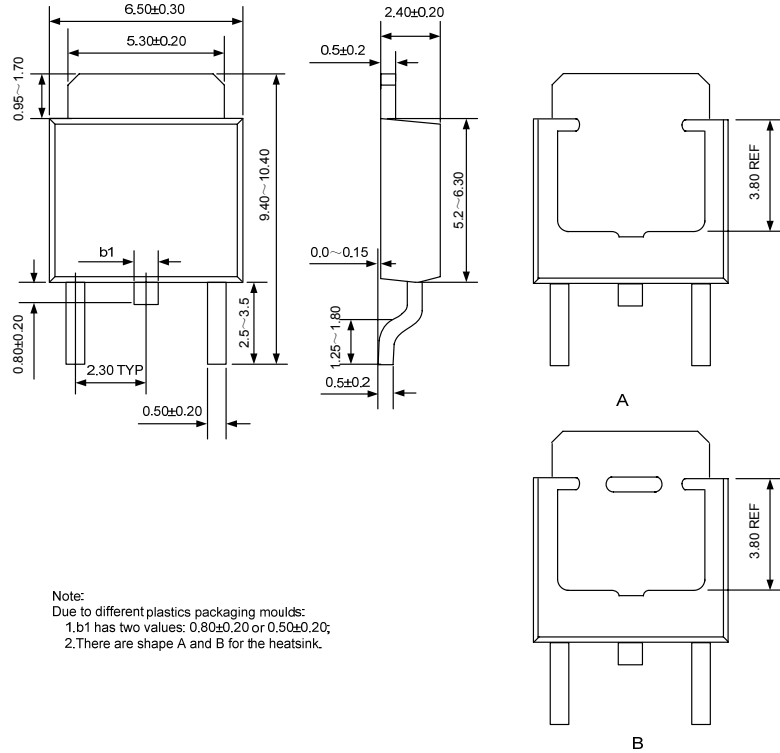
UNIT: mm



PACKAGE OUTLINE(continued)

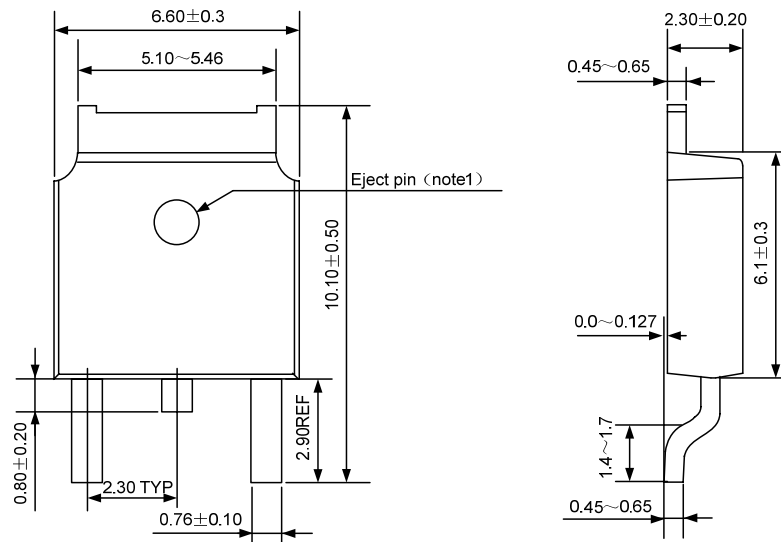
TO-252-2L(1)

UNIT: mm



TO-252-2L(2)

UNIT: mm



NOTE1 : There are two conditions for this position:has
an eject pin or has no eject pin.

Disclaimer:

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without further notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
- All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.
- Silan will supply the best possible product for customers!

ATTACHMENT**Revision History**

Date	REV	Description	Page
2011.02.18	1.0	Original	
2011.08.31	1.1	Modify "PACKAGE OUTLINE"	