

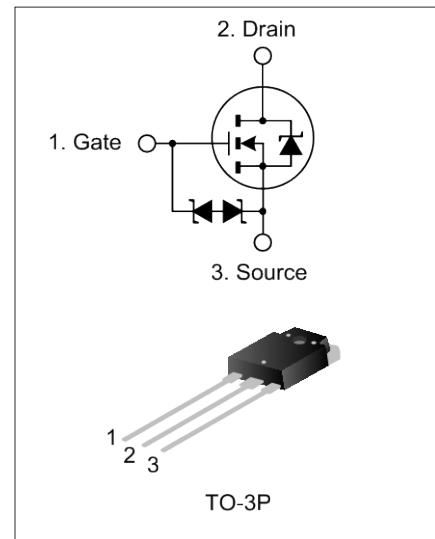
## 9A, 900V N-CHANNEL MOSFET

### DESCRIPTION

SVF3878PN is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

### FEATURES

- ◆ 9A, 900V,  $R_{DS(on)}$  (typ.)=1.0Ω@ $V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low Crss
- ◆ Fast switching
- ◆ Improved dv/dt capability



### ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVF3878PN	TO-3P	3878	Pb free	Tube

### ABSOLUTE MAXIMUM RATINGS (unless otherwise noted, $T_C=25^\circ\text{C}$ )

Characteristics	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DS}$	900	V
Gate-Source Voltage	$V_{GS}$	±30	V
Drain Current	$I_D$	$T_C=25^\circ\text{C}$	9.0
		$T_C=100^\circ\text{C}$	5.7
Drain Current Pulsed	$I_{DM}$	27.0	A
Power Dissipation ( $T_C=25^\circ\text{C}$ ) -Derate above $25^\circ\text{C}$	$P_D$	150	W
		1.2	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy (Note 1)	$E_{AS}$	966	mJ
Operation Junction Temperature Range	$T_J$	-55~+150	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-55~+150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.83	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS (unless otherwise noted, T<sub>C</sub>=25°C)**

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B <sub>VDSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	900	--	--	V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =900V, V <sub>GS</sub> =0V	--	--	100	μA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V	--	--	±10.0	μA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> =250μA	2.5	--	4.5	V
On State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =4.5A	--	1.0	1.28	Ω
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1.0MHz	--	2009	--	pF
Output Capacitance	C <sub>OSS</sub>		--	208	--	
Reverse Transfer Capacitance	C <sub>RSS</sub>		--	46.5	--	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =400V, R <sub>G</sub> =25Ω, I <sub>D</sub> =4.0A (Note2,3)	--	21.67	--	ns
Turn-on Rise Time	t <sub>r</sub>		--	27.60	--	
Turn-off Delay Time	t <sub>d(off)</sub>		--	83.73	--	
Turn-off Fall Time	t <sub>f</sub>		--	29.73	--	
Total Gate Charge	Q <sub>g</sub>	V <sub>DD</sub> =450V, V <sub>GS</sub> =10V, I <sub>D</sub> =9.0A (Note 2,3)	--	67.8	--	nC
Gate-Source Charge	Q <sub>gs</sub>		--	10.1	--	
Gate-Drain Charge	Q <sub>gd</sub>		--	38.6	--	

**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS**

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Source Current	I <sub>S</sub>	Integral Reverse P-N Junction Diode in the MOSFET	--	--	9.0	A
Pulsed Source Current	I <sub>SM</sub>		--	--	27.0	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =9.0A, V <sub>GS</sub> =0V	--	--	1.4	V
Reverse Recovery Time	T <sub>rr</sub>	I <sub>S</sub> =9.0A, V <sub>GS</sub> =0V, dI <sub>F</sub> /dt=100A/μS (Note2)	--	715	--	ns
Reverse Recovery Charge	Q <sub>rr</sub>		--	6.47	--	μC

**Notes:**

- L=30mH, I<sub>AS</sub>=7.70A, V<sub>DD</sub>=100V, R<sub>G</sub>=25Ω, starting T<sub>J</sub>=25°C;
- Pulse Test: Pulse width ≤300μs, Duty cycles ≤2%;
- Essentially independent of operating temperature.

**TYPICAL CHARACTERISTICS**

Figure 1. On-Region Characteristics

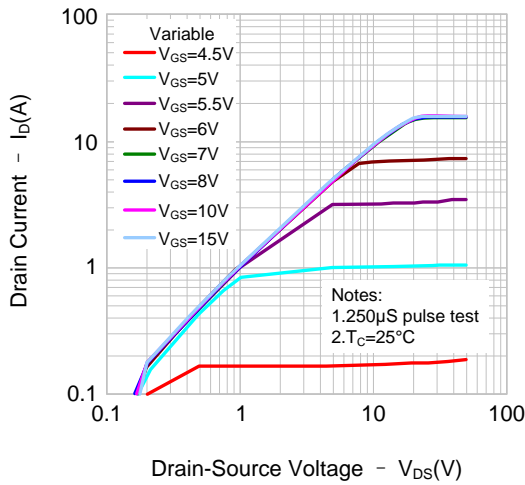


Figure 2. Transfer Characteristics

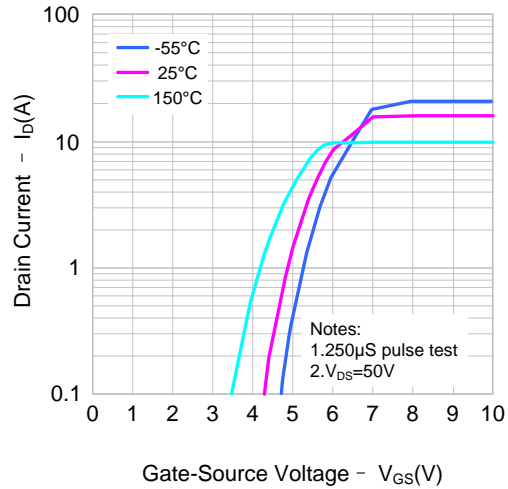


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

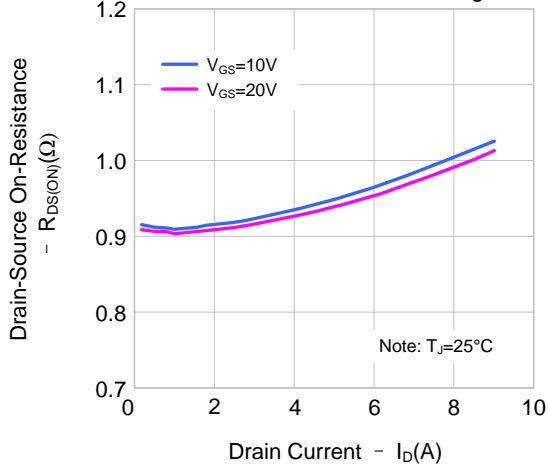


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

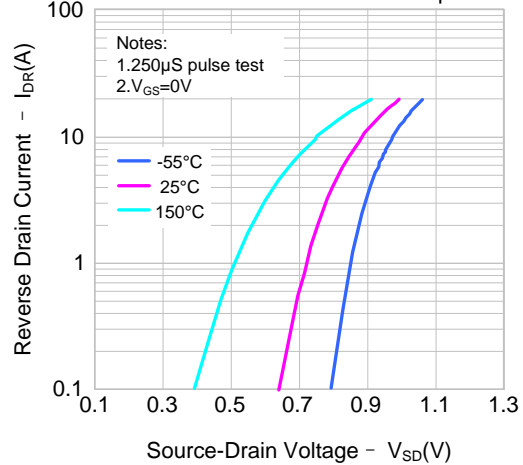


Figure 5. Capacitance Characteristics

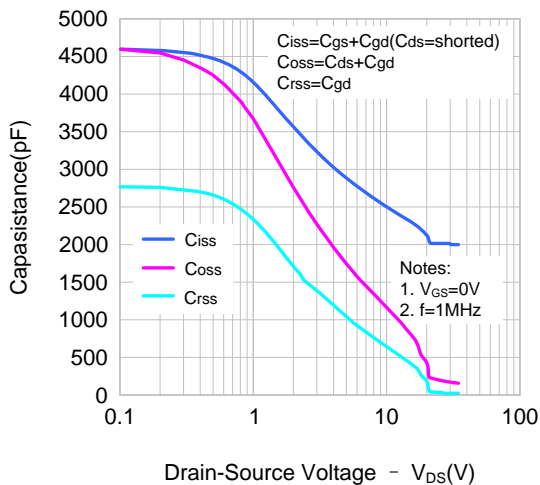
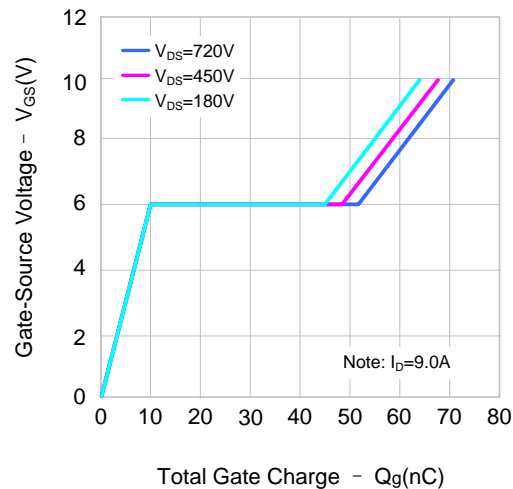


Figure 6. Gate Charge Characteristics



**TYPICAL CHARACTERISTICS(CONTINUED)**

Figure 7. Breakdown Voltage Variation vs. Temperature

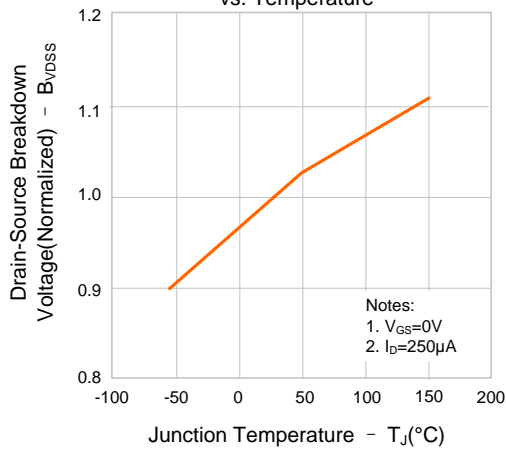


Figure 8. On-resistance Variation vs. Temperature

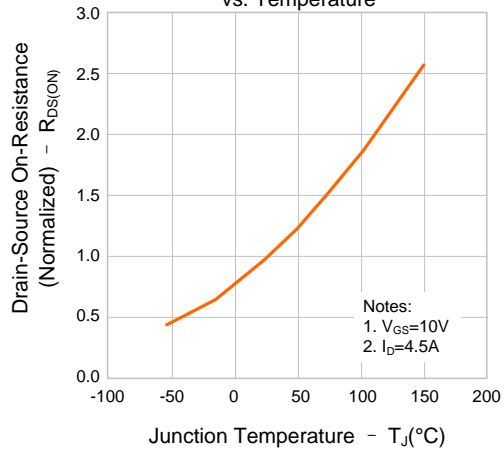


Figure 9. Max. Safe Operating Area

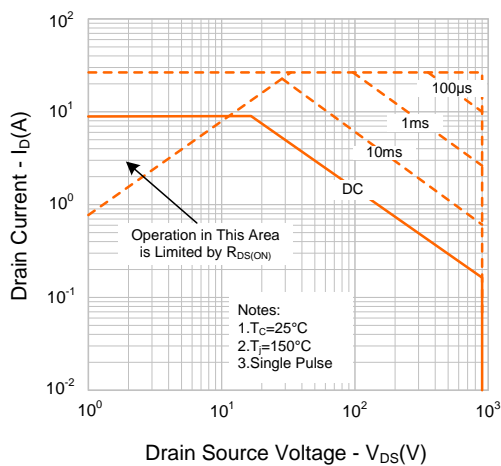
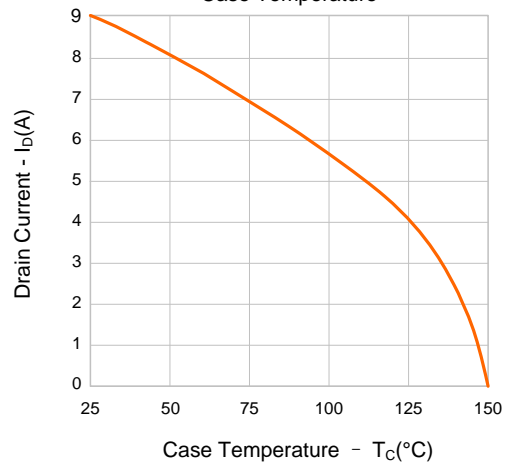
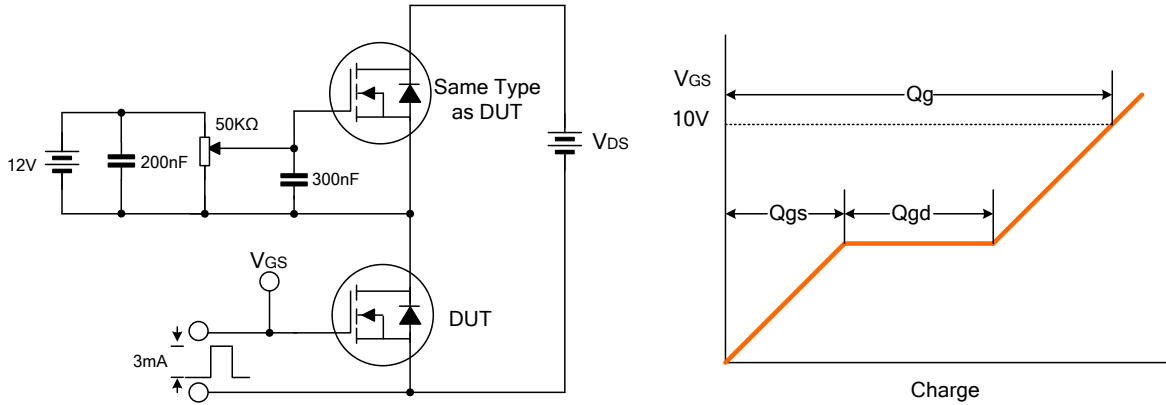


Figure 10. Maximum Drain Current vs. Case Temperature

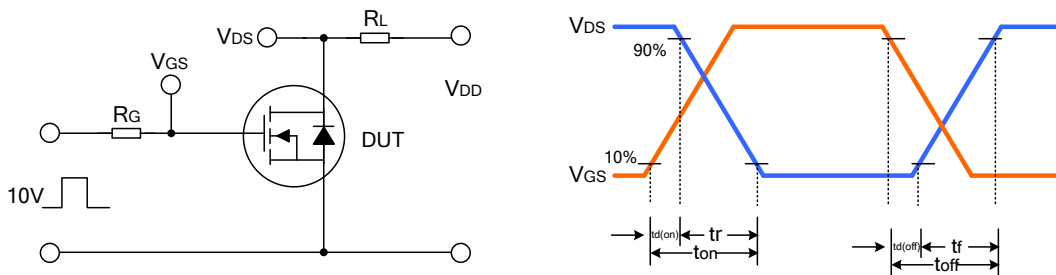


**TYPICAL TEST CIRCUIT**

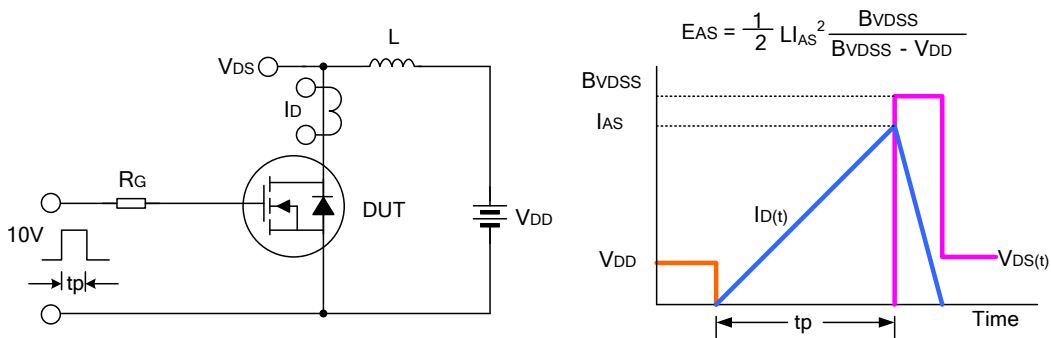
Gate Charge Test Circuit & Waveform



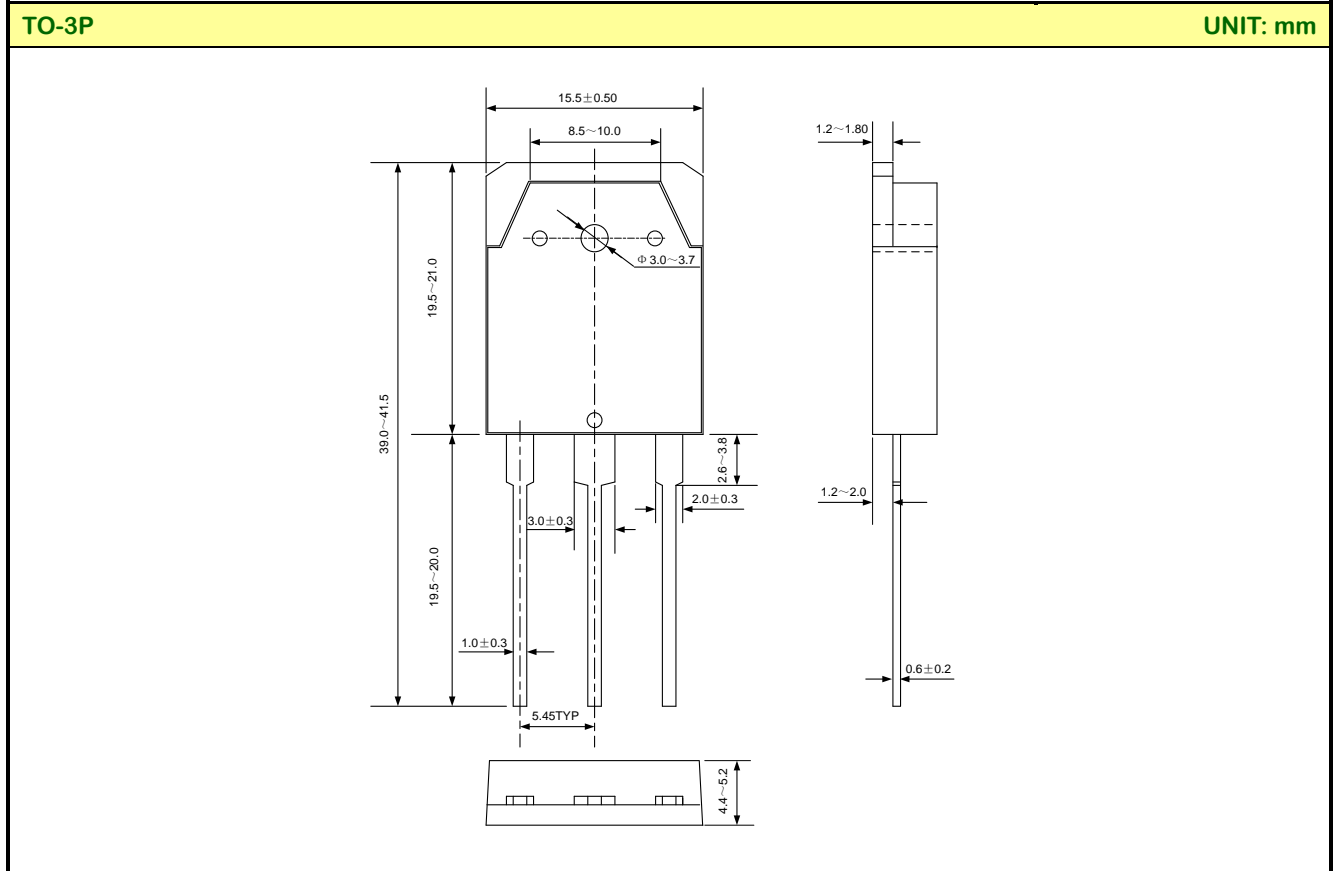
Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform



**PACKAGE OUTLINE**



**Disclaimer :**

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without further notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
- All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.
- Silan will supply the best possible product for customers!

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Rev.:	1.0	Author:	Yin Zi
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Revision History:

1. First release
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