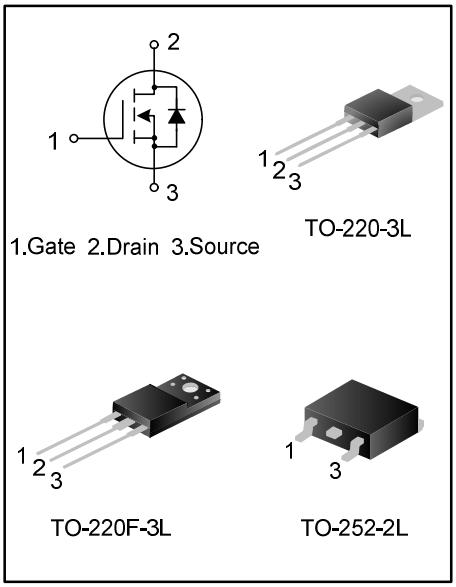
5A, 600V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF5N60CF/D/T is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

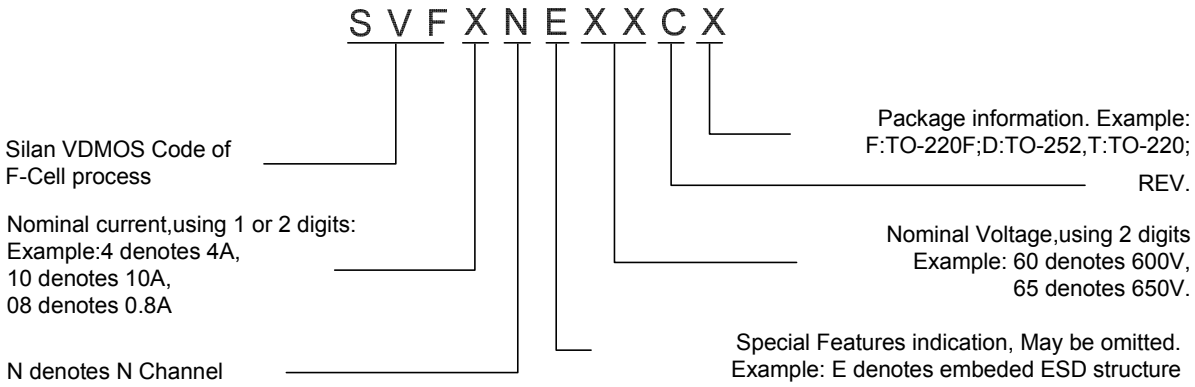
This device is widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 5A, 600V, $R_{DS(on)(typ)}$=1.8Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVF5N60CF	TO-220F-3L	SVF5N60CF	Halogen free	Tube
SVF5N60CD	TO-252-2L	5N60CD	Halogen free	Tube
SVF5N60CDTR	TO-252-2L	5N60CD	Halogen free	Tape&Reel
SVF5N60CT	TO-220-3L	SVF5N60CT	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics		Symbol	Ratings			Unit
			SVF5N60CF	SVF5N60CD	SVF5N60CT	
Drain-Source Voltage		V_{DS}	600			V
Gate-Source Voltage		V_{GS}	±30			V
Drain Current	T_C=25°C	I_D	5.0			A
	T_C=100°C		3.1			
Drain Current Pulsed		I_{DM}	20			A
Power Dissipation(T_C=25°C)		P_D	31	90	102	W
Derate above 25°C			0.32	0.72	0.68	W/°C
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	247			mJ
Operation Junction Temperature Range		T_J	-55～+150			°C
Storage Temperature Range		T_{stg}	-55～+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings			Unit
		SVF5N60CF	SVF5N60CD	SVF5N60CT	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	4.03	1.39	1.47	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.0	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min	Typ	Max	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	600	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=600V,V_{GS}=0V	--	--	1	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V,V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS},I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=2.5A	--	1.8	2.15	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V,f=1.0MHz	--	463	--	pF
Output Capacitance	C_{oss}		--	58	--	
Reverse Transfer Capacitance	C_{rss}		--	5.0	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=300V,I_D=5.0A,R_G=24Ω （Note2, 3）	--	12.73	--	ns
Turn-on Rise Time	t_r		--	30.60	--	
Turn-off Delay Time	$t_{d(off)}$		--	41.93	--	
Turn-off Fall Time	t_f		--	32.53	--	
Total Gate Charge	Q_g	V_{DS}=480V，I_D=5.0A，V_{GS}=10V （Note2, 3）	--	13.43	--	nC
Gate-Source Charge	Q_{gs}		--	2.85	--	
Gate-Drain Charge	Q_{gd}		--	6.67	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min	Typ	Max	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	5	A
Pulsed Source Current	I_{SM}		--	--	20	
Diode Forward Voltage	V_{SD}	I_S=5.0A, V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=5.0A, V_{GS}=0V, dI_F/dt=100A/μS	--	450	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.2	--	μC

Notes:

1. L=30mH, I_{AS}=3.8A, V_{GS}=100V, R_G=25Ω, starting TB_{JB}=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

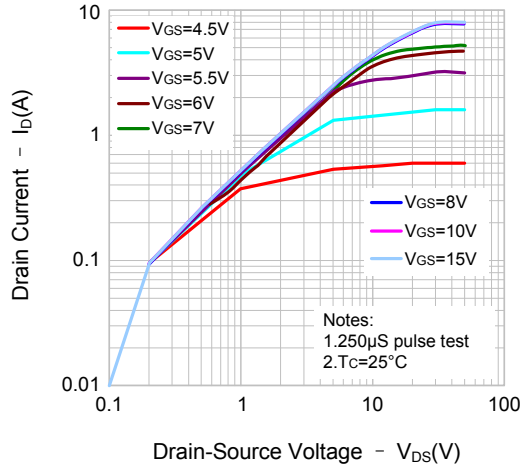


Figure 2. Transfer Characteristics

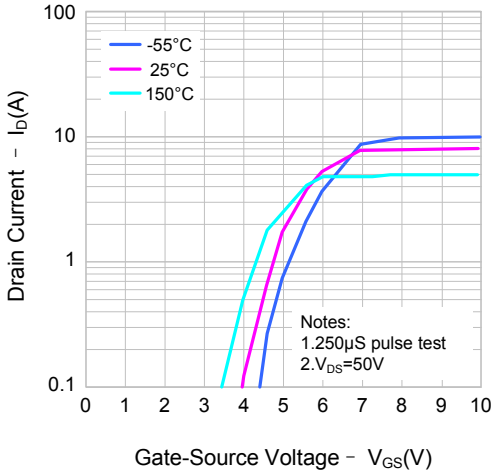


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

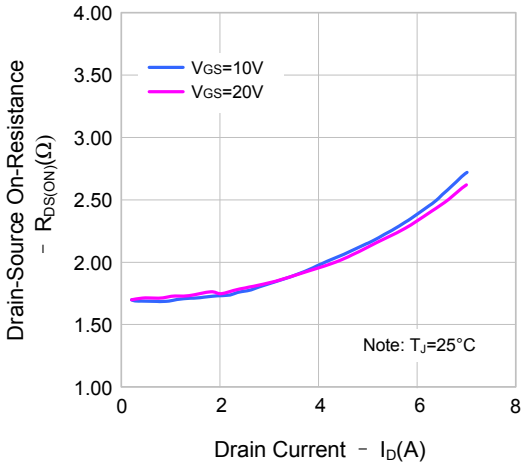


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

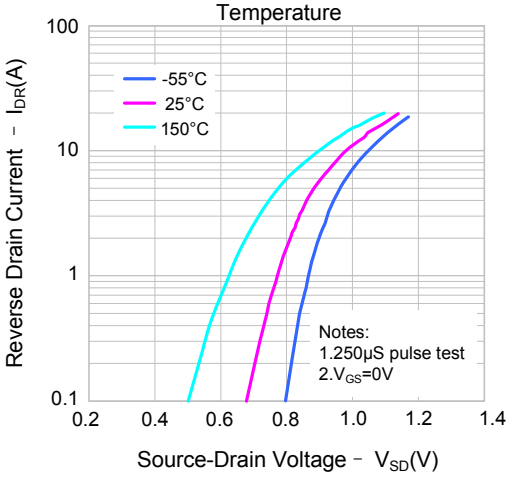


Figure 5. Capacitance Characteristics

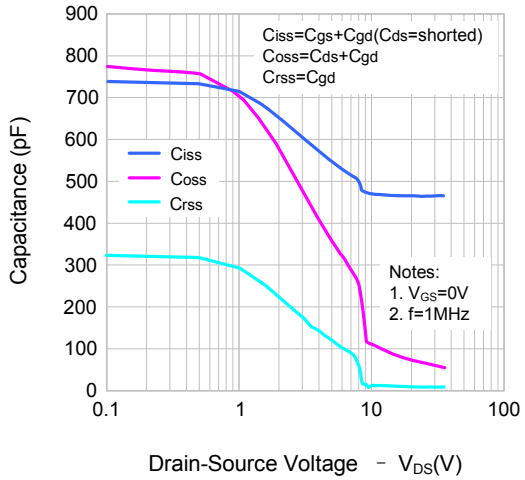
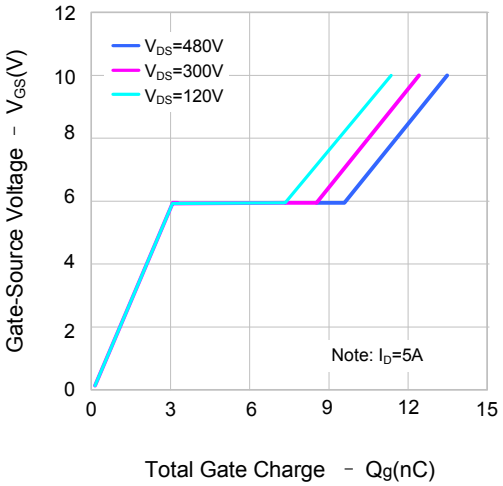


Figure 6. Gate Charge Characteristic



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

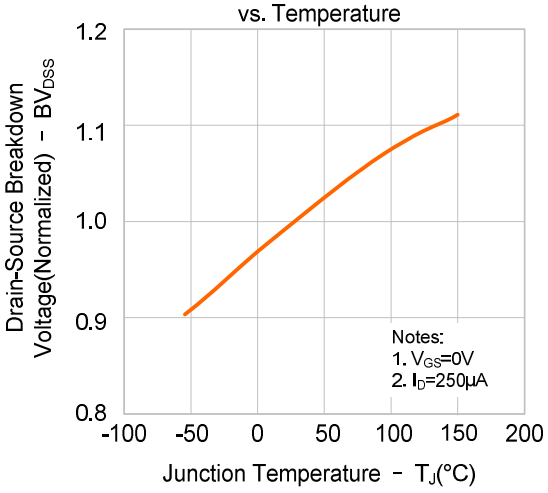


Figure 8. On-resistance Variation vs. Temperature

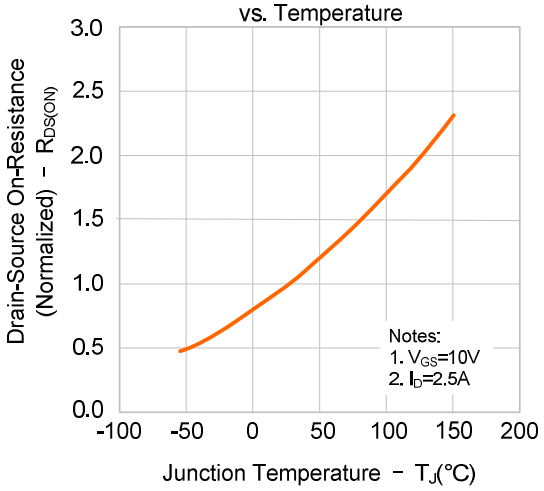


Figure 9-1. Max. Safe Operating Area (SVF5N60CF)

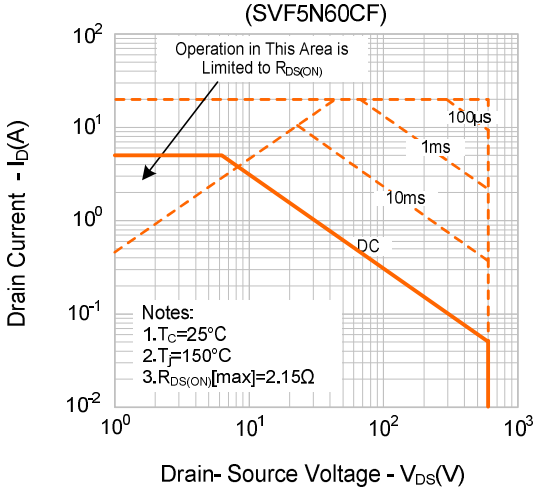


Figure 9-2. Max. Safe Operating Area (SVF5N60CD)

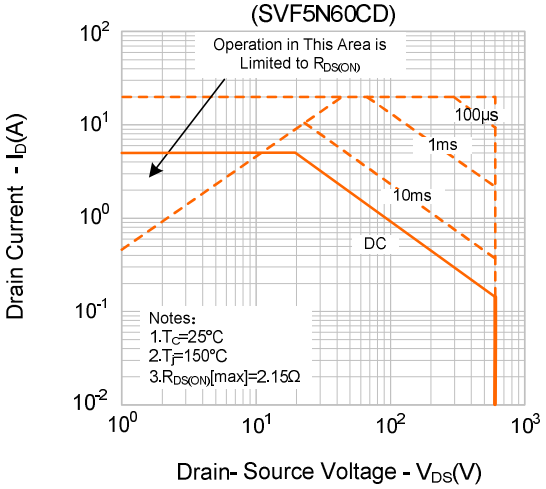


Figure 9-3. Max. Safe Operating Area (SVF5N60CT)

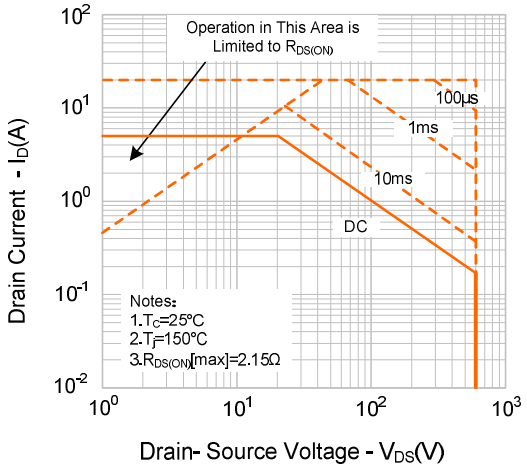
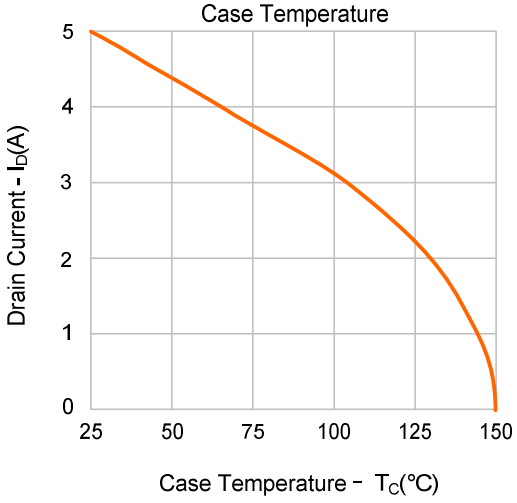
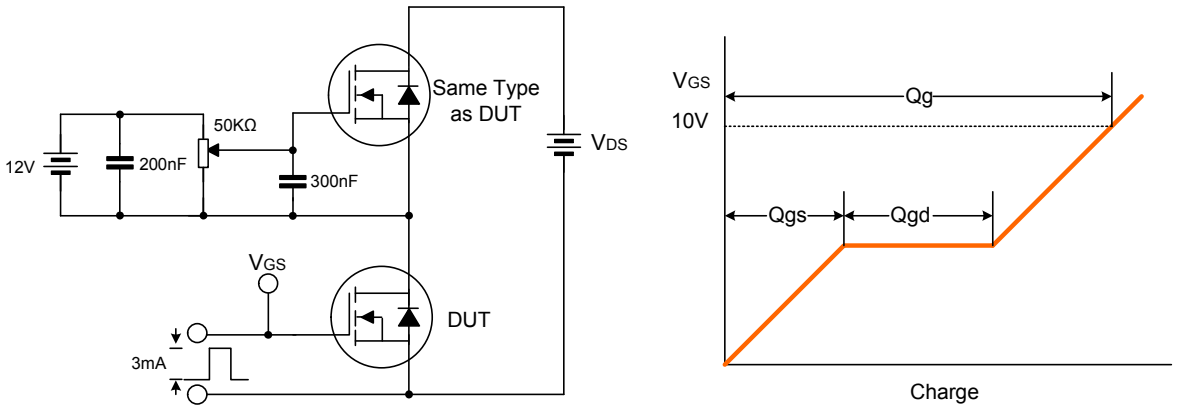


Figure 10. Maximum Drain Current vs. Case Temperature

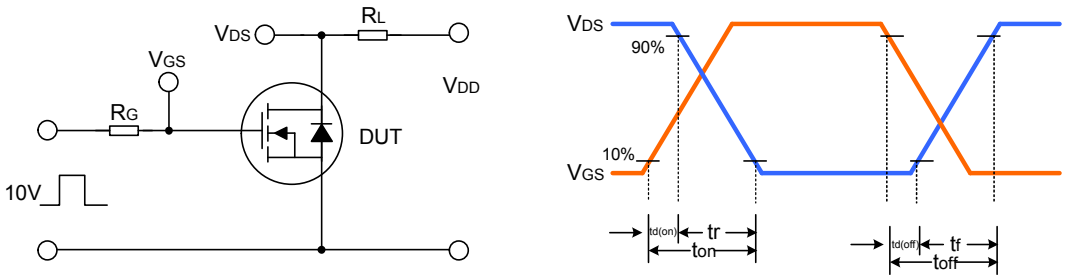


TYPICAL TEST CIRCUIT

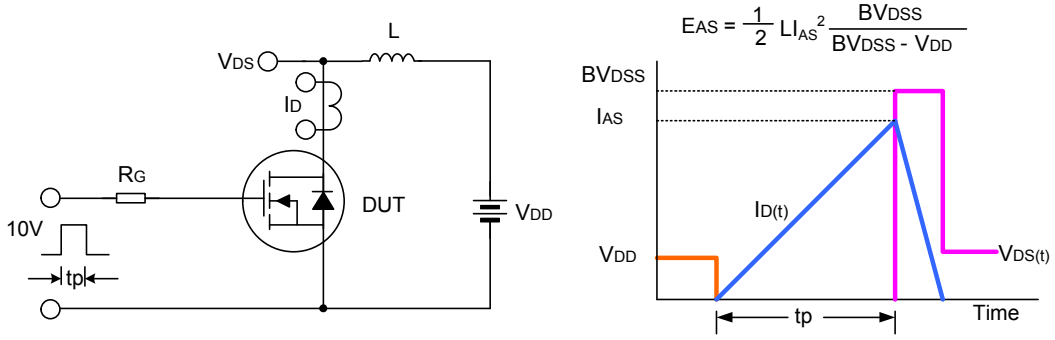
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



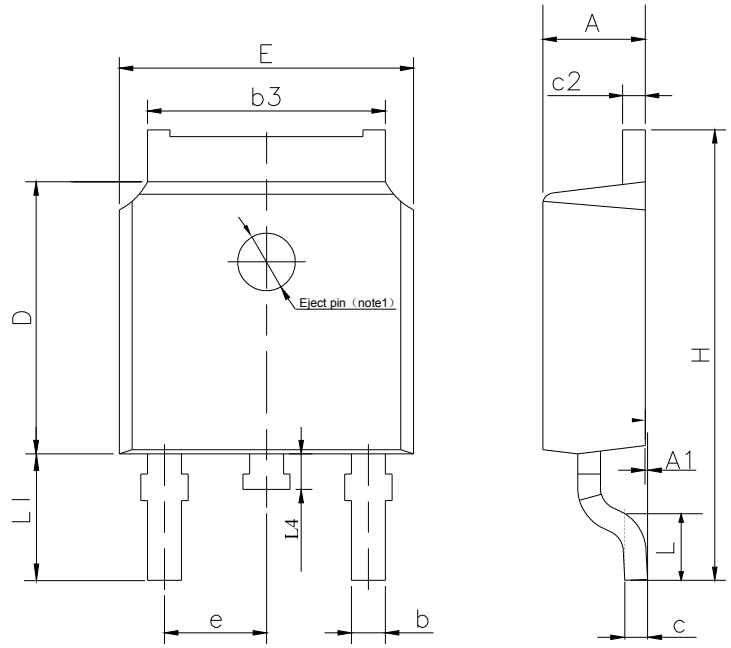
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-252-2L

UNIT: mm

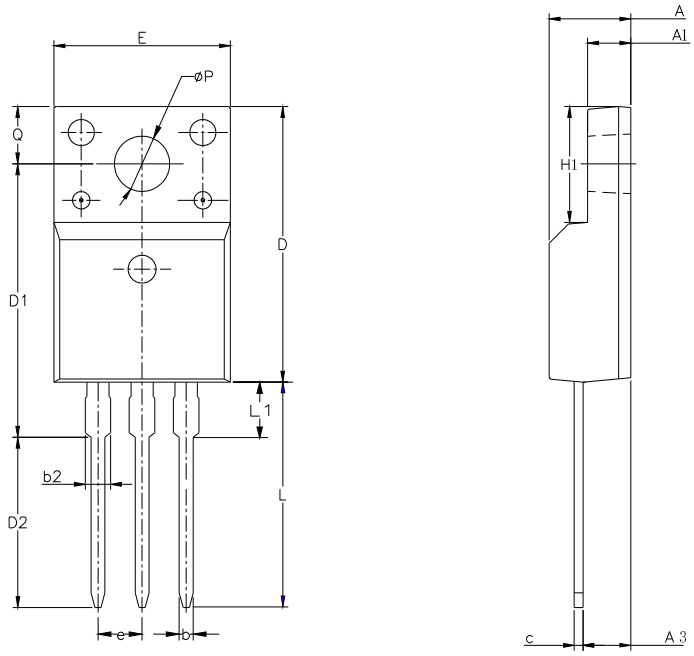


SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e		2.30TYP	
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1		2.90REF	
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

TO-220F-3L

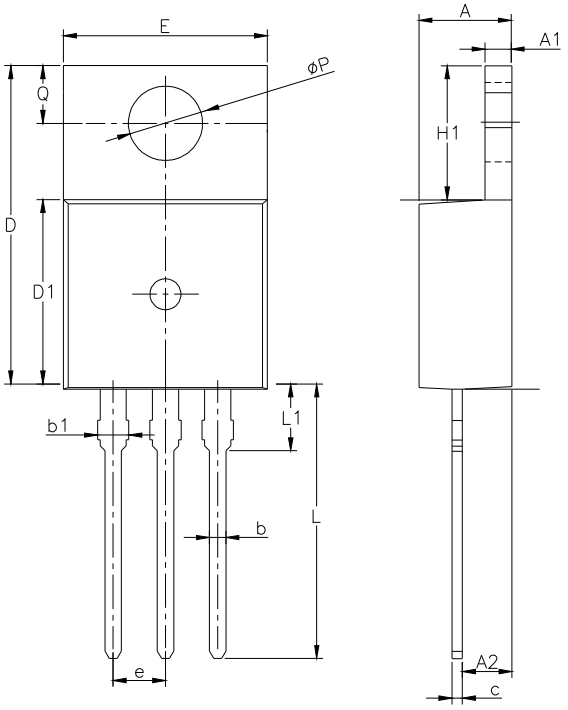
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e		2.54BCS	
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
øP	3.00	3.18	3.40
Q	3.05	3.30	3.55

PACKAGE OUTLINE(CONTINUED)

TO-220-3L **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ΦP	3.40	3.70	3.90
Q	2.60	—	3.20

Disclaimer :

- **Silan reserves the right to make changes to the information herein for the improvement of the design and performance without prior notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.**
- **All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.**
- **Silan will supply the best possible product for customers!**

Part No.:	SVF5N60CF/D/T	Document Type:	Datasheet
Copyright:	HANGZHOU SILAN MICROELECTRONICS CO.,LTD	Website:	http: //www.silan.com.cn

Rev.: 1.5

Revision History:

1. Delete package outline of TO-220F-3L(2)
2. Modify I_{DSS} from 10μA to 1μA

Rev.: 1.4

Revision History:

1. Add package outline of TO-220-3L

Rev.: 1.3

Revision History:

1. Add information of TO-252-2L package

Rev.: 1.2

Revision History:

1. Modify the figure 6

Rev.: 1.1

Revision History:

1. Modify the package information of TO-220F-3L

Rev.: 1.0

Revision History:

1. First release