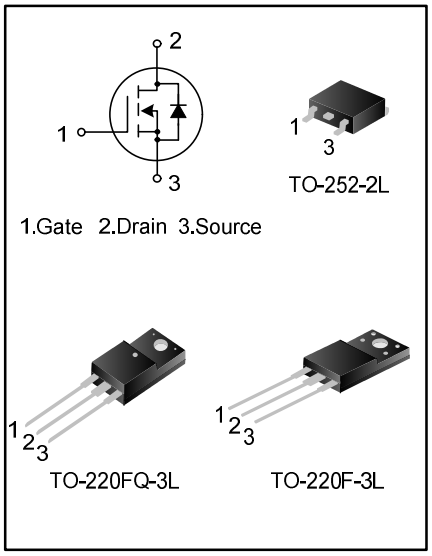
# 6A, 600V N-CHANNEL MOSFET

## GENERAL DESCRIPTION

SVF6N60F/D/FQ is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

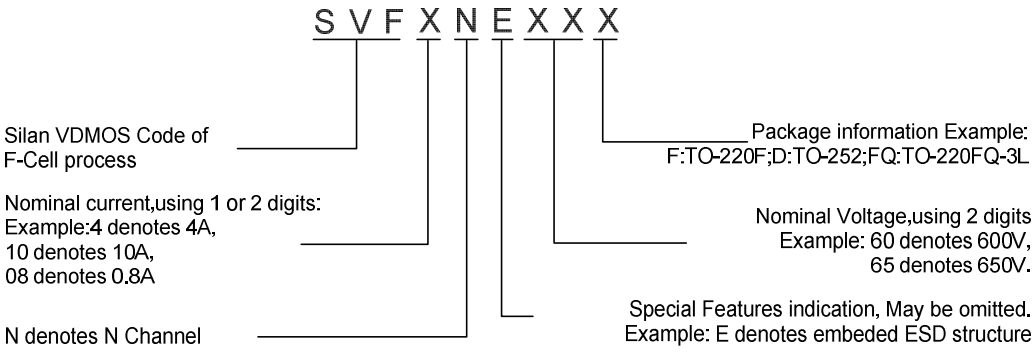
These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.




## FEATURES

- 6A,600V,$R_{DS(on(typ.)}$=1.35Ω@$V_{GS}$=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

## NOMENCLATURE




## ORDERING INFORMATION

| Part No. | Package | Marking | Hazardous substance control | Packing |
|---|---|---|---|---|
| SVF6N60F | TO-220F-3L | SVF6N60F | Pb free | Tube |
| SVF6N60DTR | TO-252-2L | SVF6N60D | Halogen free | Tape & Reel |
| SVF6N60FQ | TO-220FQ-3L | SVF6N60FQ | Pb free | Tube |

## ABSOLUTE MAXIMUM RATINGS ($T_C$=25°C unless otherwise noted)

| Characteristics | | Symbol | Ratings | | Unit |
|---|---|---|---|---|---|
| | | | SVF6N60F/FQ | SVF6N60D | |
| Drain-Source Voltage | | $V_{DS}$ | 600 | | V |
| Gate-Source Voltage | | $V_{GS}$ | ±30 | | V |
| Drain Current | $T_C$=25°C | $I_D$ | 6 | | A |
| | $T_C$=100°C | | 3.8 | | |
| Drain Current Pulsed | | $I_{DM}$ | 24 | | A |
| Power Dissipation($T_C$=25°C) | | $P_D$ | 42 | 125 | W |
| -Derate above 25°C | | | 0.34 | 1.00 | W/°C |
| Single Pulsed Avalanche Energy(Note 1) | | $E_{AS}$ | 343 | | mJ |
| Operation Junction Temperature Range | | $T_J$ | -55～+150 | | °C |
| Storage Temperature Range | | $T_{stg}$ | -55～+150 | | °C |

## THERMAL CHARACTERISTICS

| Characteristics | Symbol | Ratings | | Unit |
|---|---|---|---|---|
| | | SVF6N60F/FQ | SVF6N60D | |
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 2.98 | 1.00 | °C/W |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 62.5 | 62.0 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_C$=25°C unless otherwise noted)

| Characteristics | Symbol | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Drain -Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V, $I_D$=250μA | 600 | -- | -- | V |
| Drain-Source Leakage Current | $I_{DSS}$ | $V_{DS}$=600V, $V_{GS}$=0V | -- | -- | 1.0 | μA |
| Gate-Source Leakage Current | $I_{GSS}$ | $V_{GS}$=±30V, $V_{DS}$=0V | -- | -- | ±100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS}$= $V_{DS}$, $I_D$=250μA | 2.0 | -- | 4.0 | V |
| Static Drain- Source On State Resistance | $R_{DS(on)}$ | $V_{GS}$=10V, $I_D$=3A | -- | 1.35 | 1.5 | Ω |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=25V, $V_{GS}$=0V, f=1.0MHz | -- | 690.7 | -- | pF |
| Output Capacitance | $C_{oss}$ | | -- | 83.6 | -- | |
| Reverse Transfer Capacitance | $C_{rss}$ | | -- | 2.7 | -- | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$=300V, $I_D$=6A, $R_G$=25Ω, (Note2,3) | -- | 18.53 | -- | ns |
| Turn-on Rise Time | $t_r$ | | -- | 42.67 | -- | |
| Turn-off Delay Time | $t_{d(off)}$ | | -- | 33.20 | -- | |
| Turn-off Fall Time | $t_f$ | | -- | 28.13 | -- | |
| Total Gate Charge | $Q_g$ | $V_{DS}$=480V, $I_D$=6A, $V_{GS}$=10V, (Note 2,3) | -- | 13.32 | -- | nC |
| Gate-Source Charge | $Q_{gs}$ | | -- | 4.13 | -- | |
| Gate-Drain Charge | $Q_{gd}$ | | -- | 4.19 | -- | |

## SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

| Characteristics | Symbol | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Continuous Source Current | $I_S$ | Integral Reverse P-N Junction Diode in the MOSFET | -- | -- | 6 | A |
| Pulsed Source Current | $I_{SM}$ | | -- | -- | 24 | |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=6A,$V_{GS}$=0V | -- | -- | 1.4 | V |
| Reverse Recovery Time | $T_{rr}$ | $I_S$=6A,$V_{GS}$=0V, $dI_F/dt$=100A/μs (Note 2) | -- | 488 | -- | ns |
| Reverse Recovery Charge | $Q_{rr}$ | | -- | 3 | -- | μC |

**Notes:**

1. L=30mH, $I_{AS}$=4.40A, $V_{DD}$=105V, $R_G$=25Ω, starting $TB_{JB}$=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

## TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

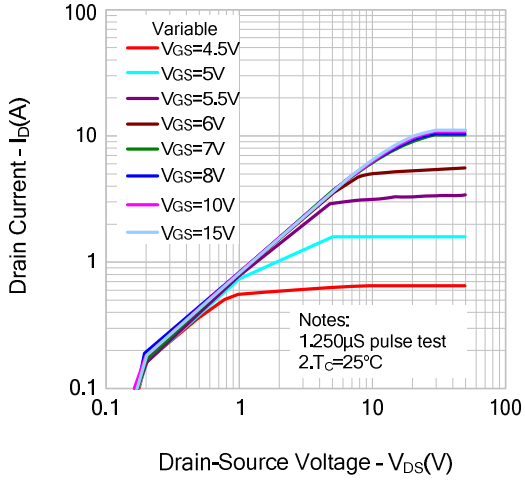



Figure 2. Transfer Characteristics

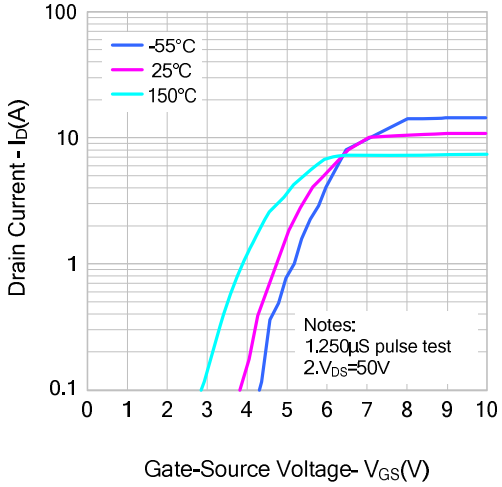



Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

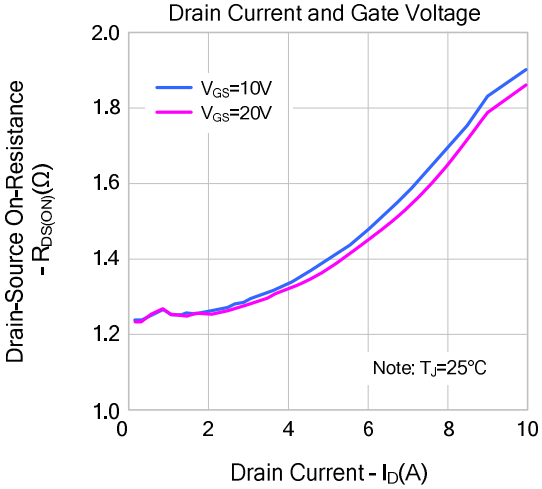



Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

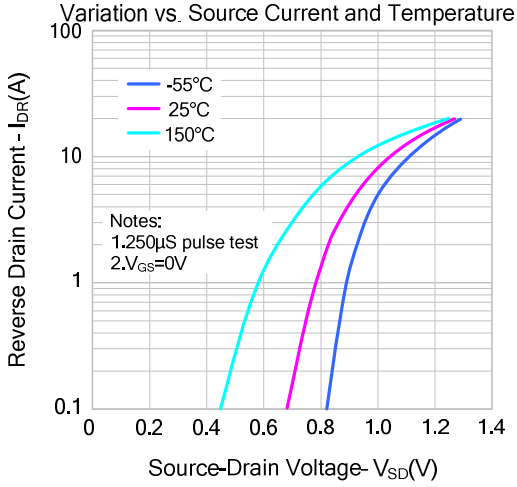



Figure 5. Capacitance Characteristics

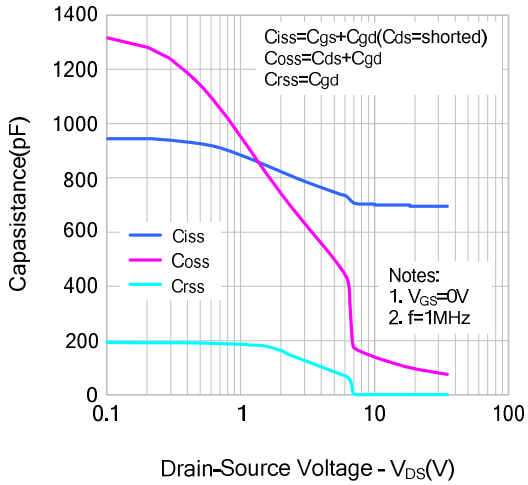
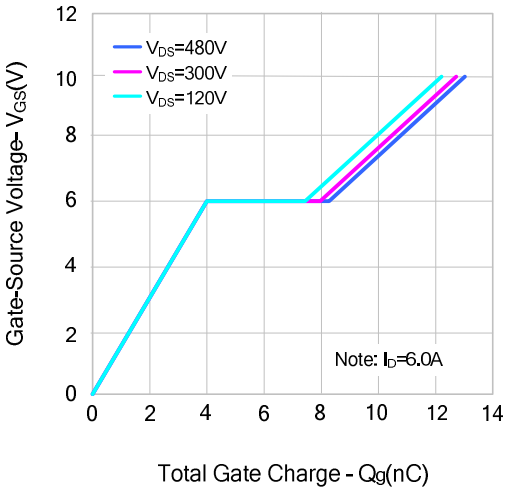



Figure 6. Gate Charge Characteristics



## TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

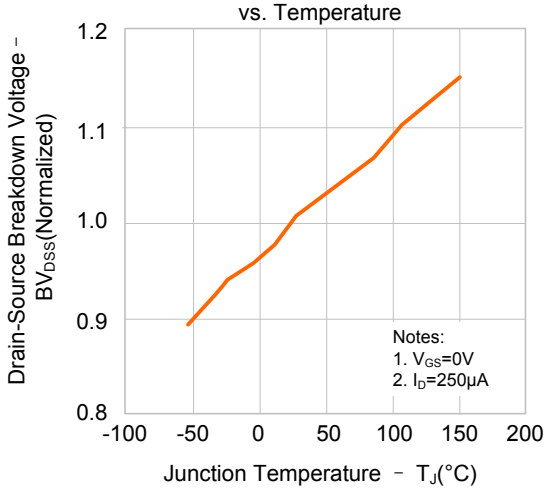



Figure 8. On-resistance Variation vs. Temperature

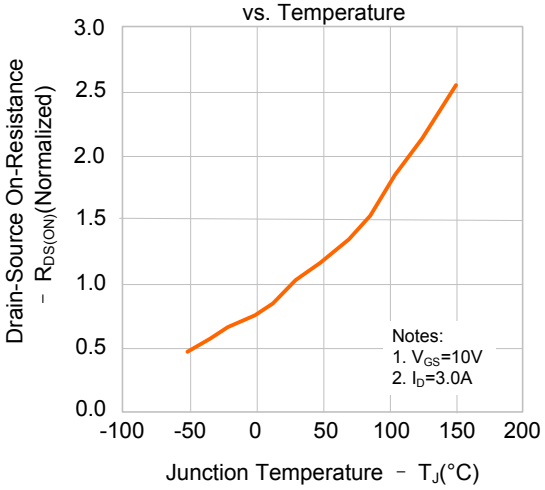



Figure 9-1. Max. Safe Operating Area(SVF6N60F/FQ)

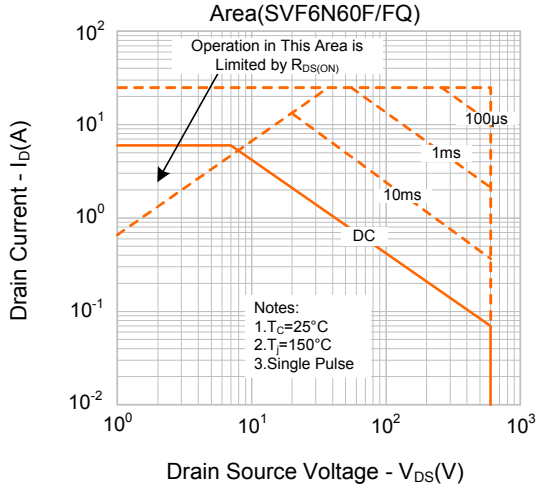



Figure 9-2. Max. Safe Operating Area(SVF6N60D)

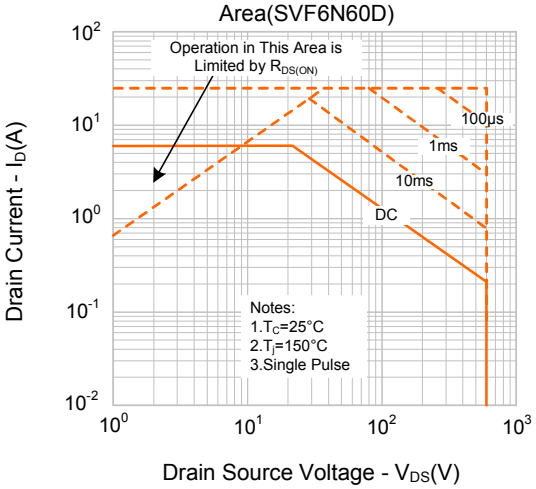
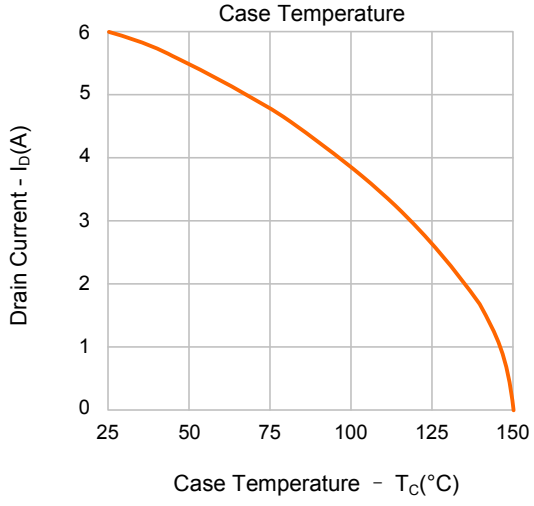
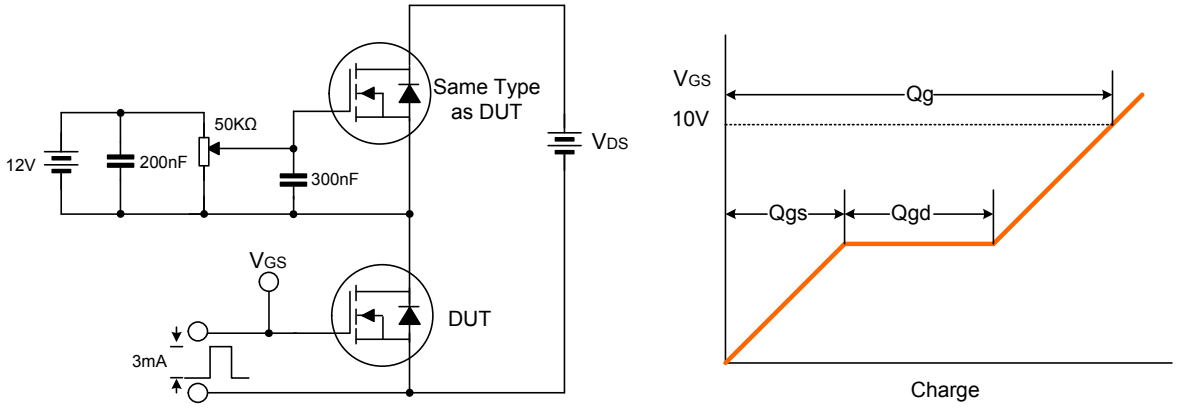



Figure 10. Maximum Drain Current vs. Case Temperature

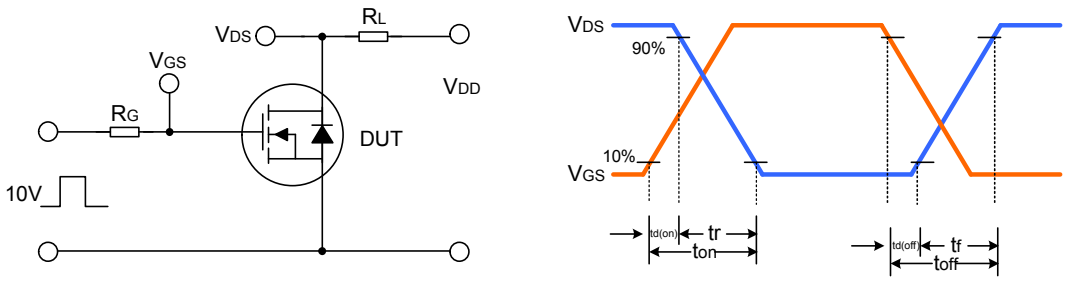


## TYPICAL TEST CIRCUIT

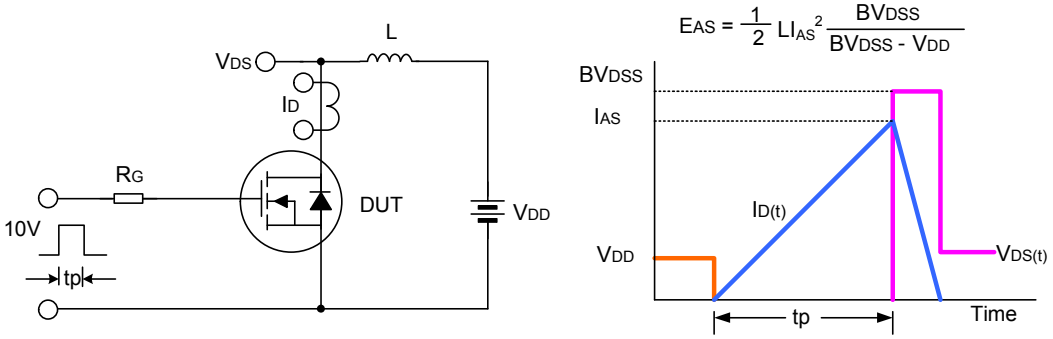
Gate Charge Test Circuit & Waveform




Resistive Switching Test Circuit & Waveform

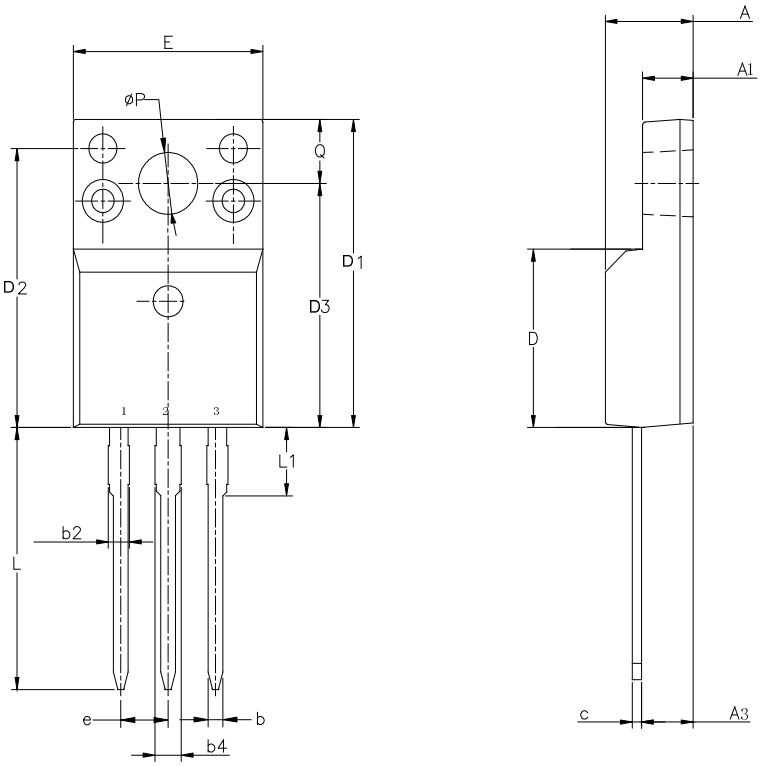



Unclamped Inductive Switching Test Circuit & Waveform



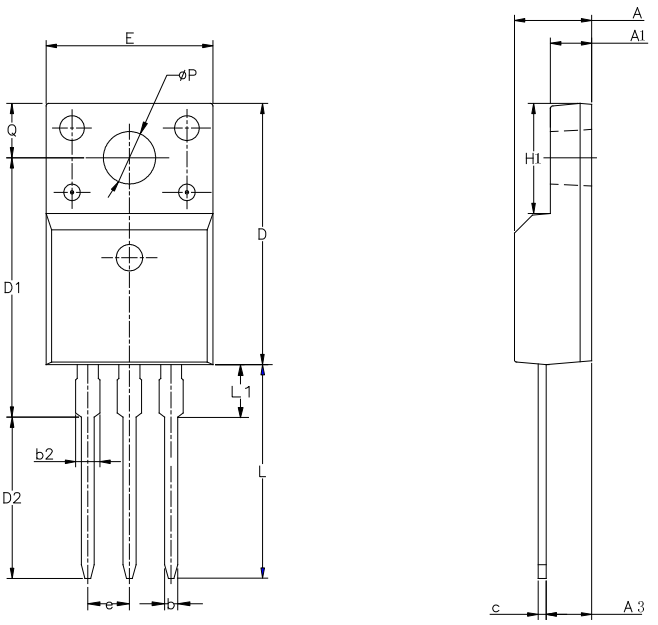
## PACKAGE OUTLINE

**TO-220FQ-3L** **UNIT: mm**




| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 4.57 | 4.70 | 4.83 |
| A1 | 2.57 | 2.70 | 2.83 |
| A3 | 2.56 | 2.76 | 2.93 |
| b | 0.76 | – | 0.90 |
| b2 | 0.96 | – | 1.19 |
| b4 | 1.24 | – | 1.47 |
| c | 0.46 | – | 0.60 |
| D | 8.99 | 9.19 | 9.39 |
| D1 | 15.80 | 15.87 | 16.13 |
| D2 | 14.17 | 14.37 | 14.57 |
| D3 | 12.30 | 12.57 | 12.87 |
| E | 9.96 | 10.16 | 10.36 |
| e | 2.54BSC | | |
| L | 13.20 | 13.50 | 13.70 |
| L1 | 3.37 | 3.52 | 3.67 |
| øP | 3.08 | 3.18 | 3.28 |
| Q | 3.20 | 3.30 | 3.40 |

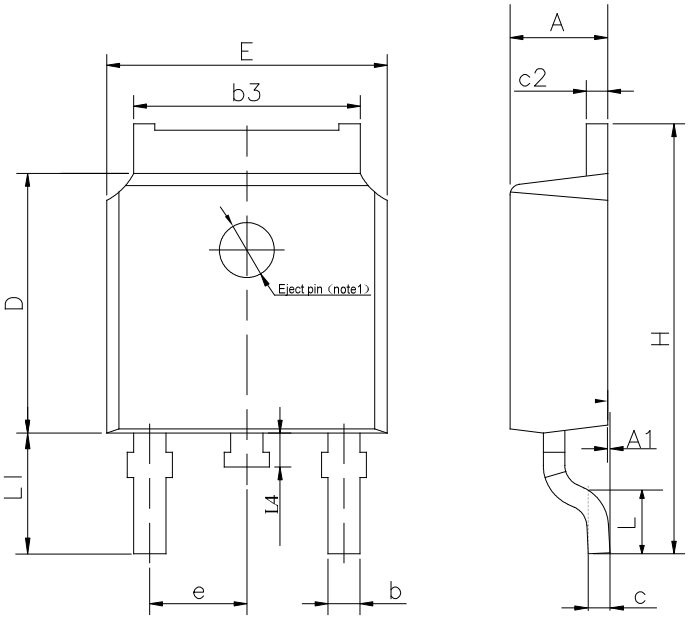
**TO-220F-3L** **UNIT: mm**




| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 4.42 | 4.70 | 5.02 |
| A1 | 2.30 | 2.54 | 2.80 |
| A3 | 2.50 | 2.76 | 3.10 |
| b | 0.70 | 0.80 | 0.90 |
| b2 | — | — | 1.47 |
| c | 0.35 | 0.50 | 0.65 |
| D | 15.25 | 15.87 | 16.25 |
| D1 | 15.30 | 15.75 | 16.30 |
| D2 | 9.30 | 9.80 | 10.30 |
| E | 9.73 | 10.16 | 10.36 |
| e | 2.54BCS | | |
| H1 | 6.40 | 6.68 | 7.00 |
| L | 12.48 | 12.98 | 13.48 |
| L1 | / | / | 3.50 |
| øP | 3.00 | 3.18 | 3.40 |
| Q | 3.05 | 3.30 | 3.55 |

## PACKAGE OUTLINE(continued)

**TO-252-2L** **UNIT: mm**




| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 2.10 | 2.30 | 2.50 |
| A1 | 0 | --- | 0.127 |
| b | 0.66 | 0.76 | 0.89 |
| b3 | 5.10 | 5.33 | 5.46 |
| c | 0.45 | --- | 0.65 |
| c2 | 0.45 | --- | 0.65 |
| D | 5.80 | 6.10 | 6.40 |
| E | 6.30 | 6.60 | 6.90 |
| e | | 2.30TYP | |
| H | 9.60 | 10.10 | 10.60 |
| L | 1.40 | 1.50 | 1.70 |
| L1 | | 2.90REF | |
| L4 | 0.60 | 0.80 | 1.00 |

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

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|---|---|---|---|
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Rev.: 2.5

Revision History:

1. Delete the package outline of TO-251J-3L

Rev.: 2.4

Revision History:

1. Update the package outline of TO-251J-3L

Rev.: 2.3

Revision History:

1. Add TO-220FQ-3L

Rev.: 2.2

Revision History:

1. Modify the General description
2. Modify the ordering information

Rev.: 2.1

Revision History:

1. Modify the package information of TO-220F-3L
2. Modify the package information of TO-252-2L

Rev.: 2.0

Revision History:

1. Modify the thermal characteristics

Rev.: 1.9

Revision History:

1. Modify the package outline of TO-251J-3L

Rev.: 1.8

Revision History:

1. Modify the ordering information

Rev.: 1.7

Revision History:

1. Change the schematic diagram of MOS

Rev.: 1.6

Revision History:

1. Add the pin no. in stereogram

Rev.: 1.5

Revision History:

1. Modify “ORDERING INFORMATION”

Rev.: 1.4

Revision History:

1. Modify “SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS”

Rev.: 1.3

Revision History:

1. Add the halogen free information of SVF6N60F

Rev.: 1.2

Revision History:

1. Delete the package of TO-251-3L and TO-251D-3L

Rev.: 1.1

Revision History:

1. Add the package of TO-251D-3L and TO-251J-3L
2. Update the package outline of TO-220F-3L and TO-252-2L

Rev.: 1.0

Revision History:

1. Original