

10A, 400V N-CHANNEL MOSFET

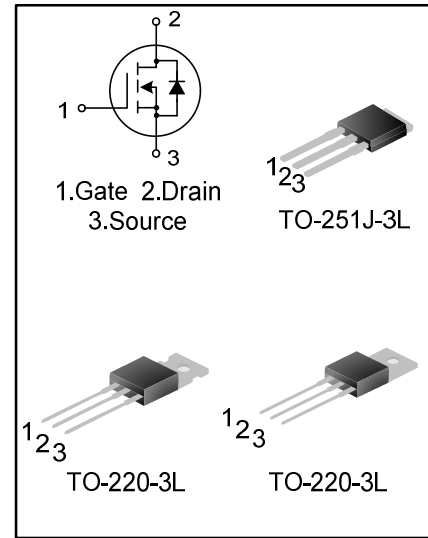
GENERAL DESCRIPTION

SVF740T/MJ is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- 10A, 400V, $R_{DS(on)(typ.)} = 0.45\Omega @ V_{GS} = 10V$
- Low gate charge
- Low C_{rss}
- Fast switching
- Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVF740T	TO-220-3L	SVF740T	Pb free	Tube
SVF740MJ	TO-251J-3L	SVF740MJ	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristics		Symbol	Ratings		Unit
			SVF740T	SVF740MJ	
Drain-Source Voltage		V _{DS}	400		V
Gate-Source Voltage		V _{GS}	±30		V
Drain Current	T _C =25°C	I _D	10		A
	T _C =100°C		6.3		
Drain Current Pulsed		I _{DM}	40		A
Power Dissipation(T _C =25°C) -Derate above 25°C		P _D	130	98	W
			1.04	0.78	W/°C
Single Pulsed Avalanche Energy(Note 1)		E _{AS}	517		mJ
Operation Junction Temperature Range		T _J	-55~+150		°C
Storage Temperature Range		T _{stg}	-55~+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVF740T	SVF740MJ	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.96	1.28	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.0	°C/W

ELECTRICAL CHARACTERISTICS ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	400	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=400V, V_{GS}=0V$	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30V, V_{DS}=0V$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=5.0A$	--	0.45	0.60	Ω
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V, f=1.0MHz$	--	801	--	pF
Output Capacitance	C_{oss}		--	118.5	--	
Reverse Transfer Capacitance	C_{rss}		--	5.06	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=200V, I_D=10A, R_G=25\Omega,$ (Note2,3)	--	15.44	--	ns
Turn-on Rise Time	t_r		--	38.60	--	
Turn-off Delay Time	$t_{d(off)}$		--	35.12	--	
Turn-off Fall Time	t_f		--	28.16	--	
Total Gate Charge	Q_g	$V_{DS}=320V, I_D=10A, V_{GS}=10V,$ (Note 2,3)	--	16.18	--	nC
Gate-Source Charge	Q_{gs}		--	4.77	--	
Gate-Drain Charge	Q_{gd}		--	7.18	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	10	A
Pulsed Source Current	I_{SM}		--	--	40	
Diode Forward Voltage	V_{SD}	$I_S=10A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=10A, V_{GS}=0V,$ $dl_F/dt=100A/\mu s$ (Note 2)	--	255.6	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.15	--	μC

Notes:

1. $L=30mH, I_{AS}=5.30A, V_{DD}=100V, R_G=25\Omega,$ starting $T_{BJB}=25^{\circ}\text{C}$;
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

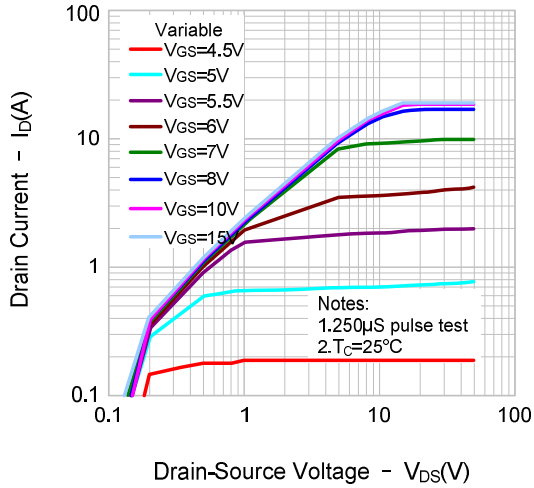


Figure 2. Transfer Characteristics

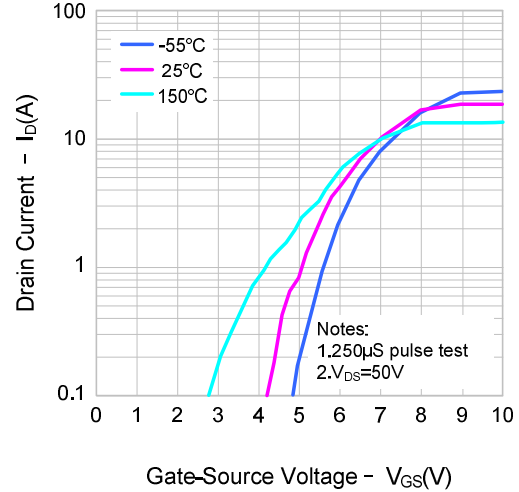


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

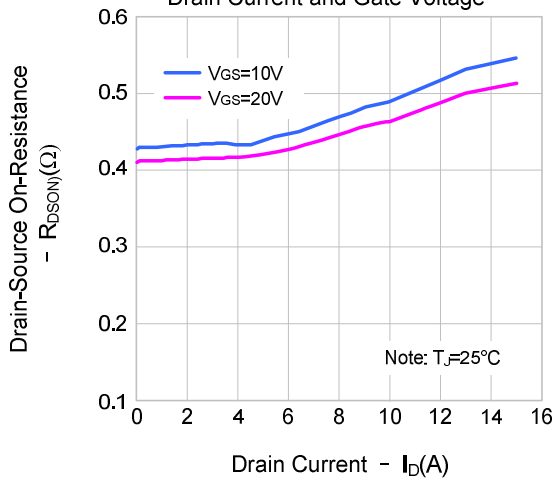


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

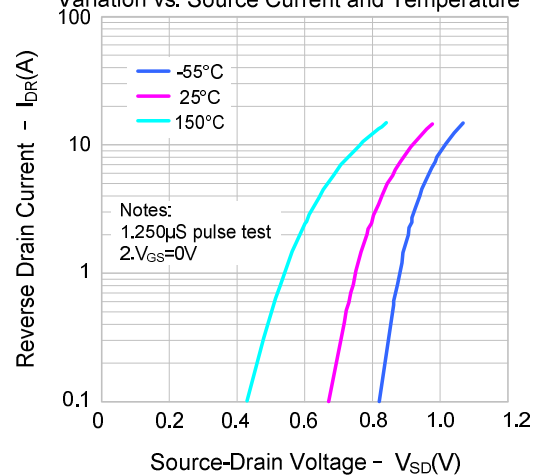


Figure 5. Capacitance Characteristics

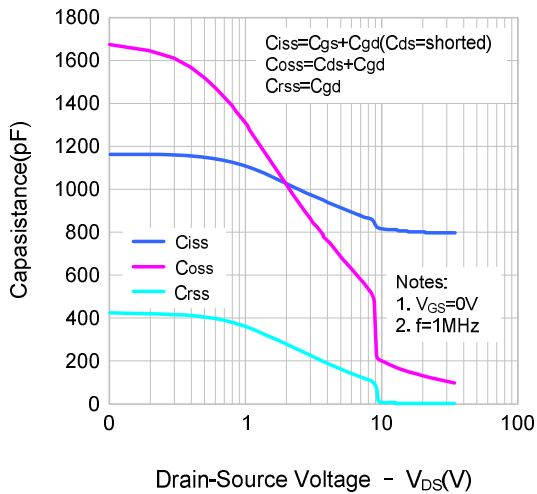
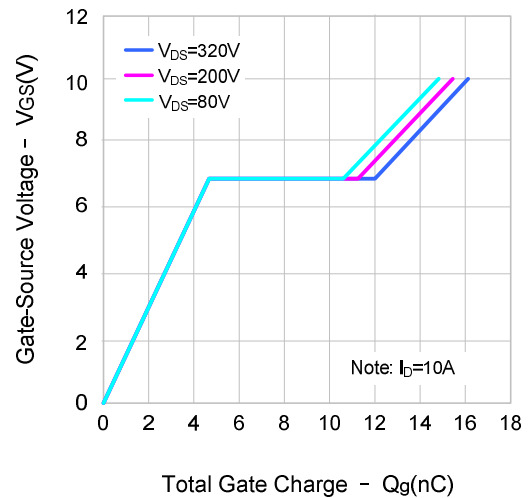


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

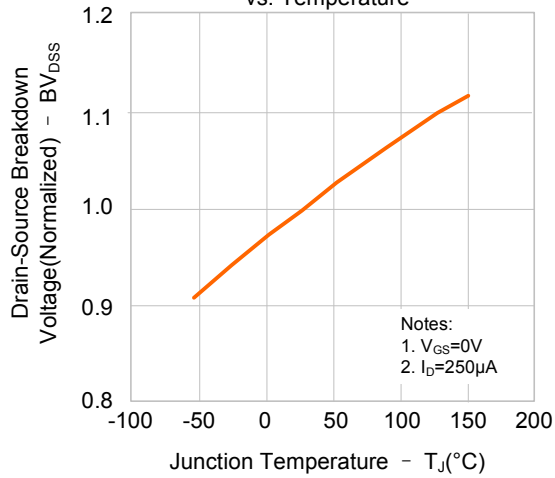


Figure 8. On-resistance Variation vs. Temperature

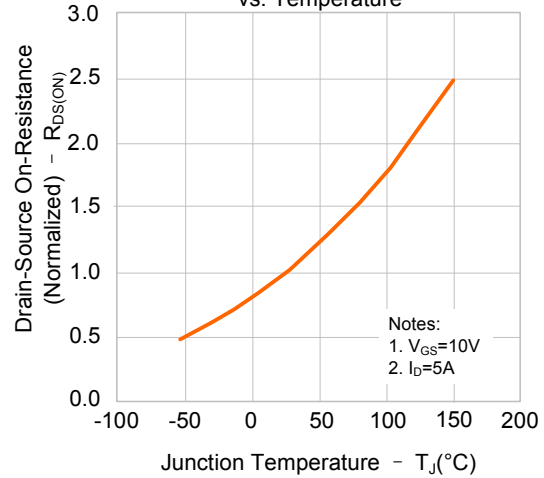


Figure 9-1. Max. Safe Operating Area(SVF740T)

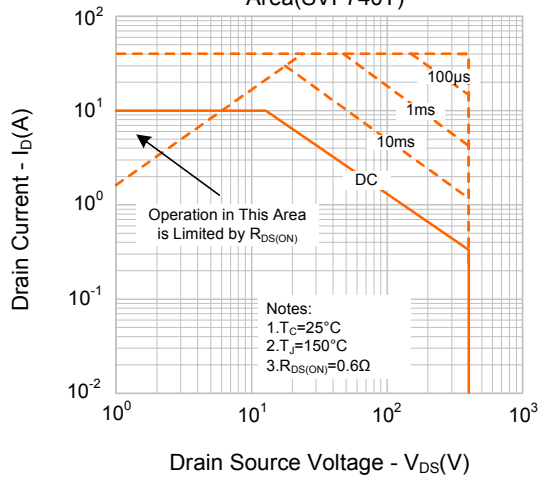


Figure 9-2. Max. Safe Operating Area(SVF740MJ)

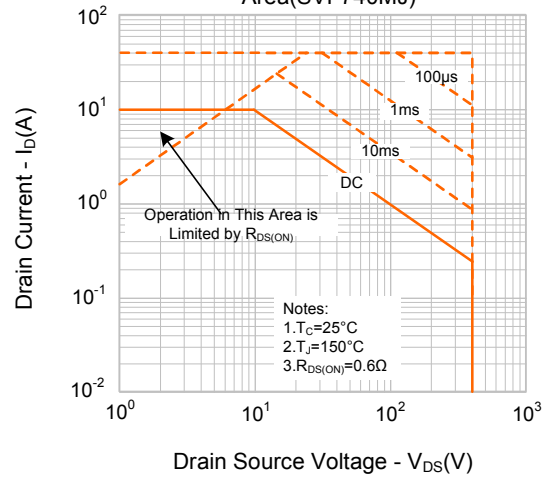
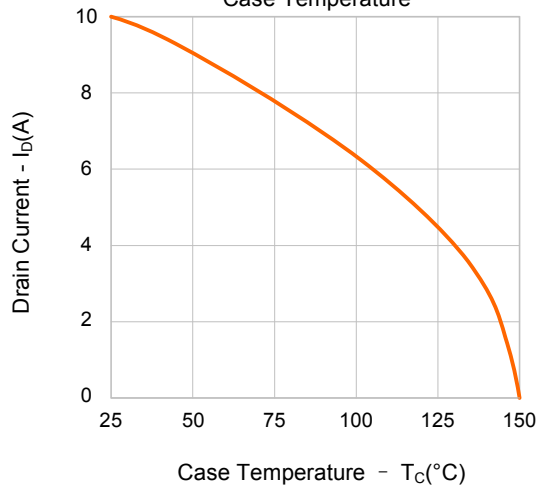
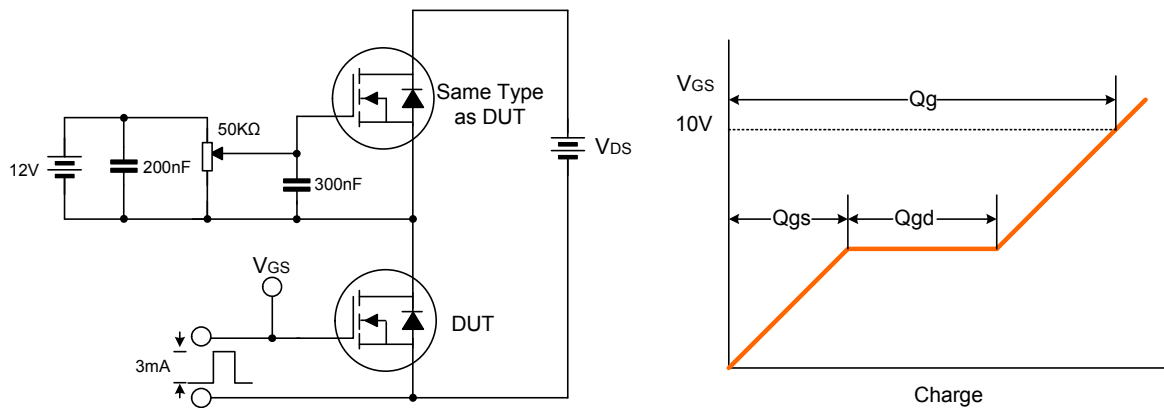


Figure 10. Maximum Drain Current vs. Case Temperature

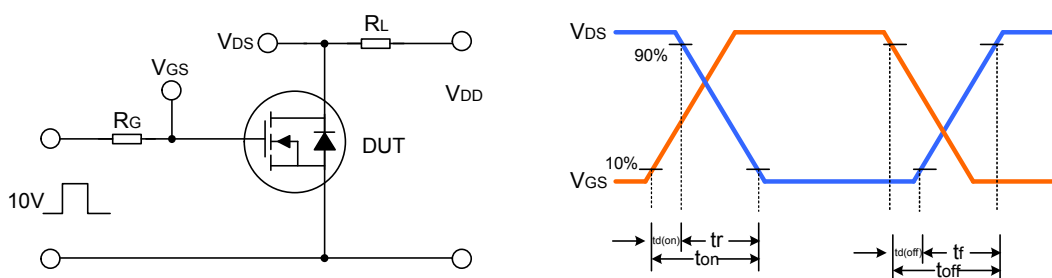


TYPICAL TEST CIRCUIT

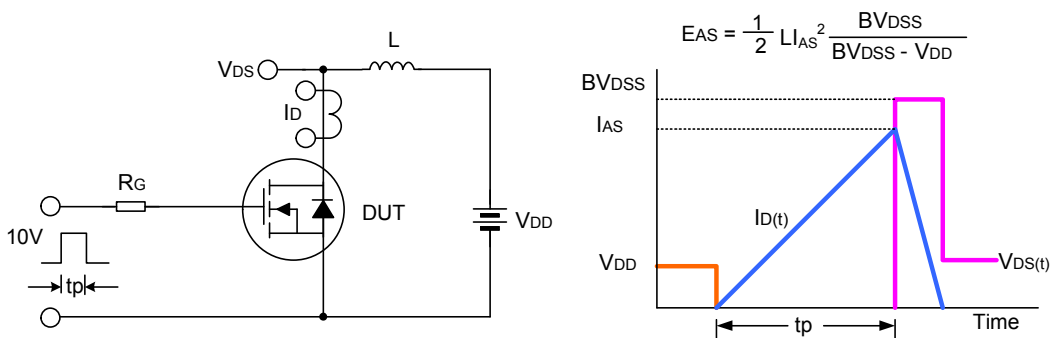
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



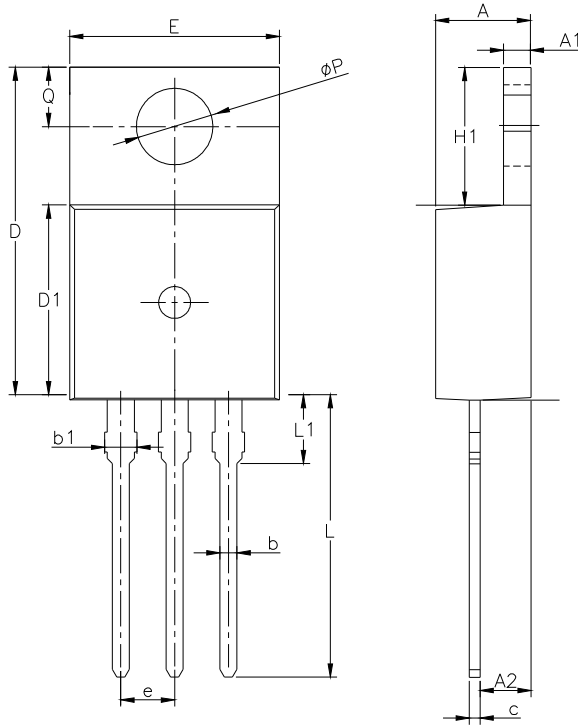
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220-3L

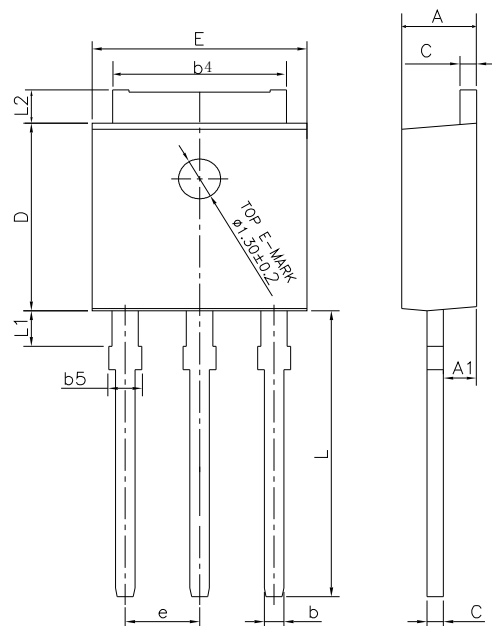
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ϕP	3.40	3.70	3.90
Q	2.60	—	3.20

TO-251J-3L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	2.18	2.30	2.39
A1	0.89	1.00	1.14
b	0.56	---	0.89
b4	4.95	5.33	5.46
b5	---	---	1.05
c	0.46	---	0.61
D	5.97	6.10	6.27
E	6.35	6.60	6.73
e	2.29 BCS		
L	8.89	9.30	9.65
L1	0.95	---	1.50
L2	0.89	---	1.27

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Part No.:	SVF740T/MJ	Document Type:	Datasheet
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Rev.: 2.0

Revision History:

1. Delete the package outline of TO-220F-3L
-

Rev.: 1.9

Revision History:

1. Update the package outline of TO-251J-3L
-

Rev.: 1.8

Revision History:

1. Modify the notes of curve
-

Rev.: 1.7

Revision History:

1. Modify the ordering information
-

Rev.: 1.6

Revision History:

1. Modify the ordering information
-

Rev.: 1.5

Revision History:

1. Add the package information of TO-251J-3L
-

Rev.: 1.4

Revision History:

1. Modify the package information of TO-220F-3L
 2. Modify the package information of TO-220-3L
-

Rev.: 1.3

Revision History:

1. Modify the thermal characteristics
-

Rev.: 1.2

Revision History:

1. Modify the ordering information
-

Rev.: 1.1

Revision History:

1. Change the schematic diagram of MOS
-



Rev.: 1.0

Revision History:

1. Initial release
