

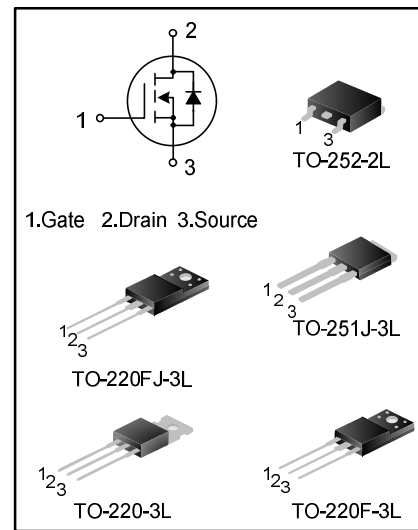
5A, 500V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF830T/D/MJ/FJ/F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- ◆ 5A,500V, $R_{DS(on)(typ.)}=1.2\Omega@V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low Crss
- ◆ Fast switching
- ◆ Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVF830T	TO-220-3L	SVF830T	Pb free	Tube
SVF830DTR	TO-252-2L	SVF830D	Halogen free	Tape & Reel
SVF830MJ	TO-251-3L	SVF830MJ	Halogen free	Tube
SVF830FJ	TO-220FJ-3L	830FJ	Halogen free	Tube
SVF830F	TO-220F-3L	SVF830F	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Ratings				Unit
		SVF830T	SVF830FJ/F	SVF830D	SVF830MJ	
Drain-Source Voltage	V _{DS}	500				V
Gate-Source Voltage	V _{GS}	±30				V
Drain Current	I _D	T _C =25°C				A
		5				
		T _C =100°C				
		3.1				
Drain Current Pulsed	I _{DM}	20				A
Power Dissipation(T _C =25°C) -Derate above 25°C	P _D	87.5	42	76	80	W
		0.7	0.34	0.61	0.64	W/°C
Single Pulsed Avalanche Energy(Note 1)	E _{AS}	234				mJ
Operation Junction Temperature Range	T _J	-55~+150				°C
Storage Temperature Range	T _{stg}	-55~+150				°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings				Unit
		SVF830T	SVF830FJ/F	SVF830D	SVF830MJ	
Thermal Resistance, Junction-to-Case	R _{θJC}	1.43	2.94	1.64	1.56	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	62.5	62.0	62.0	°C/W

ELECTRICAL CHARACTERISTICS (T_c=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	500	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =500V, V _{GS} =0V	--	--	1.0	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =2.5A	--	1.2	1.5	Ω
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	---	479	---	pF
Output Capacitance	C _{oss}		--	72	--	
Reverse Transfer Capacitance	C _{rss}		--	2.2	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =250V, I _D =5A, R _G =25Ω (Note 2,3)	--	15.3	--	ns
Turn-on Rise Time	t _r		--	37.4	--	
Turn-off Delay Time	t _{d(off)}		--	27.0	--	
Turn-off Fall Time	t _f		--	22.2	--	
Total Gate Charge	Q _g	V _{DS} =400V, I _D =5A, V _{GS} =10V (Note 2,3)	--	12.0	--	nC
Gate-Source Charge	Q _{gs}		--	4.0	--	
Gate-Drain Charge	Q _{gd}		--	4.28	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I _S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	5	A
Pulsed Source Current	I _{SM}		--	--	20	
Diode Forward Voltage	V _{SD}	I _S =5A, V _{GS} =0V	--	--	1.4	V
Reverse Recovery Time	T _{rr}	I _S =5 A, V _{GS} =0V, dI _F /dt=100A/μS(Note2)	--	420	--	ns
Reverse Recovery Charge	Q _{rr}		--	2.19	--	μC

Notes:

- L=30mH, I_{AS}=3.75A, V_{DD}=100V, R_G=25Ω, starting T_{BjB}=25°C;
- Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
- Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

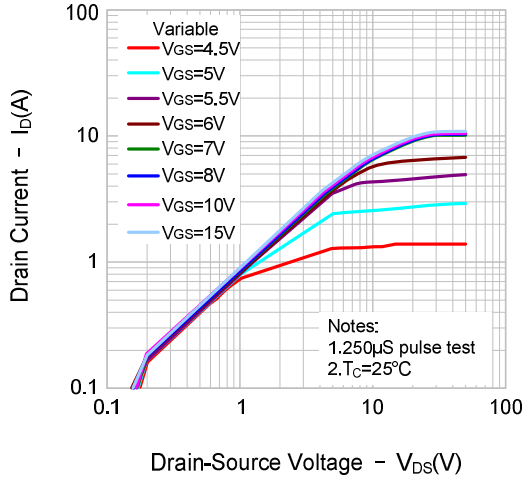


Figure 2. Transfer Characteristics

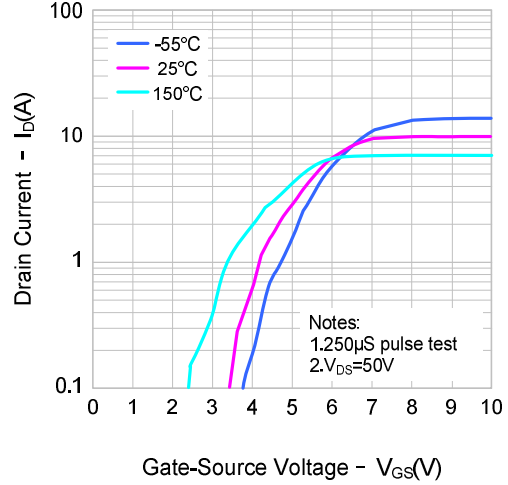


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

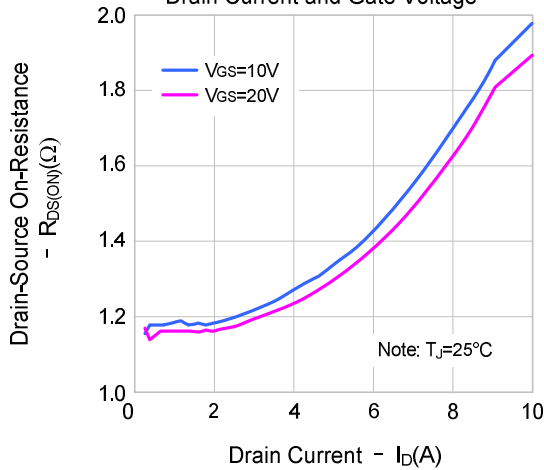


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

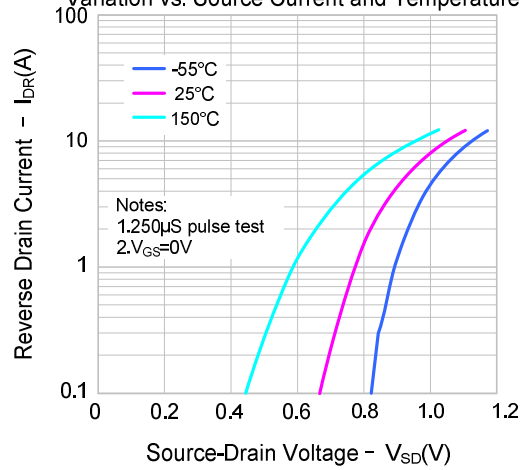


Figure 5. Capacitance Characteristics

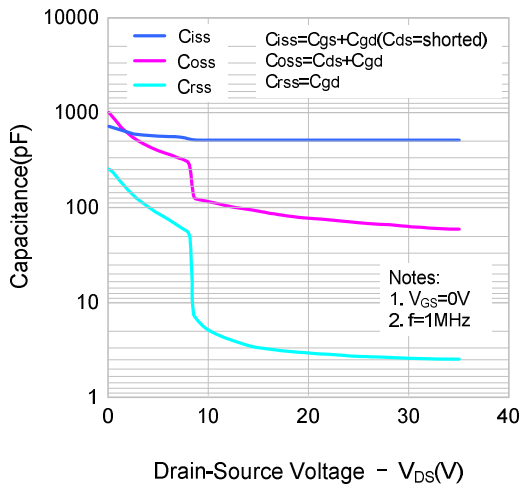
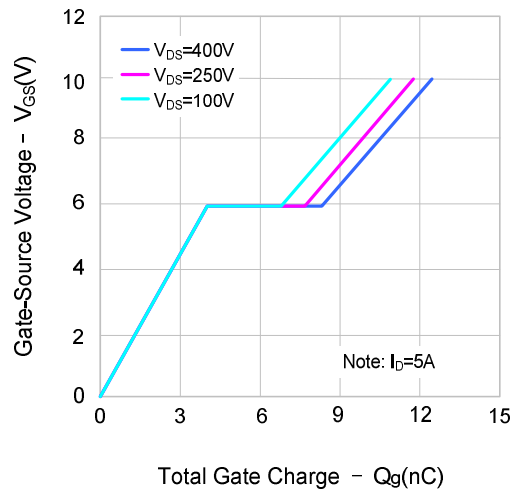


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

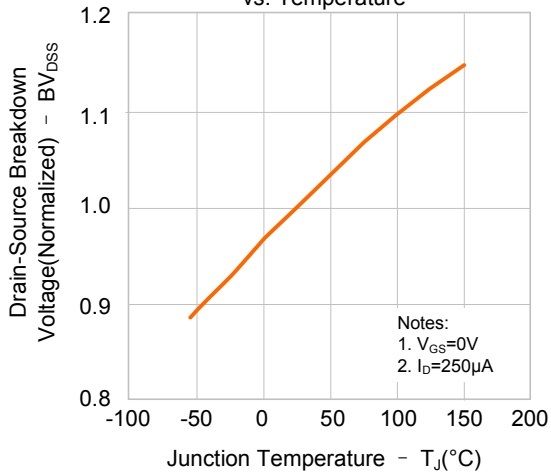


Figure 8. On-resistance Variation vs. Temperature

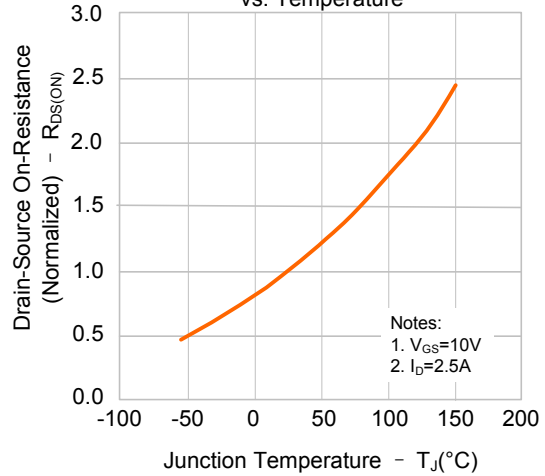


Figure 9-1. Max. Safe Operating Area(SVF830T)

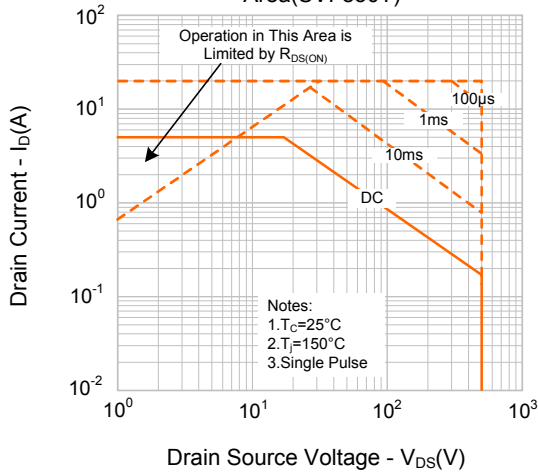


Figure 9-2. Max. Safe Operating Area(SVF830FJ/F)

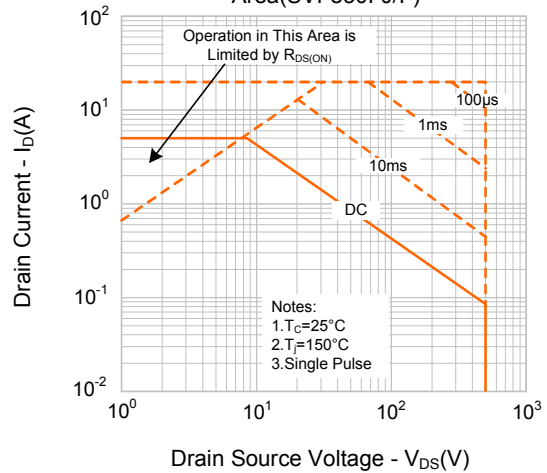


Figure 9-3. Max. Safe Operating Area(SVF830D)

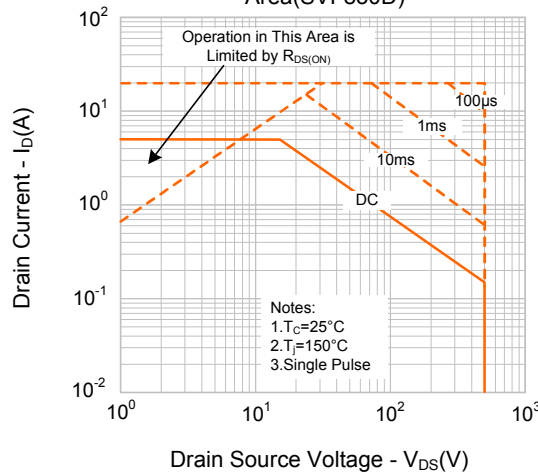
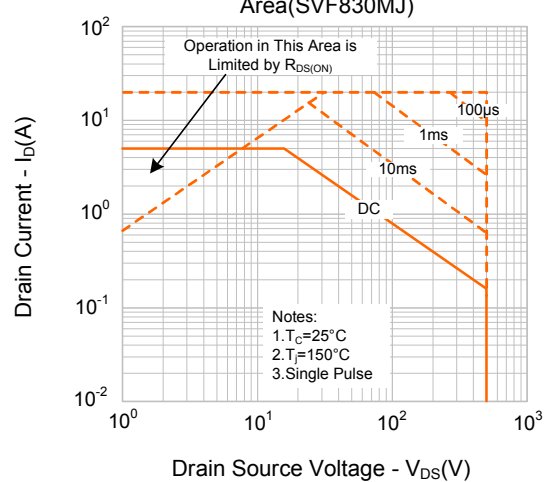
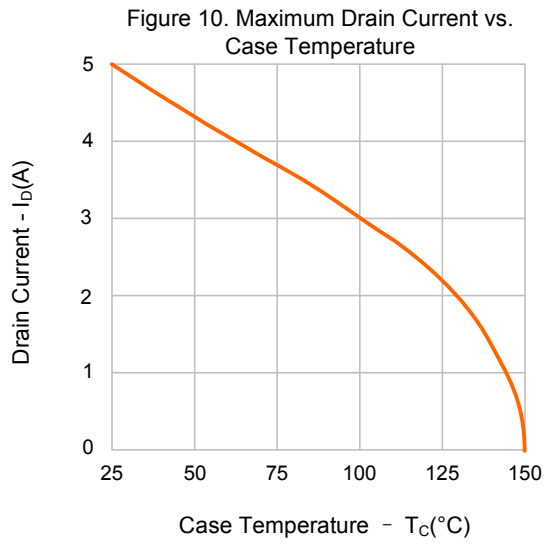


Figure 9-4. Max. Safe Operating Area(SVF830MJ)

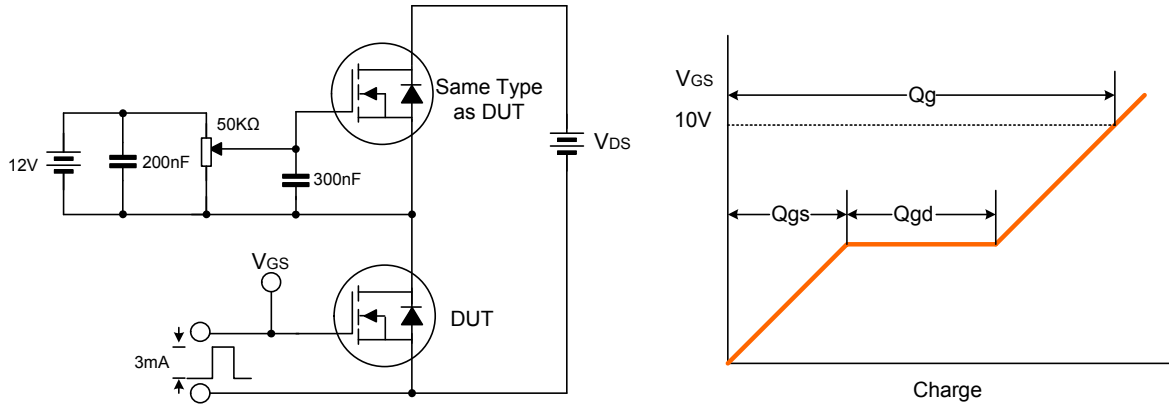


TYPICAL CHARACTERISTICS(continued)

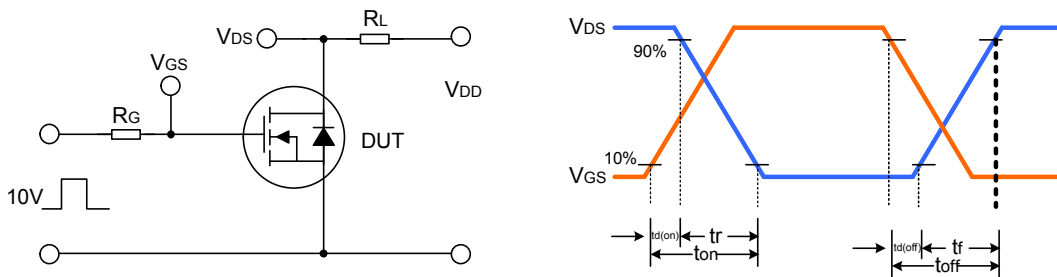


TYPICAL TEST CIRCUIT

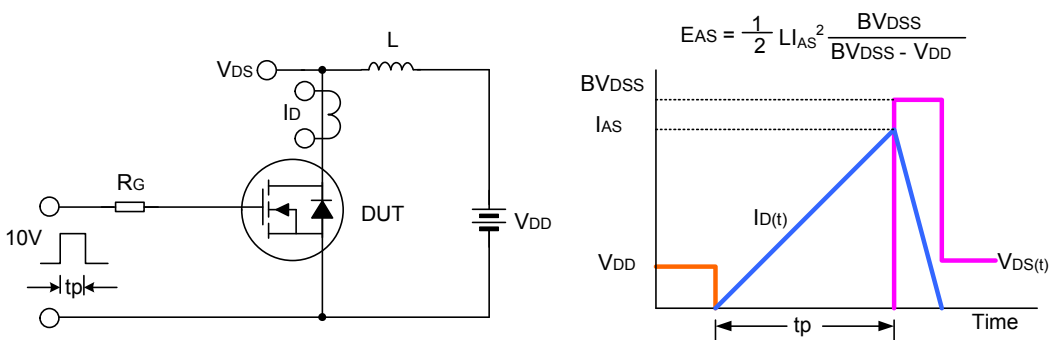
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



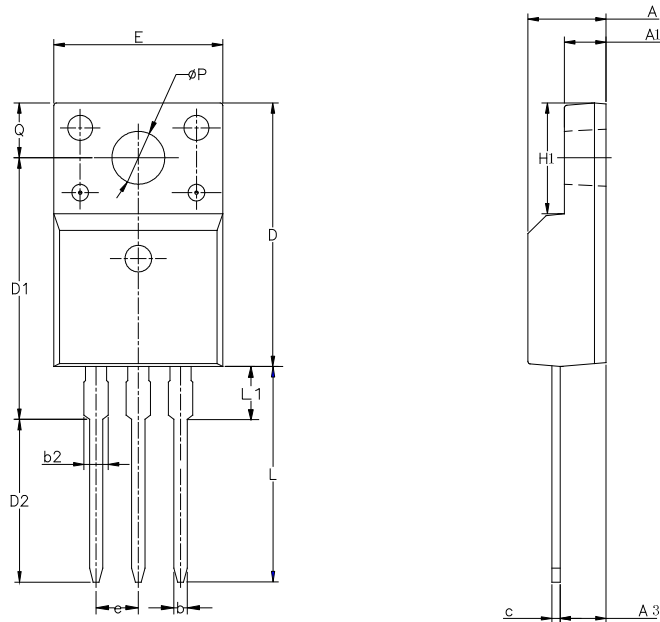
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220FJ-3L

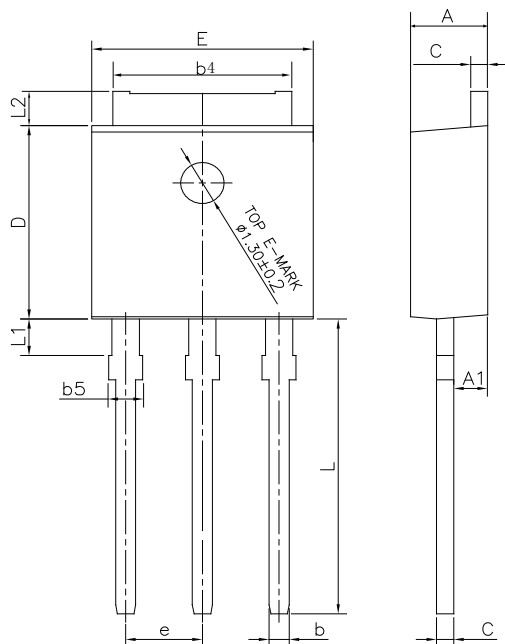
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.85
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	13.97	14.47	14.97
D2	10.58	11.08	11.58
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	2.00
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

TO-251J-3L

UNIT: mm

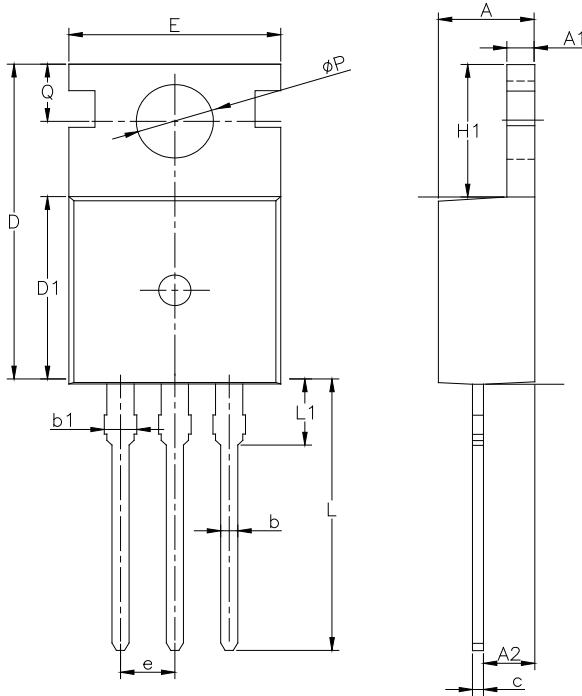


SYMBOL	MIN	NOM	MAX
A	2.18	2.30	2.39
A1	0.89	1.00	1.14
b	0.56	---	0.89
b4	4.95	5.33	5.46
b5	---	---	1.05
c	0.46	---	0.61
D	5.97	6.10	6.27
E	6.35	6.60	6.73
e	2.29 BCS		
L	8.89	9.30	9.65
L1	0.95	---	1.50
L2	0.89	---	1.27

PACKAGE OUTLINE(continued)

TO-220-3L

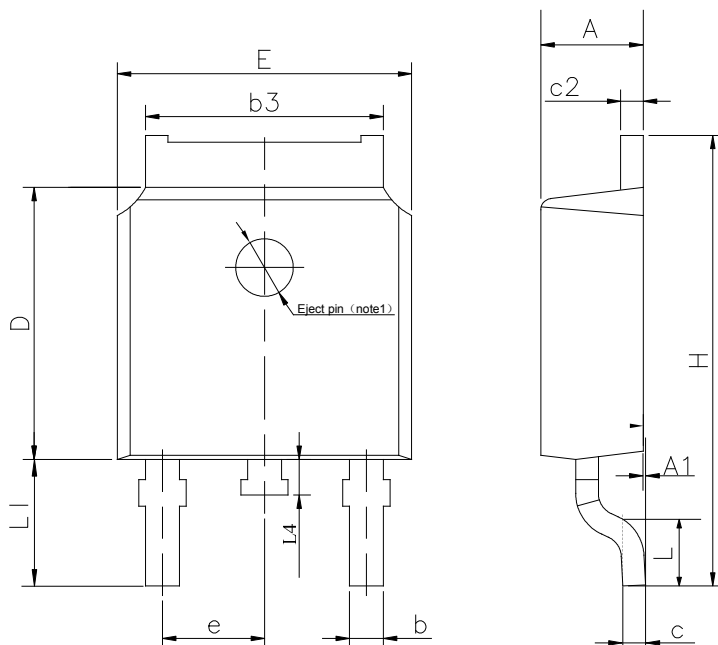
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
phi P	3.40	3.70	3.90
Q	2.60	—	3.20

TO-252-2L

UNIT: mm



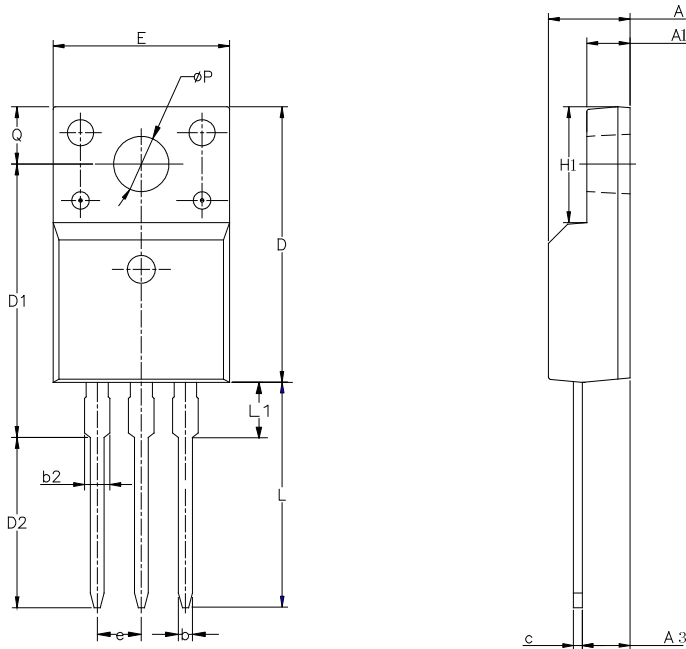
SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	—	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	—	0.65
c2	0.45	—	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

PACKAGE OUTLINE(continued)

TO-220F-3L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

Disclaimer :

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without prior notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
- All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.
- Silan will supply the best possible product for customers!

Part No.: SVF830T/D/MJ/FJ/F Document Type: Datasheet
Copyright: HANGZHOU SILAN MICROELECTRONICS CO.,LTD Website: <http://www.silan.com.cn>

Rev.: 2.4

Revision History:

1. Add the package outline of TO-220F-3L
-

Rev.: 2.3

Revision History:

1. Delete the package outline of TO-220F-3L
-

Rev.: 2.2

Revision History:

1. Add another solid figure of TO-220-3L
-

Rev.: 2.1

Revision History:

1. Add the package outline of TO-220FJ-3L
-

Rev.: 2.0

Revision History:

1. Update the package outline of TO-251J-3L
-

Rev.: 1.9

Revision History:

1. Modify the charge and the curve
-

Rev.: 1.8

Revision History:

1. Modify the package information of TO-220F-3L
 2. Modify the package information of TO-252-2L
 3. Modify the package information of TO-220-3L
-

Rev.: 1.7

Revision History:

1. Modify the ordering information
-

Rev.: 1.6

Revision History:

1. Modify the thermal characteristics
-

Rev.: 1.5

Revision History:

1. Modify the ordering information
-

Rev.: 1.4

Revision History:

1. Change the schematic diagram of MOS
-

Rev.: 1.3

Revision History:

1. Modify the values of T_{rr} and Q_{rr}
-

Rev.: 1.2

Revision History:

1. Add the package of TO-251J-3L
-

Rev.: 1.1

Revision History:

1. Modify "PACKAGE OUTLINE"
-

Rev.: 1.0

Revision History:

1. Original
-