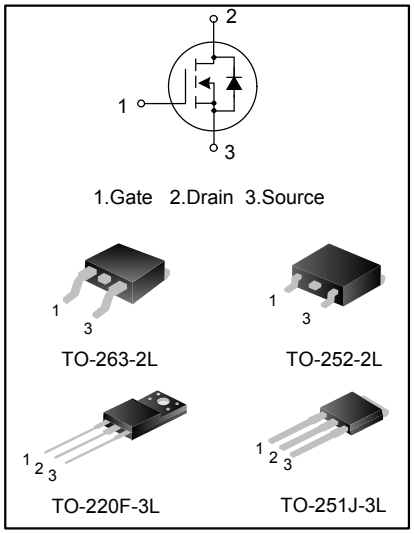
8A, 500V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF840F/D/S/MJ is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 8A, 500V, $R_{DS(on)(typ.)}$=0.68Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVF840F	TO-220F-3L	SVF840F	Pb free	Tube
SVF840DTR	TO-252-2L	SVF840D	Halogen free	Tape & Reel
SVF840S	TO-263-2L	SVF840S	Halogen free	Tube
SVF840STR	TO-263-2L	SVF840S	Halogen free	Tape & Reel
SVF840MJ	TO-251J-3L	SVF840MJ	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Characteristics		Symbol	Ratings				Unit
			SVF840F	SVF840D	SVF840S	SVF840MJ	
Drain-Source Voltage		V_{DS}	500				V
Gate-Source Voltage		V_{GS}	±30				V
Drain Current	T_C = 25°C	I_D	8				A
	T_C = 100°C		5				
Drain Current Pulsed		I_{DM}	32				A
Power Dissipation(T_C=25°C)		P_D	49	130	131	120	W
-Derate above 25°C			0.39	1.04	1.05	0.96	W/°C
Single Pulsed Avalanche Energ(Note 1)		E_{AS}	511.6				mJ
Operation Junction Temperature Range		T_J	-55～+150				°C
Storage Temperature Range		T_{stg}	-55～+150				°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings				Unit
		SVF840F	SVF840D	SVF840S	SVF840MJ	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.56	0.96	0.95	1.04	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.0	110	62	°C/W

ELECTRICAL CHARACTERISTICS (TC=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain –Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	500	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=500V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=4.0A	--	0.68	0.90	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ	--	904	--	pF
Output Capacitance	C_{oss}		--	120	--	
Reverse Transfer Capacitance	C_{rss}		--	2.69	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=250V,I_D=8.0A, R_G=25Ω (Note 2,3)	--	29.2	--	ns
Turn-on Rise Time	t_r		--	59.6	--	
Turn-off Delay Time	$t_{d(off)}$		--	41.3	--	
Turn-off Fall Time	t_f		--	29.2	--	
Total Gate Charge	Q_g	V_{DS}=400V,I_D=8.0A, V_{GS}=10V (Note 2,3)	--	14.7	--	nC
Gate-Source Charge	Q_{gs}		--	5.6	--	
Gate-Drain Charge	Q_{gd}		--	4.4	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	8.0	A
Pulsed Source Current	I_{SM}		--	--	32.0	
Diode Forward Voltage	V_{SD}	I_S=8.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=8.0A,V_{GS}=0V, dI_F/dt=100A/μS (Note 2)	--	470.91	--	ns
Reverse Recovery Charge	Q_{rr}		--	3.28	--	μC

Notes:

1. L=30mH, I_{AS}=5.3A, V_{DD}=130V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

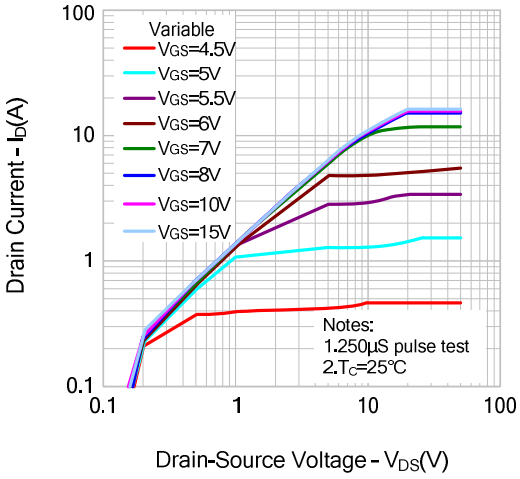


Figure 2. Transfer Characteristics

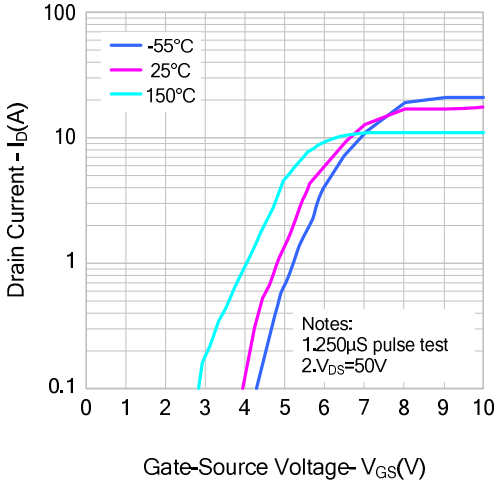


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

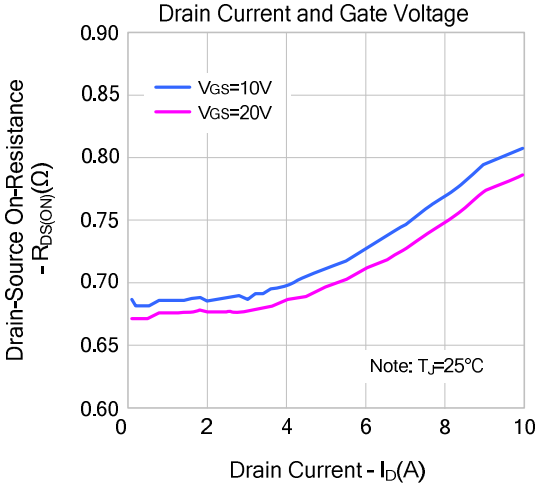


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

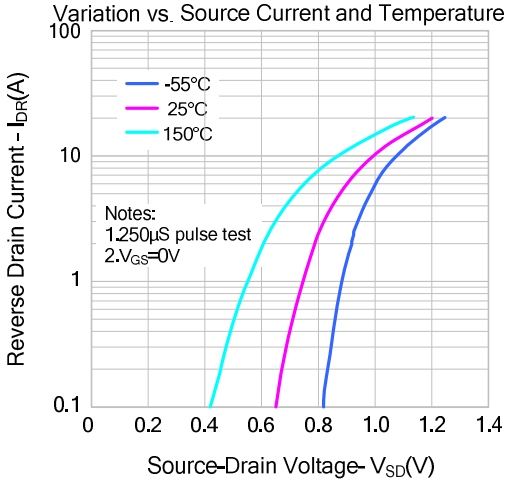


Figure 5. Capacitance Characteristics

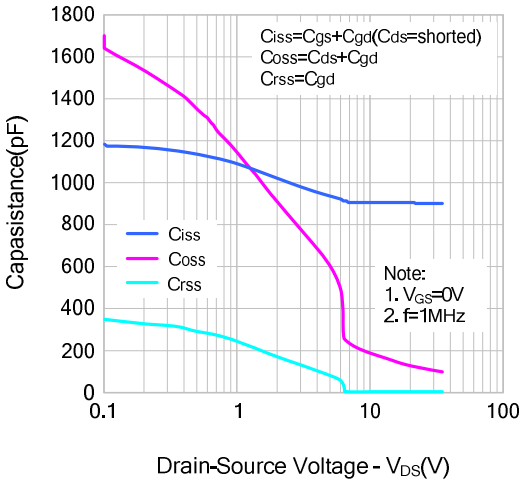
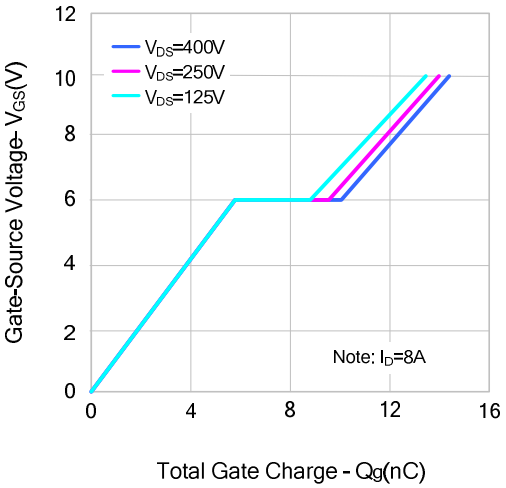


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

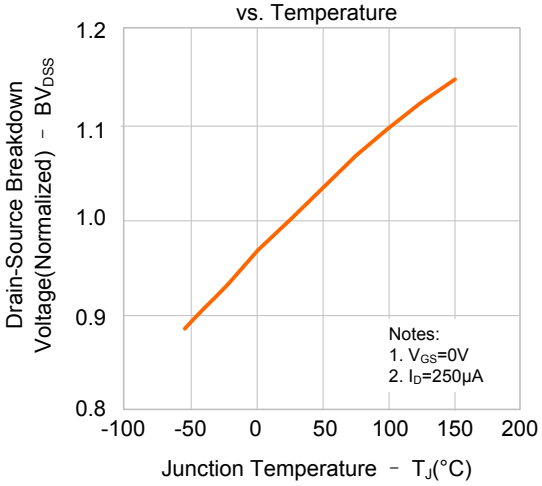


Figure 8. On-resistance Variation vs. Temperature

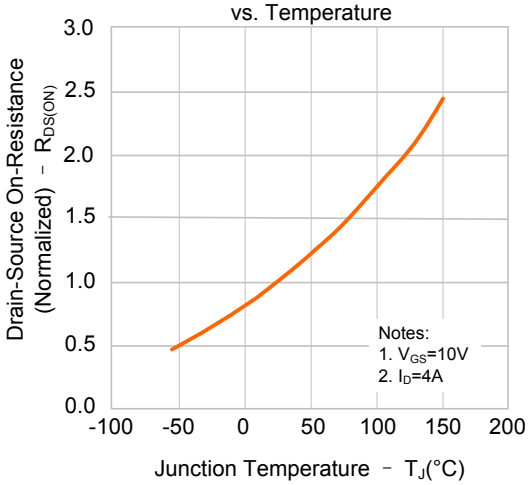


Figure 9-1. Max. Safe Operating Area(SVF840MJ)

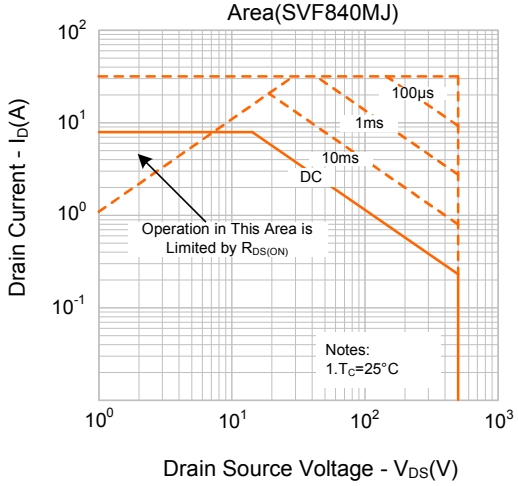


Figure 9-2. Max. Safe Operating Area(SVF840F)

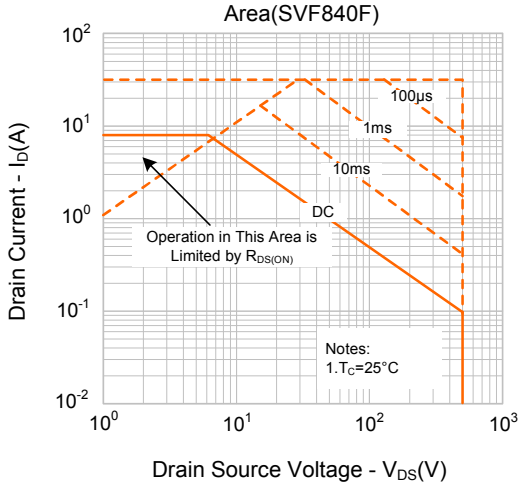


Figure 9-3. Max. Safe Operating Area(SVF840D)

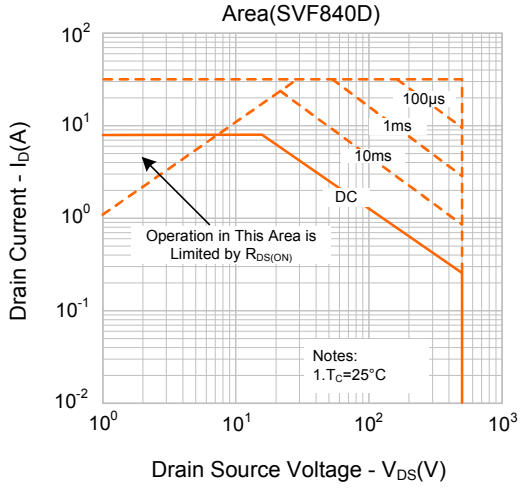
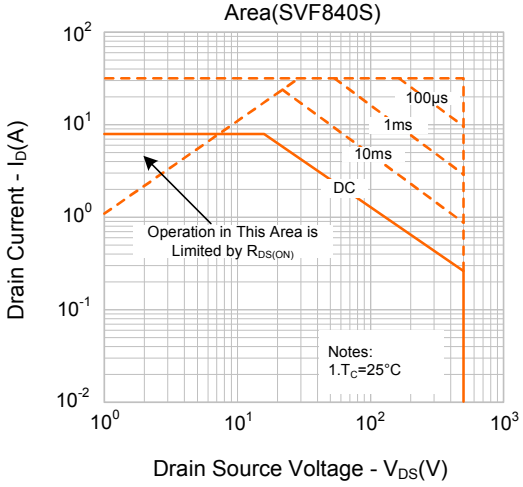
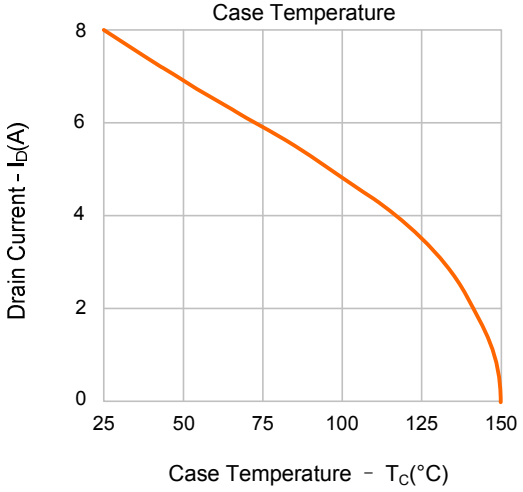


Figure 9-4. Max. Safe Operating Area(SVF840S)



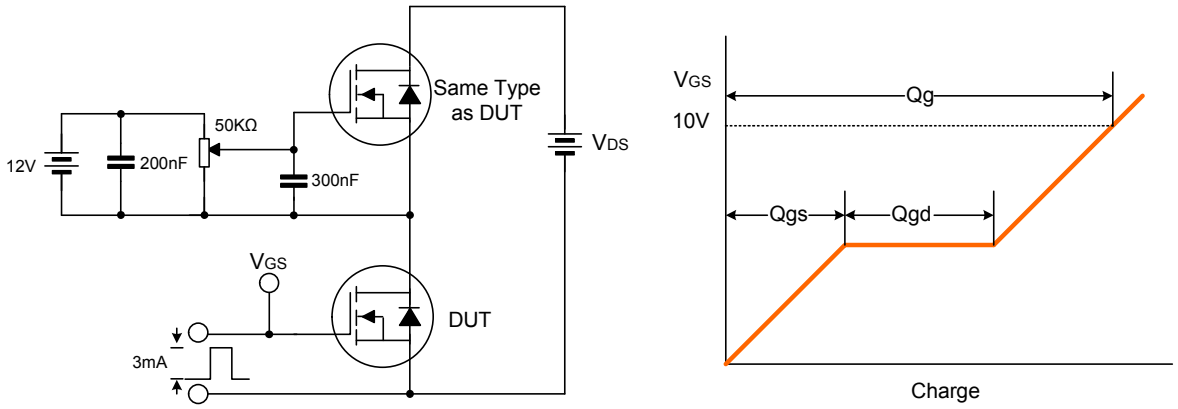
TYPICAL CHARACTERISTICS(continued)

Figure 10. Maximum Drain Current vs. Case Temperature

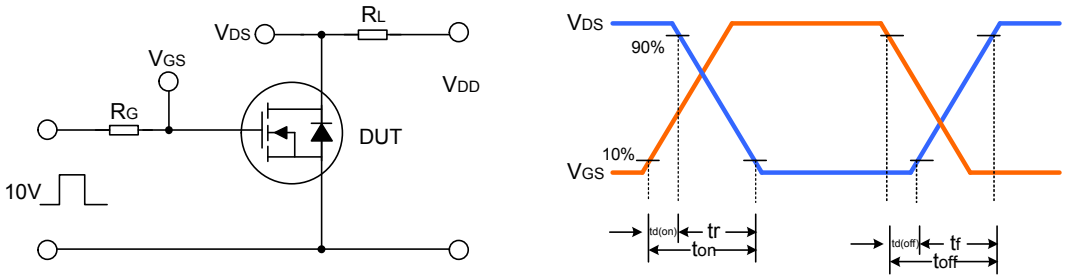


TYPICAL TEST CIRCUIT

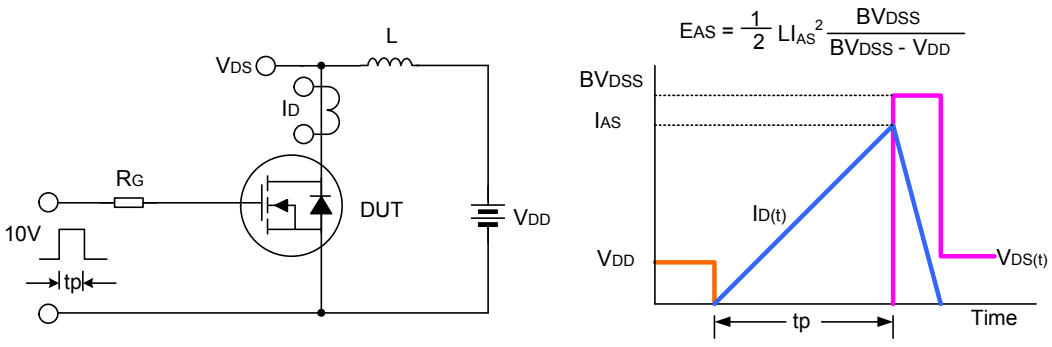
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

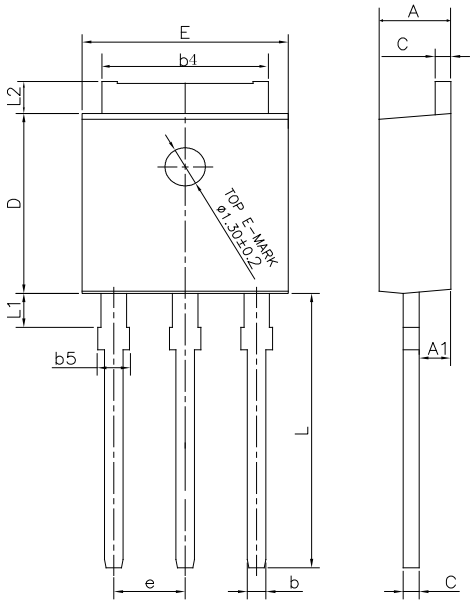


Unclamped Inductive Switching Test Circuit & Waveform



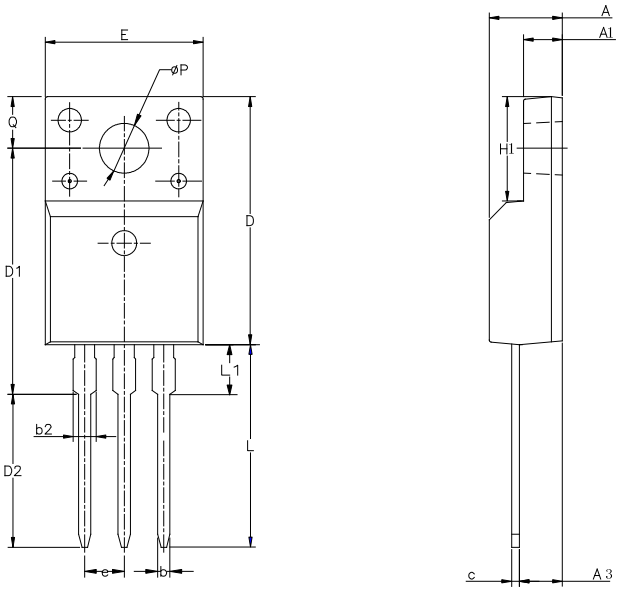
PACKAGE OUTLINE

TO-251J-3L **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	2.18	2.30	2.39
A1	0.89	1.00	1.14
b	0.56	---	0.89
b4	4.95	5.33	5.46
b5	---	---	1.05
c	0.46	---	0.61
D	5.97	6.10	6.27
E	6.35	6.60	6.73
e		2.29 BCS	
L	8.89	9.30	9.65
L1	0.95	---	1.50
L2	0.89	---	1.27

TO-220F-3L **单位: mm**

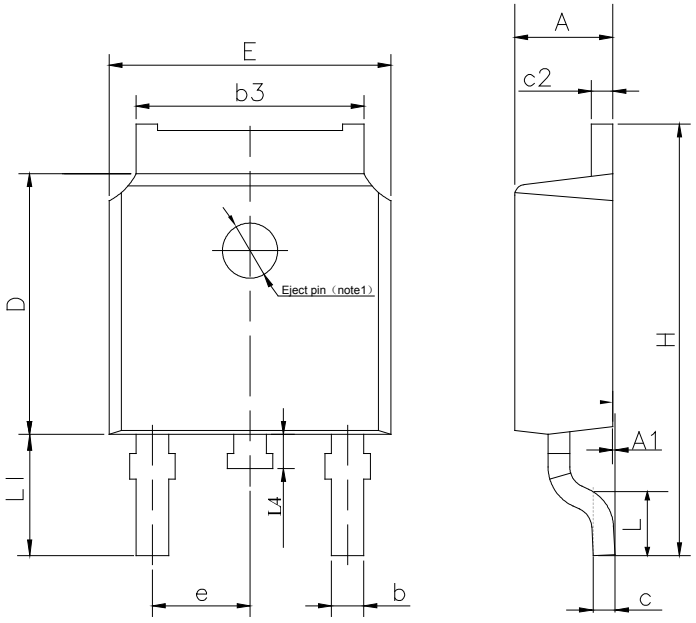


SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e		2.54BCS	
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
øP	3.00	3.18	3.40
Q	3.05	3.30	3.55

PACKAGE OUTLINE (continued)

TO-252-2L

UNIT: mm

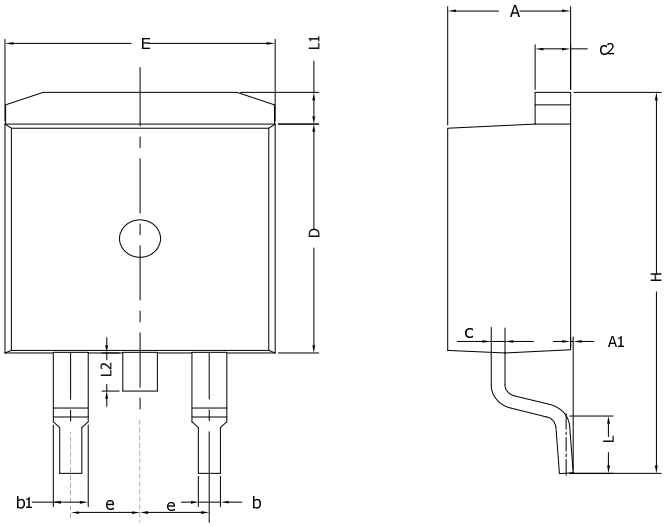


SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

TO-263-2L

单位: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
c	0.30	---	0.60
c2	1.17	1.27	1.37
D	8.50	---	9.35
E	9.80	---	10.45
e	2.54BSC		
H	14.70	---	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	---	---	1.75

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Part No.:	SVF840F/D/S/MJ	Document Type:	Datasheet
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Rev.: 2.6

Revision History:

1. Delete the package outline of TO-220-3L

Rev.: 2.5

Revision History:

1. Add another solid figure of TO-220-3L

Rev.: 2.4

Revision History:

1. Update the package outline of TO-251J-3L

Rev.: 2.3

Revision History:

1. Modify the Typical Characteristics

Rev.: 2.2

Revision History:

1. Modify the ordering information

Rev.: 2.1

Revision History:

1. Add the package information of TO-251J-3L

Rev.: 2.0

Revision History:

1. Modify the package information of TO-220F-3L;
2. Modify the package information of TO-252-2L;
3. Modify the package information of TO-220-3L

Rev.: 1.9

Revision History:

1. Modify the ordering information

Rev.: 1.8

Revision History:

1. Modify the thermal characteristics

Rev.: 1.7

Revision History:

1. Modify the ordering information

Rev.: 1.6

Revision History:

1. Modify the ordering information

Rev.: 1.5

Revision History:

1. Change the schematic diagram of MOS

Rev.: 1.4

Revision History:

1. Modify the values of T_{rr} and Q_{rr}

Rev.: 1.3

Revision History:

1. Add the package of TO-263-2L

Rev.: 1.2

Revision History:

1. Add the package of TO-252-2L

Rev.: 1.1

Revision History:

1. Modify “PACKAGE OUTLINE”

Rev.: 1.0

Revision History:

1. Original