

9A, 650V N-CHANNEL MOSFET

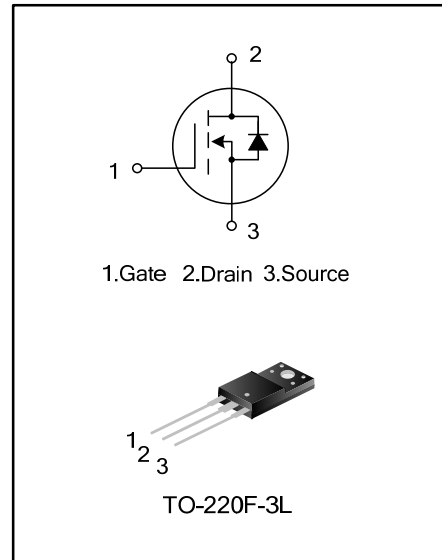
GENERAL DESCRIPTION

SVF9N65F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

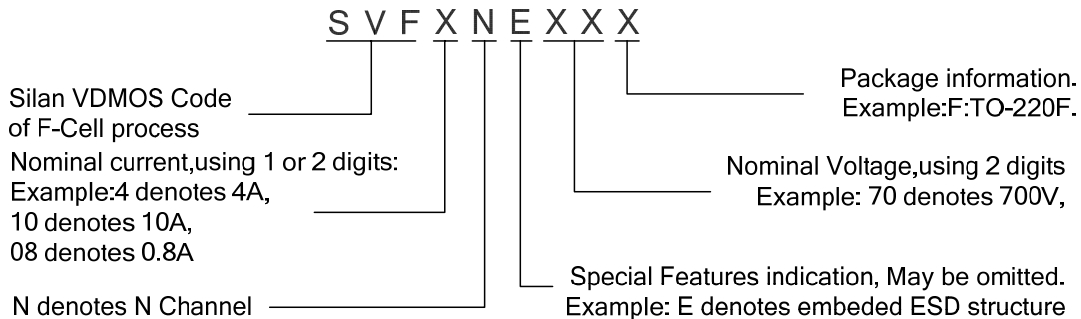
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- * 9A, 650V, $R_{DS(on)(typ)}=0.98\Omega@V_{GS}=10V$
- * Low gate charge
- * Low Crss
- * Fast switching
- * Improved dv/dt capability



NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Material	packing
SVF9N65F	TO-220F-3L	SVF9N65F	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	V
Drain Current	I_D	$T_C=25^\circ\text{C}$	9.0
		$T_C=100^\circ\text{C}$	5.69
Drain Current Pulsed	I_{DM}	36.0	A
Power Dissipation($T_C=25^\circ\text{C}$) -Derate above 25°C	P_D	49	W
		0.39	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy (Note 1)	E_{AS}	532	mJ
Operation Junction Temperature Range	T_{stg}	$-55 \sim +150$	$^\circ\text{C}$
Storage Temperature Range	I_{DM}	$-55 \sim +150$	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Rating	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.55	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	120	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=650\text{V}, V_{GS}=0\text{V}$	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30\text{V}, V_{DS}=0\text{V}$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=4.5\text{A}$	--	0.98	1.2	Ω
Input Capacitance	C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0\text{V},$ $f=1.0\text{MHz}$	--	928.0	--	pF
Output Capacitance	C_{oss}		--	109.3	--	
Reverse Transfer Capacitance	C_{rss}		--	4.6	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=325\text{V}, R_G=10\Omega,$ $I_D=9.0\text{A}$ (Note2, 3)	--	12.8	--	ns
Turn-on Rise Time	t_r		--	25.7	--	
Turn-off Delay Time	$t_{d(off)}$		--	31.1	--	
Turn-off Fall Time	t_f		--	23.9	--	
Total Gate Charge	Q_g	$V_{DS}=520\text{V}, I_D=9.0\text{A},$ $V_{GS}=10\text{V}$ (Note2, 3)	--	20.71	--	nC
Gate-Source Charge	Q_{gs}		--	5.69	--	
Gate-Drain Charge	Q_{gd}		--	8.47	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	9.0	A
Pulsed Source Current	I_{SM}		--	--	36.0	
Diode Forward Voltage	V_{SD}	$I_S=9.0A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=9.0A, V_{GS}=0V, di_F/dt=100A/\mu S$	--	574.2	--	ns
Reverse Recovery Charge	Q_{rr}		--	4.36	--	μC

Notes:

1. $L=30mH, I_{AS}=5.78A, V_{DD}=50V, R_G=25\Omega$, starting $T_J=25^\circ C$;
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycles $\leq 2\%$;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

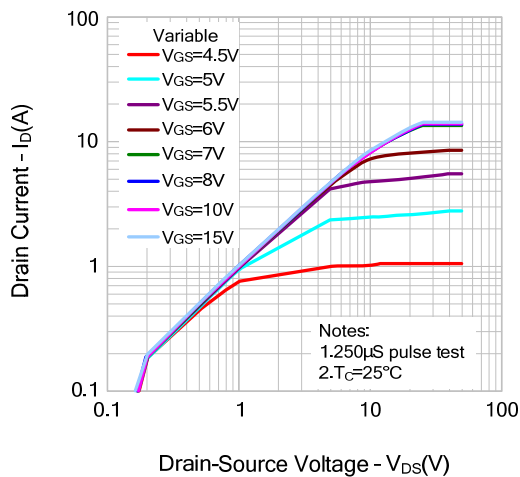


Figure 2. Transfer Characteristics

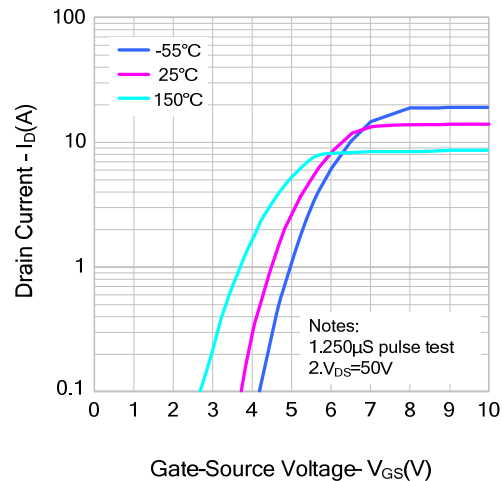


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

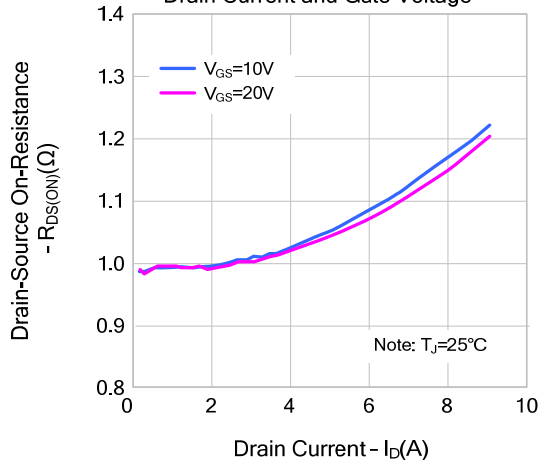
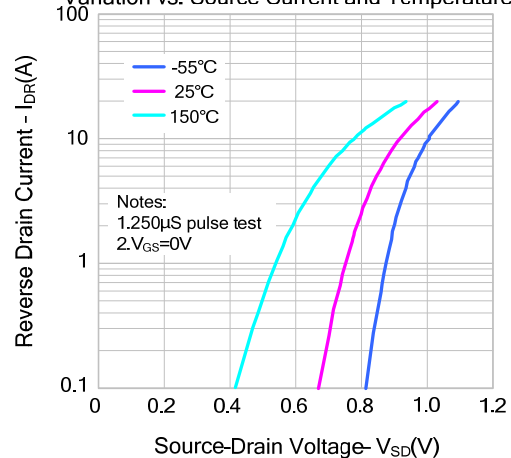


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature



TYPICAL CHARACTERISTICS(continued)

Figure 5. Capacitance Characteristics

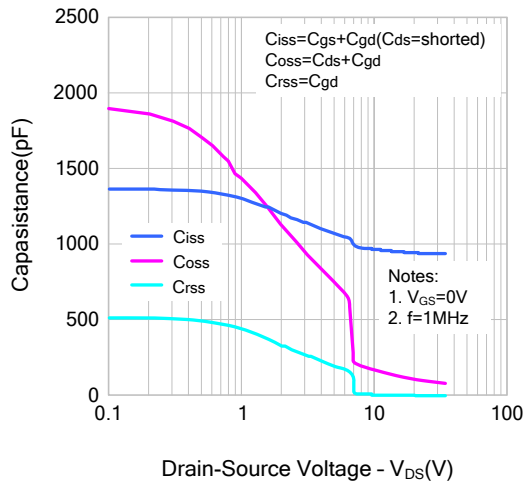


Figure 6. Gate Charge Characteristics

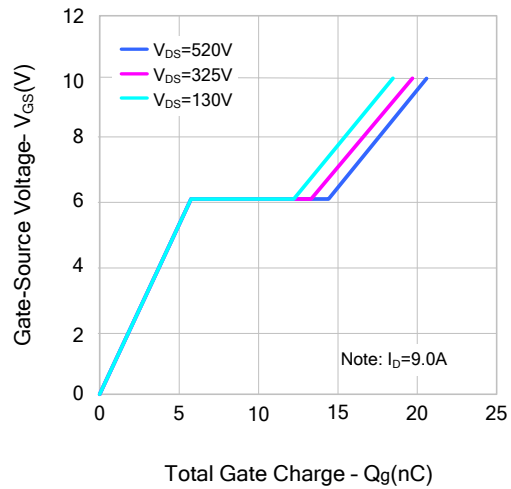


Figure 7. Breakdown Voltage Variation vs. Temperature

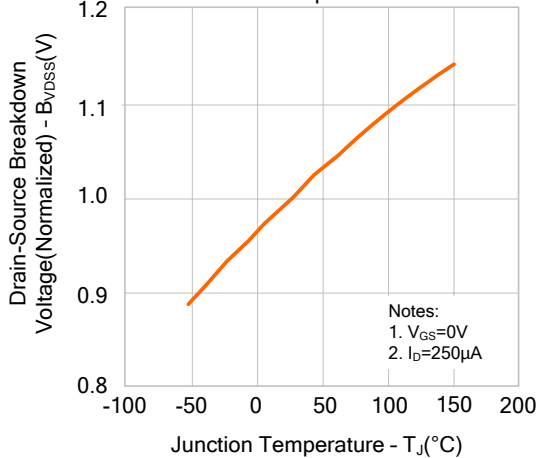


Figure 8. On-resistance Variation vs. Temperature

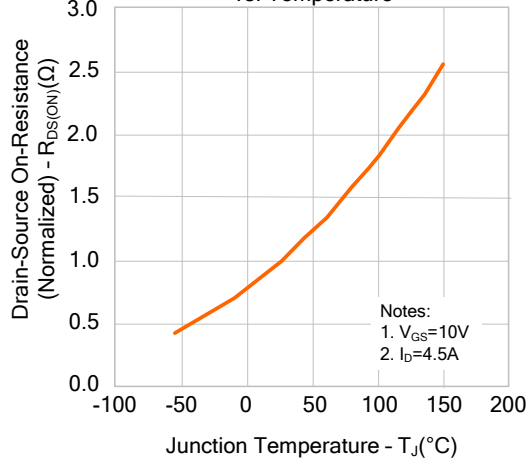


Figure 9. Max. Safe Operating Area

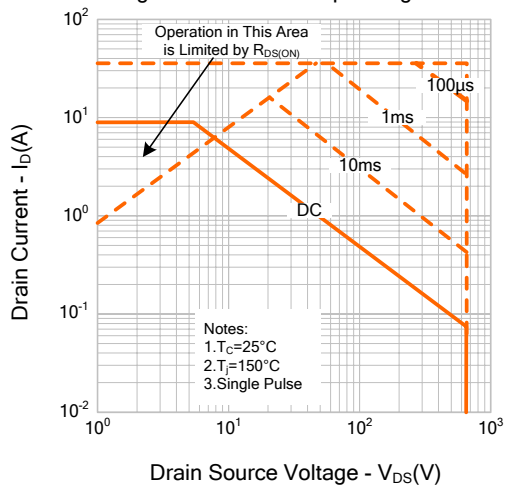
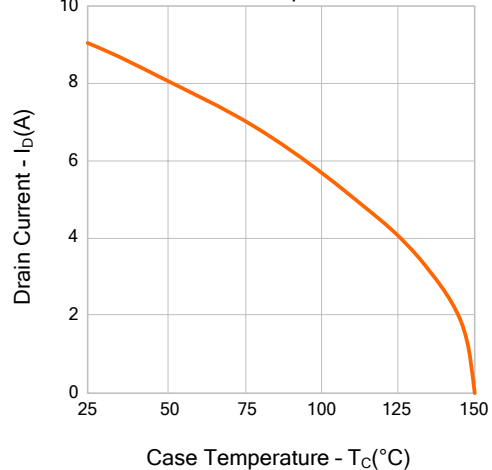
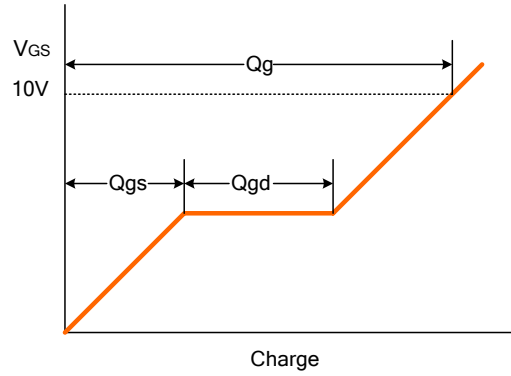
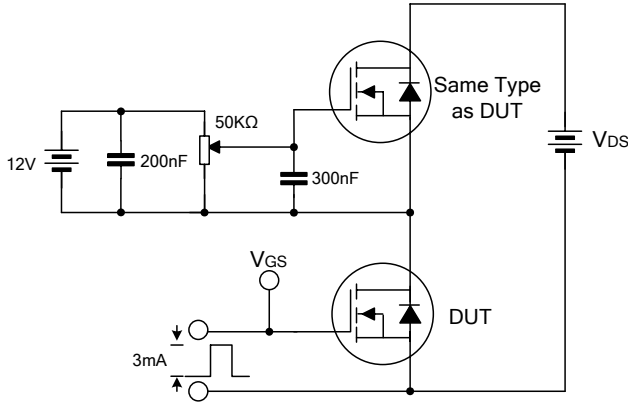


Figure 10. Maximum Drain Current vs. Case Temperature

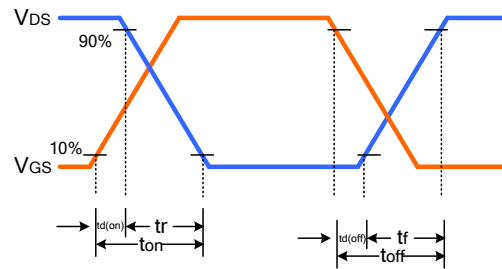
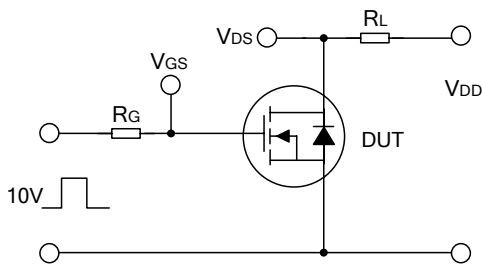


TYPICAL TEST CIRCUIT

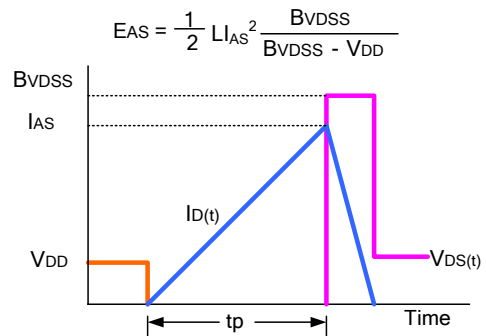
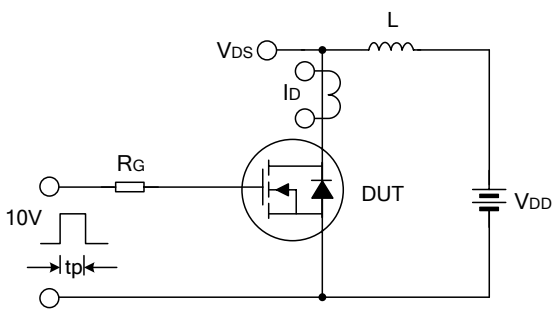
Gate Charge Test Circuit & Waveform



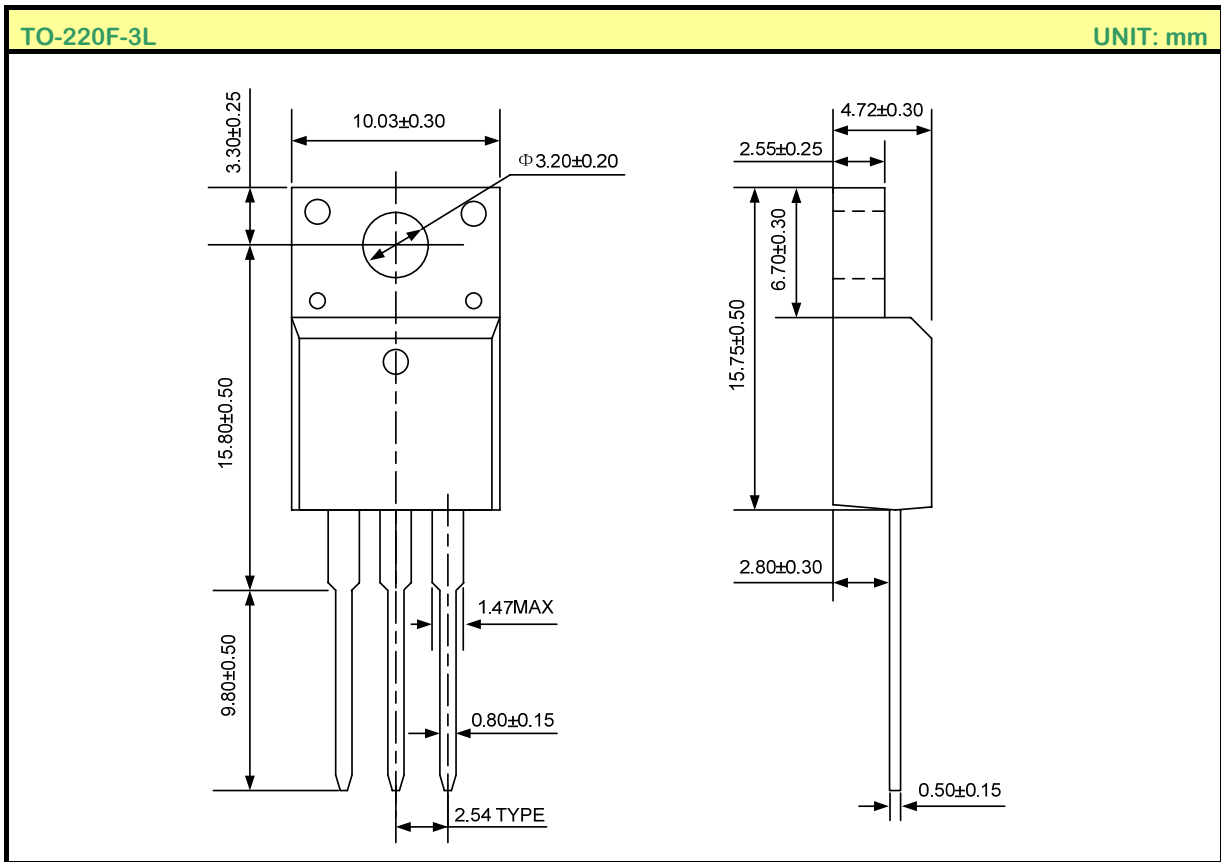
Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE



Disclaimer:

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without further notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
- All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.
- Silan will supply the best possible product for customers!

ATTACHMENT**Revision History**

Date	REV	Description	Page
2012.04.13	1.0	Initial release	
2012.06.15	1.1	Modify the typ. value of $R_{DS(on)}$	