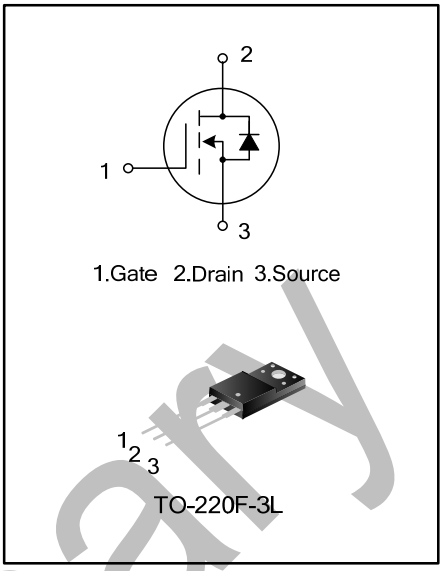
9A, 800V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF9NE80F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 9A,800V,$R_{DS(on)(typ.)}$=0.78Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

NOMENCLATURE

S V F X N E X X X

- Silan VDMOS Code of F-Cell process
- Nominal current,using 1 or 2 digits:
  Example:4 denotes 4A,
  10 denotes 10A,
  08 denotes 0.8A
- N denotes N Channel
- Special Features indication, May be omitted.
  Example: E denotes embeded ESD structure
- Nominal Voltage,using 2 digits
  Example: 70 denotes 700V,
- Package information.
  Example:F:TO-220F.

ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVF9NE80F	TO-220F-3L	SVF9NE80F	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	800	V
Gate-Source Voltage	V_{GS}	±30	V
Drain Current	I_D	9	A
Drain Current Pulsed	I_{DM}	36	A
Power Dissipation(T_C=25°C)	P_D	40	W
-Derate above 25°C		0.32	W/°C
Single Pulsed Avalanche Energy (Note 1)	E_{AS}	320	mJ
Operation Junction Temperature Range	T_J	-55～+150	°C
Storage Temperature Range	T_{stg}	-55～+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Rating	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.1	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	120	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250μA	800	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=800V, V_{GS}=0V	--	--	10	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	μA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= VDS, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=4.5A	--	0.78	0.9	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ	--	2340	--	pF
Output Capacitance	C_{oss}		--	260	--	
Reverse Transfer Capacitance	C_{rss}		--	45	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=400V,I_D=9.0A, R_G=25Ω (Note 2,3)	--	39	--	ns
Turn-on Rise Time	t_r		--	25	--	
Turn-off Delay Time	$t_{d(off)}$		--	74	--	
Turn-off Fall Time	t_f		--	21	--	
Total Gate Charge	Q_g	V_{DS}=640V,I_D=9.0A, V_{GS}=10V (Note 2,3)	--	85	--	nC
Gate-Source Charge	Q_{gs}		--	15	--	
Gate-Drain Charge	Q_{gd}		--	42	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

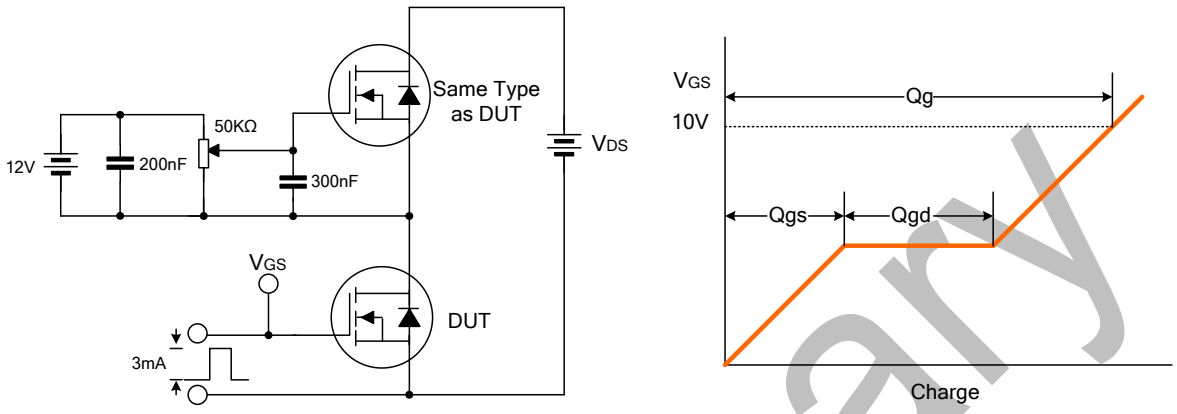
Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	9	A
Pulsed Source Current	I_{SM}		--	--	36	
Diode Forward Voltage	V_{SD}	I_S=9.0A,V_{GS}=0V	--	--	1.5	V
Reverse Recovery Time	T_{rr}	I_S=9.0A,V_{GS}=0V, dI_F/dt=100A/μs	--	660	--	ns
Reverse Recovery Charge	Q_{rr}		--	7.0	--	μC

Notes:

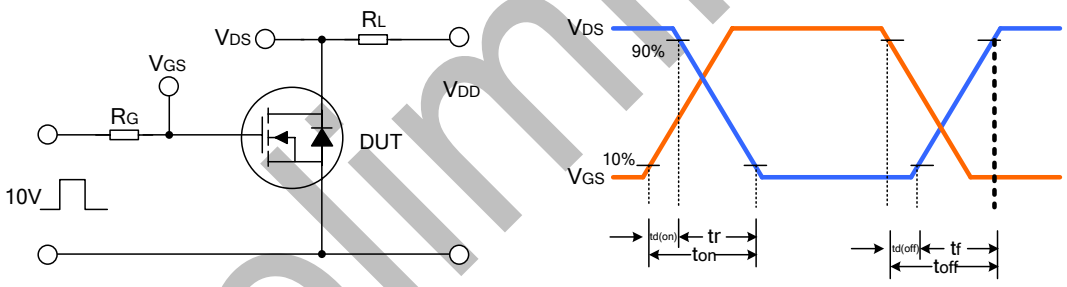
1. L=30 mH, I_{AS}=9.0A, V_{DD}=195V, R_G=25Ω,starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL TEST CIRCUIT

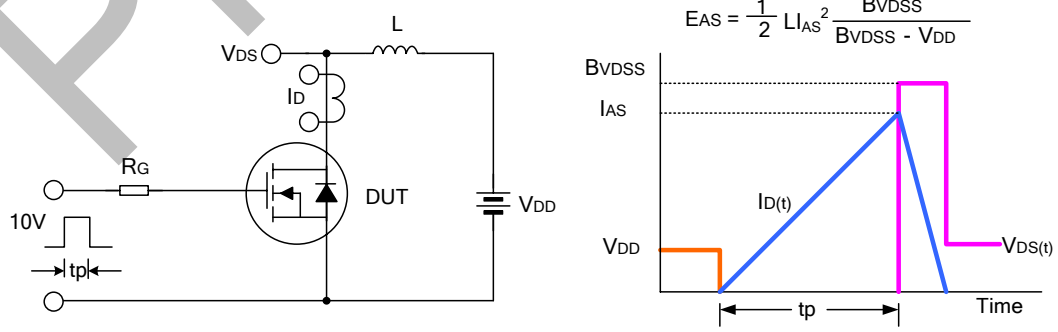
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

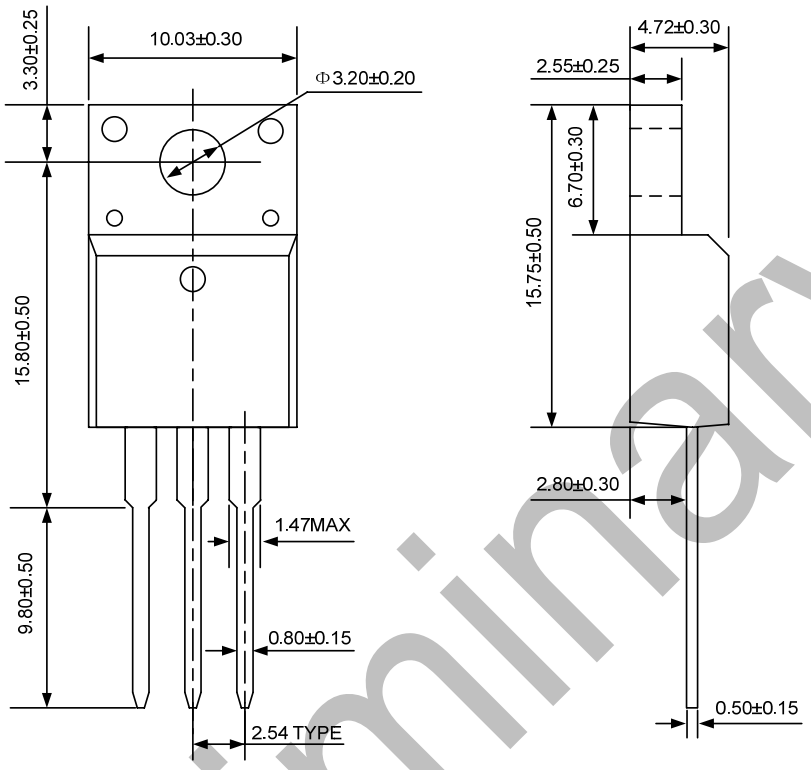


Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220F-3L UNIT: mm



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