

10A, 600V N-CHANNEL MOSFET

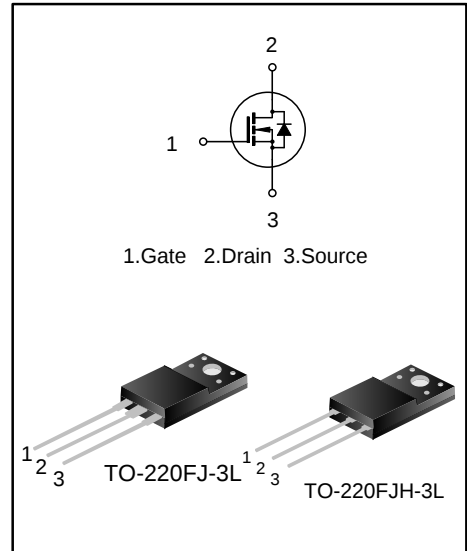
GENERAL DESCRIPTION

SVFP10N60CAFJ/FJH is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- 10A, 600V, $R_{DS(on)}(typ.)=0.60\Omega@V_{GS}=10V$
- Low gate charge
- Low C_{rss}
- Fast switching
- Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVFP10N60CAFJ	TO-220FJ-3L	P10N60CAFJ	Halogen free	Tube
SVFP10N60CAFJH	TO-220FJH-3L	P10N60CA	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (T_A=25°C UNLESS OTHERWISE NOTED)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V _{DS}	600	V
Gate-Source Voltage		V _{GS}	±30	V
Drain Current	T _C = 25°C	I _D	10	A
	T _C = 100°C		6.3	
Drain Current Pulsed		I _{DM}	40	A
Power Dissipation(T _C =25°C) -Derate above 25°C		P _D	45	W
			0.36	W/°C
Single Pulsed Avalanche Energy (Note 1)		E _{AS}	750	mJ
Reverse diode dv/dt (Note 2)		dv/dt	4.5	V/ns
MOSFET dv/dt ruggedness (Note 3)		dv/dt	50	V/ns
Operation Junction Temperature Range		T _J	-55~+150	°C
Storage Temperature Range		T _{stg}	-55~+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	R _{θJC}	2.78	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_J=25°C UNLESS OTHERWISE NOTED)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	600	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =600V, V _{GS} =0V	--	--	1	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D =250μA	2	--	4	V
Static Drain-Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =5.0A	--	0.60	0.75	Ω
		T _J =25°C T _J =125°C	--	1.27	--	
Gate resistance	R _g	f=1.0MHz	--	4.5	--	Ω
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	--	1300	--	pF
Output Capacitance	C _{oss}		--	150	--	
Reverse Transfer Capacitance	C _{rss}		--	14	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =300V, I _D =10A, R _G =25Ω (Note 4,5)	--	23	--	ns
Turn-on Rise Time	t _r		--	42	--	
Turn-off Delay Time	t _{d(off)}		--	67	--	
Turn-off Fall Time	t _f		--	36	--	
Total Gate Charge	Q _g	V _{DS} =480V, I _D =10A, V _{GS} =10V (Note 4,5)	--	34	--	nC
Gate-Source Charge	Q _{gs}		--	7.3	--	
Gate-Drain Charge	Q _{gd}		--	15	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction	--	--	10	A
Pulsed Source Current	I_{SM}	Diode In The MOSFET	--	--	40	
Diode Forward Voltage	V_{SD}	$I_S=10A, V_{GS}=0V$	--	--	1.2	V
Reverse Recovery Time	T_{rr}	$I_S=10A, V_{GS}=0V,$	--	530	--	ns
Reverse Recovery Charge	Q_{rr}	$dI/dt=100A/\mu s$ (Note4)	--	4.80	--	μC

Notes:

1. $L=30mH, I_{AS}=6.0A, V_{DD}=100V, R_G=25\Omega$, starting $T_J=25^\circ C$;
2. $V_{DS}=0\sim 400V, I_{SD}\leq 12A, T_J=25^\circ C$;
3. $V_{DS}=0\sim 480V$;
4. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

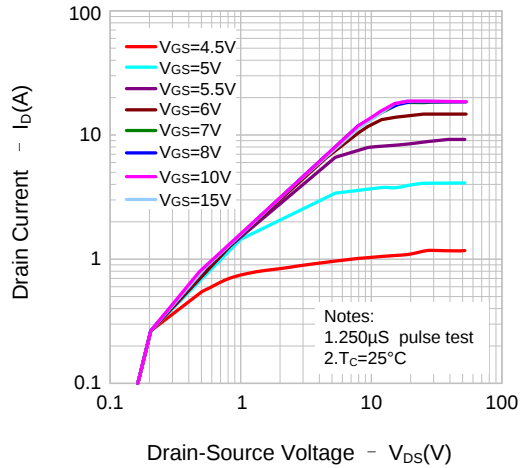


Figure 2. Transfer Characteristics

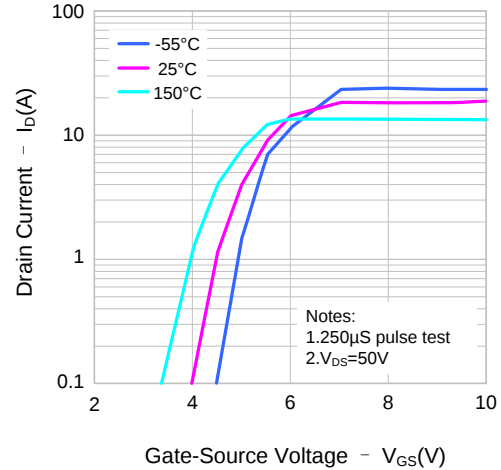


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

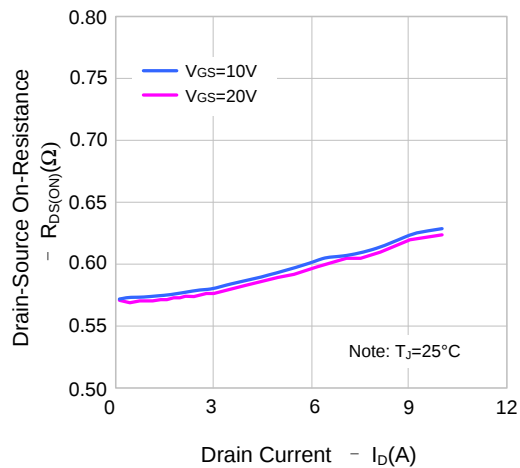


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

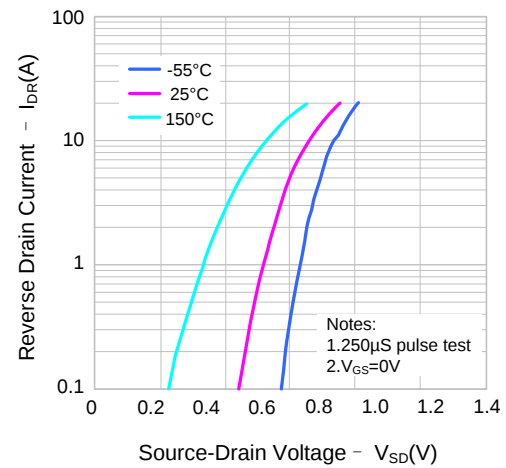


Figure 5. Capacitance Characteristics

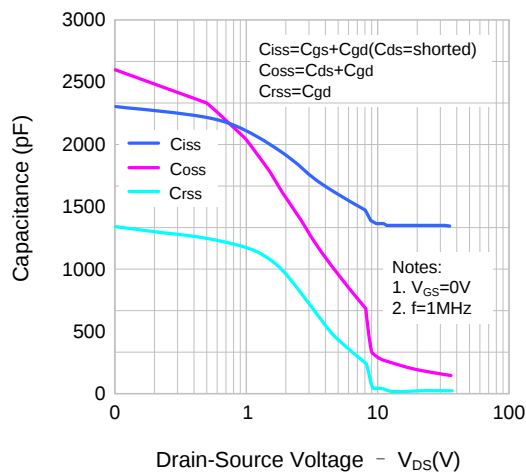
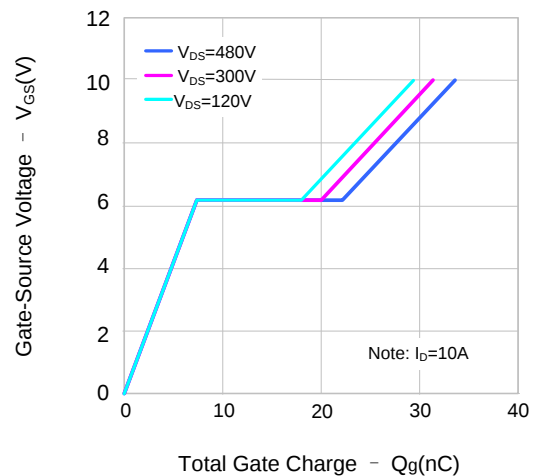


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS (CONTINUED)

Figure 7. Breakdown Voltage vs. Temperature

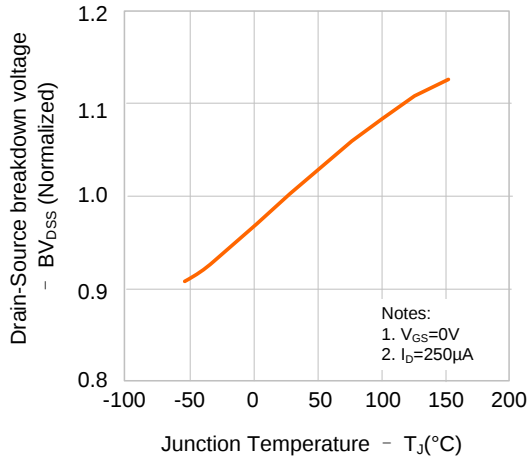


Figure 8. On-resistance Variation vs. Temperature

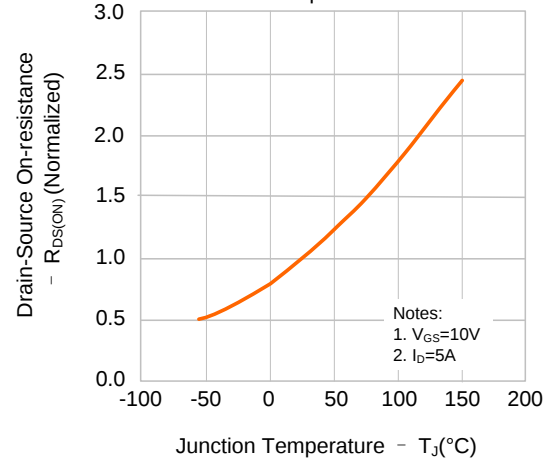


Figure 9. Max. Safe Operating Area

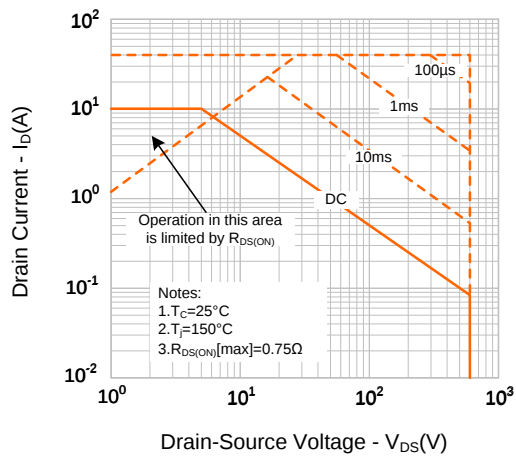
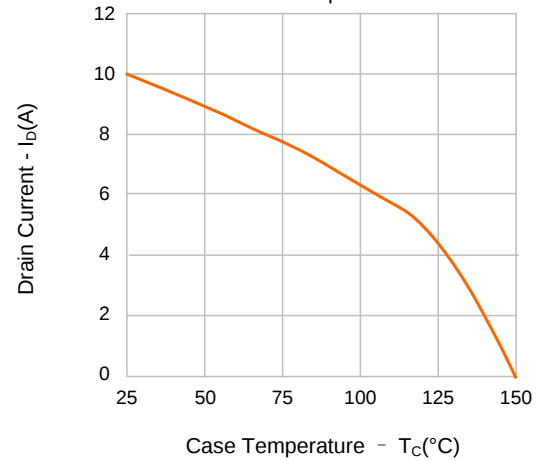
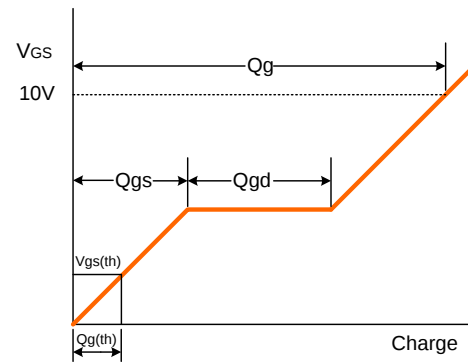
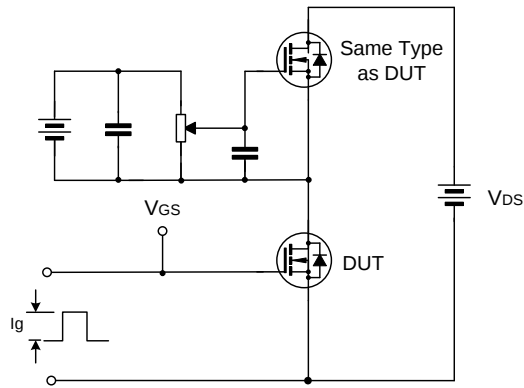


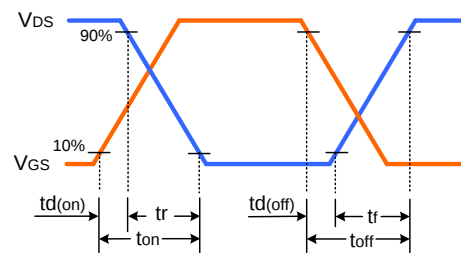
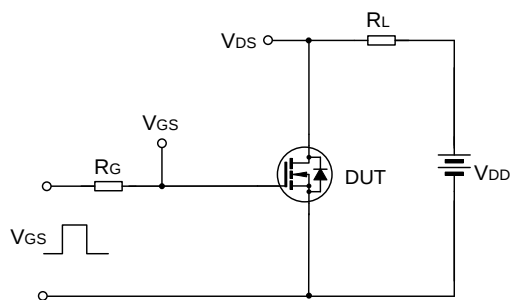
Figure 10. Max. Drain Current vs. Case Temperature



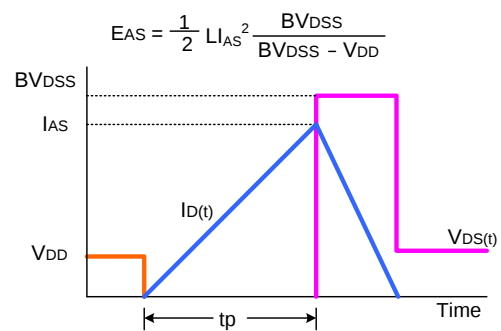
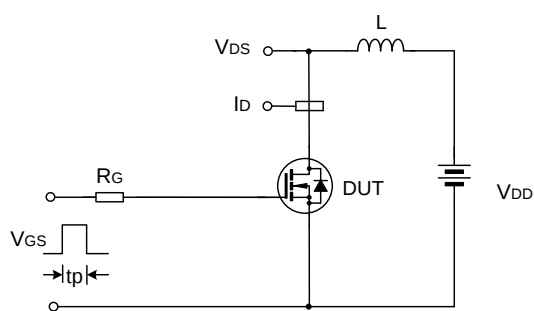
TYPICAL TEST CIRCUIT



Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

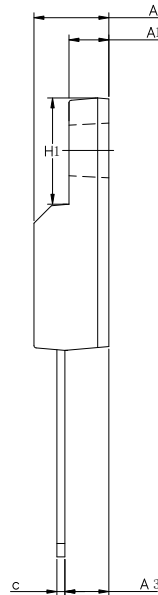
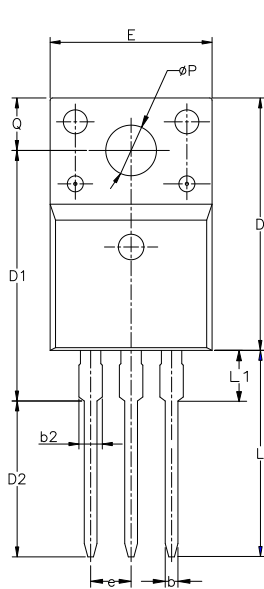


Unclamped Inductive Switching Test Circuit & Waveform

PACKAGE OUTLINE

TO-220FJ-3L

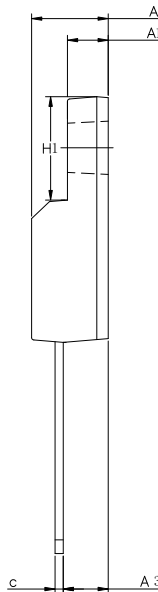
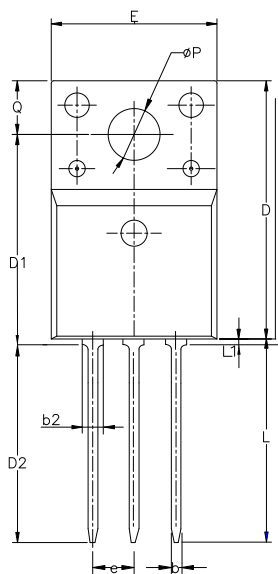
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.85
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	13.97	14.47	14.97
D2	10.58	11.08	11.58
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	2.00
ØP	3.00	3.18	3.40
Q	3.05	3.30	3.55

TO-220FJH-3L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.80
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	12.87	13.07	13.27
D2	12.28	12.48	12.68
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	0.85
ØP	3.00	3.18	3.40
Q	3.05	3.30	3.55

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Rev.: 1.3

Revision History:

1. Motify Electrical schematic and TYPICAL TEST CIRCUIT

Rev.: 1.2

Revision History:

1. Add TO-220FJH-3L

Rev.: 1.1

Revision History:

1. Modify I_{DSS} and V_{SD}

Rev.: 1.0

Revision History:

1. First Release
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