

7A, 650V N-CHANNEL MOSFET

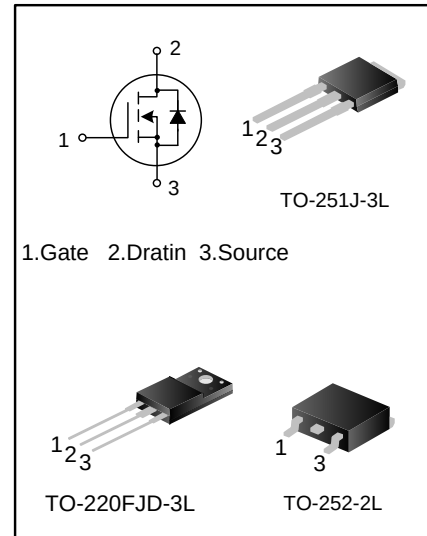
GENERAL DESCRIPTION

SVFP7N65CFJD/D/MJ is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

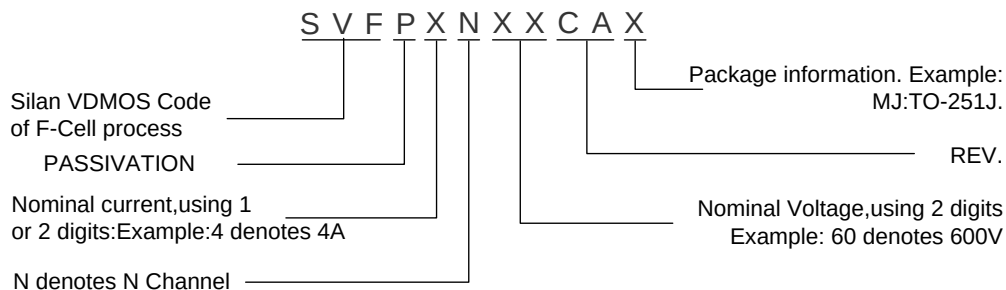
These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- 7A, 650V, $R_{DS(on)}(typ.)=1.1\Omega@V_{GS}=10V$
- Low gate charge
- Low C_{rss}
- Fast switching
- Improved dv/dt capability



NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVFP7N65CFJD	TO-220FJD-3L	P7N65CFJD	Halogen free	Tube
SVFP7N65CDTR	TO-252-2L	P7N65CD	Halogen free	Tape & Reel
SVFP7N65CMJ	TO-251J-3L	P7N65CMJ	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics		Symbol	Ratings		Unit
			SVFP7N65CFJD	SVFP7N65CD/CMJ	
Drain-Source Voltage		V _{DS}	650		V
Gate-Source Voltage		V _{GS}	±30		V
Drain Current	T _C = 25°C	I _D	7.0		A
	T _C = 100°C		4.4		
Drain Current Pulsed		I _{DM}	28		A
Power Dissipation(T _C =25°C) -Derate above 25°C		P _D	46	89	W
			0.37	0.71	W/°C
Single Pulsed Avalanche Energy (Note 1)		E _{AS}	435		mJ
Reverse Diode dv/dt (Note 2)		dv/dt	4.5		V/ns
MOSFET dv/dt Ruggedness (Note 3)		dv/dt	50		V/ns
Operation Junction Temperature Range		T _J	-55~+150		°C
Storage Temperature Range		T _{stg}	-55~+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVFP7N65CFJD	SVFP7N65CD/CMJ	
Thermal Resistance, Junction-to-Case	R _{θJC}	2.7	1.4	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	62.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	650	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =650V, V _{GS} =0V	--	--	1.0	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =3.5A	--	1.1	1.4	Ω
Input Capacitance	R _g	f=1.0MHz	--	2.8	--	Ω
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	--	789	--	pF
Output Capacitance	C _{oss}		--	98	--	
Reverse Transfer Capacitance	C _{rss}		--	9.0	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =32V, R _G =25Ω, I _D =7.0A (Note 2,3)	--	15	--	ns
Turn-on Rise Time	t _r		--	32	--	
Turn-off Delay Time	t _{d(off)}		--	51	--	
Turn-off Fall Time	t _f		--	33	--	
Total Gate Charge	Q _g	V _{DS} =520V, I _D =7.0A, V _{GS} =10V (Note 2,3)	--	21	--	nC
Gate-Source Charge	Q _{gs}		--	4.5	--	
Gate-Drain Charge	Q _{gd}		--	10	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I _S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	7.0	A
Pulsed Source Current	I _{SM}		--	--	28	
Diode Forward Voltage	V _{SD}	I _S =7.0A, V _{GS} =0V	--	--	1.4	V
Reverse Recovery Time	T _{rr}	I _S =7.0A, V _{GS} =0V, dI _F /dt=100A/μS (Note 2)	--	499	--	ns
Reverse Recovery Charge	Q _{rr}		--	3.0	--	μC

Notes:

1. L=30mH, I_{AS}=5.0A, V_{DD}=100V, R_G=25Ω, starting temperature T_J=25°C;
2. V_{DS}=0~400V, I_{SD}≤7A, T_J=25°C;
3. V_{DS}=0~480V;
4. Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

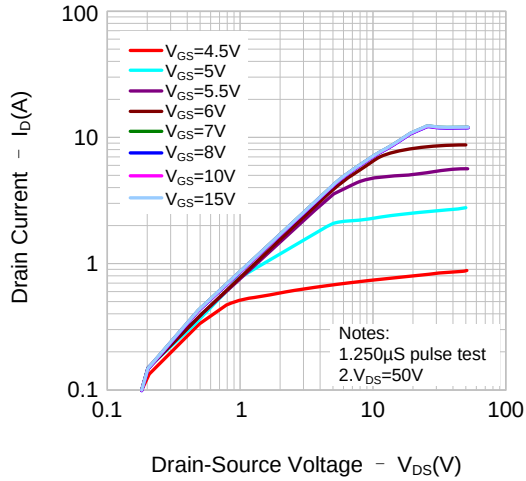


Figure 2. Transfer Characteristics

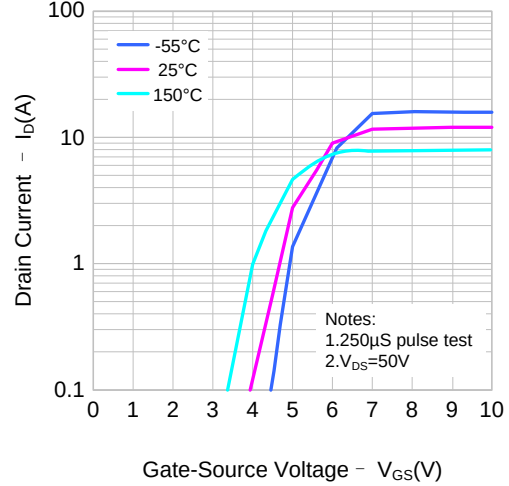


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

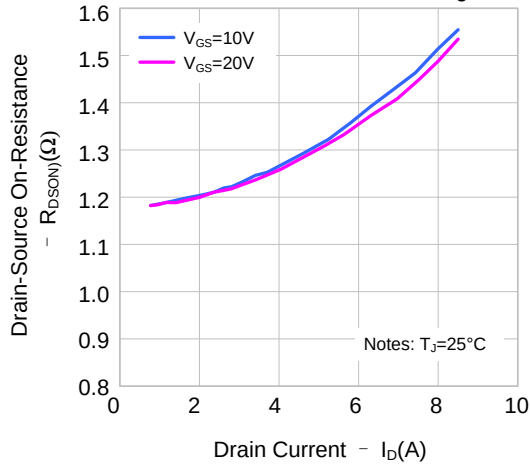


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

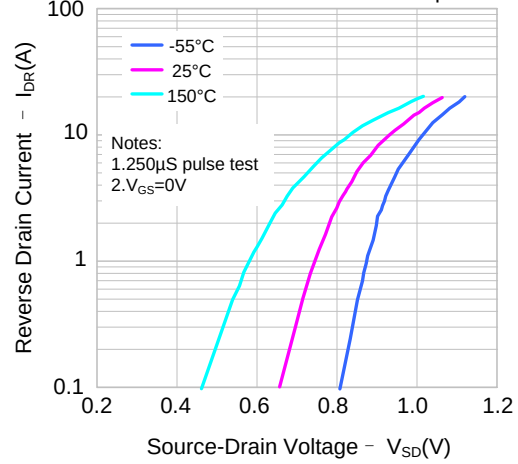


Figure 5. Capacitance Characteristics

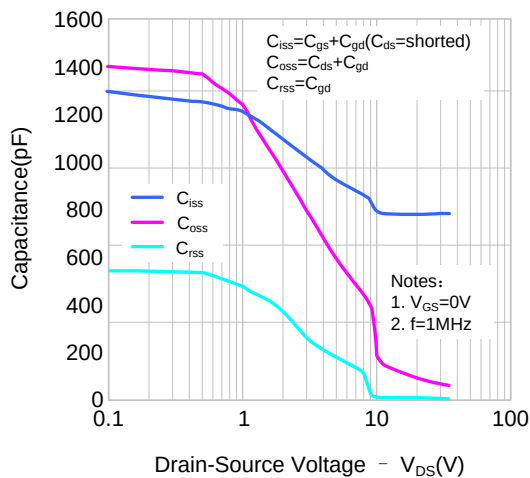
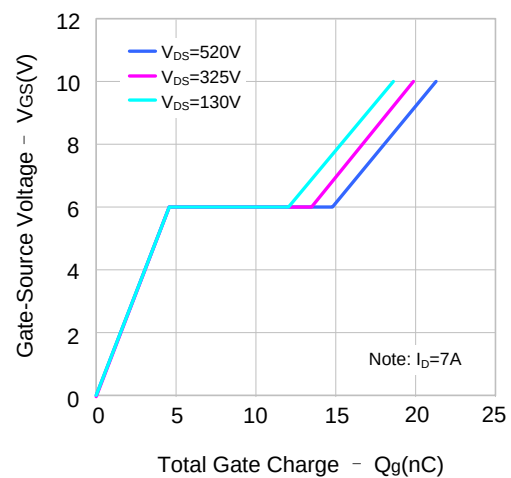


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS (continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

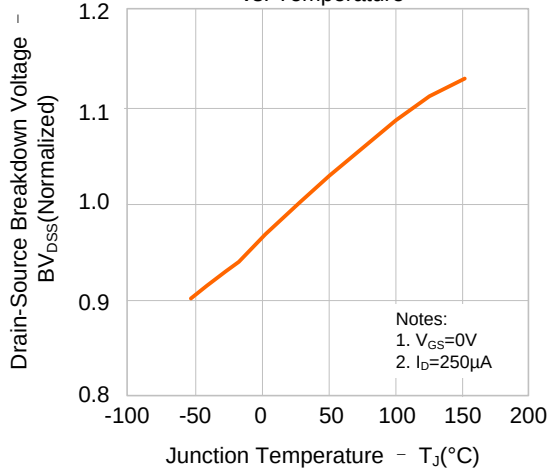


Figure 8. On-resistance Variation vs. Temperature

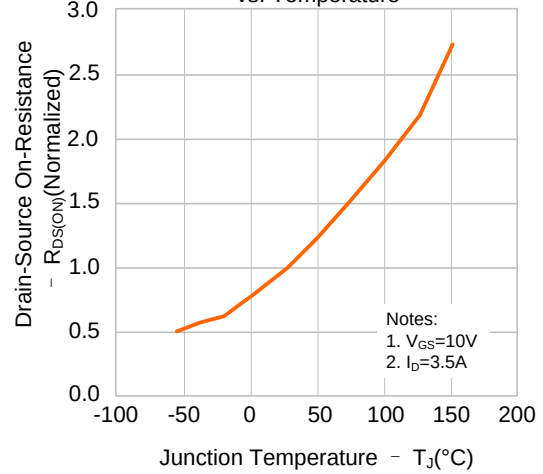


Figure 9-1. Max. Safe Operating Area(SVFP7N65CFJD)

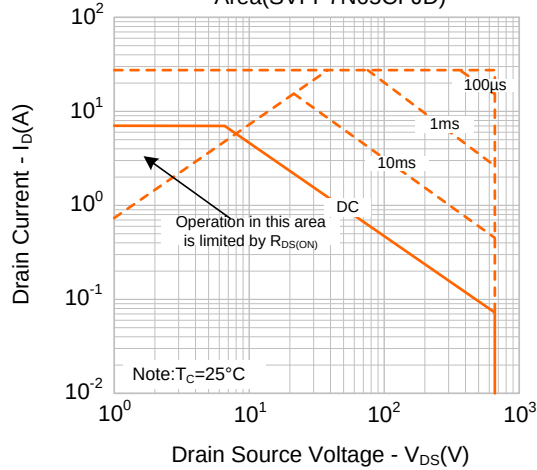


Figure 9-2. Max. Safe Operating Area(SVFP7N65CD)

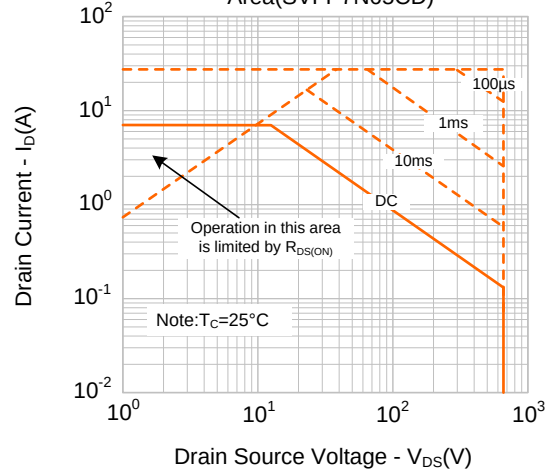
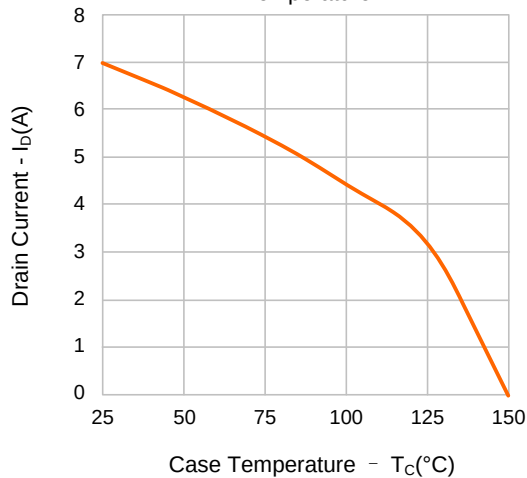
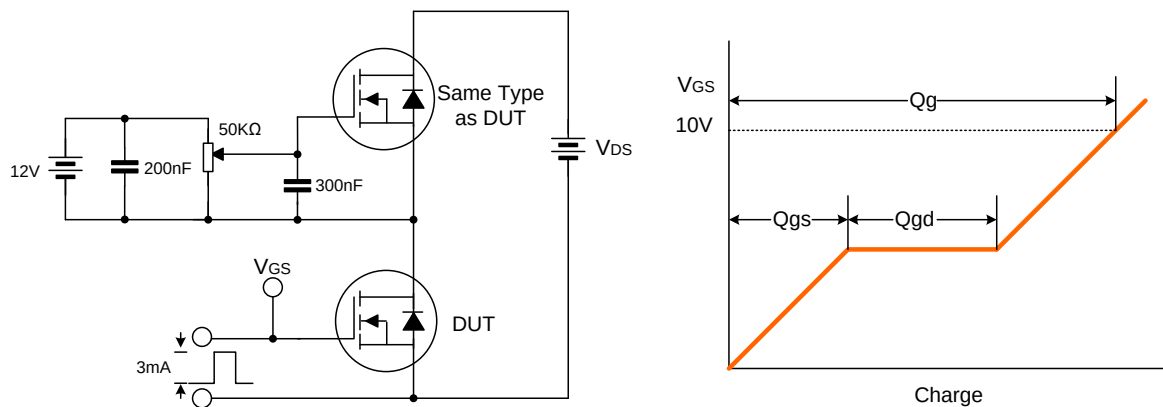


Figure 10. Max. Drain Current vs. Case Temperature

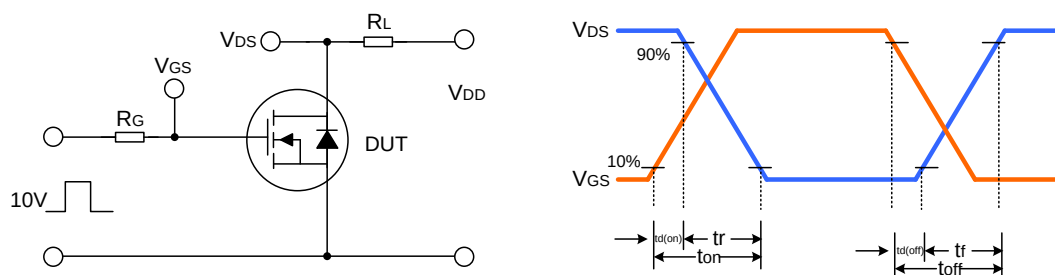


TYPICAL TEST CIRCUIT

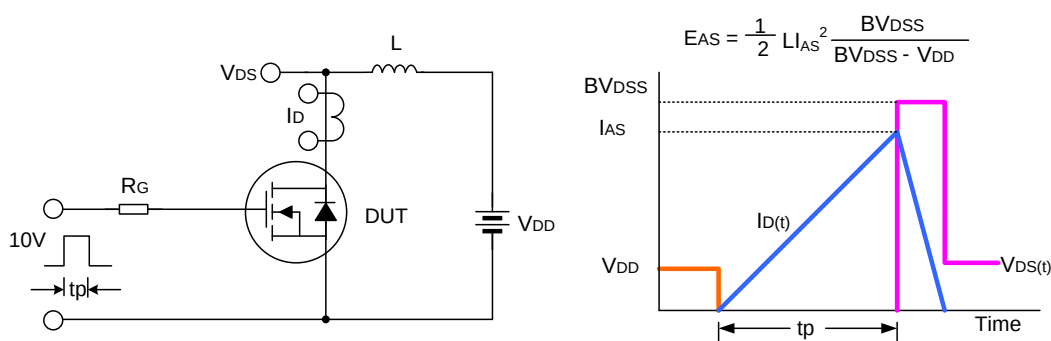
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



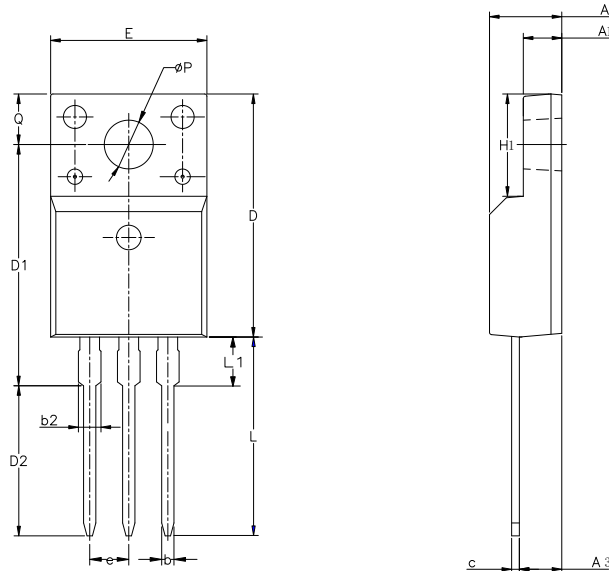
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220FJD-3L

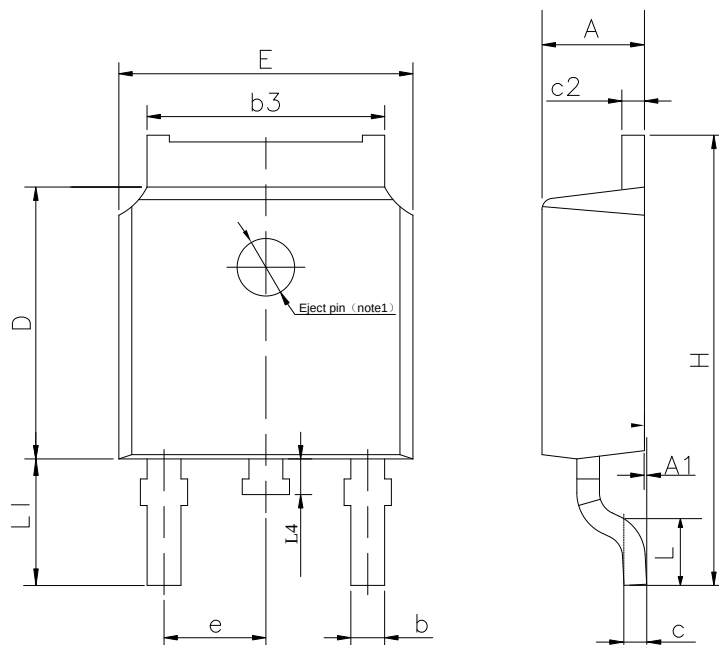
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.85
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	13.97	14.47	14.97
D2	10.58	11.08	11.58
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	2.00
ØP	3.00	3.18	3.40
Q	3.05	3.30	3.55

TO-252-2L

UNIT: mm



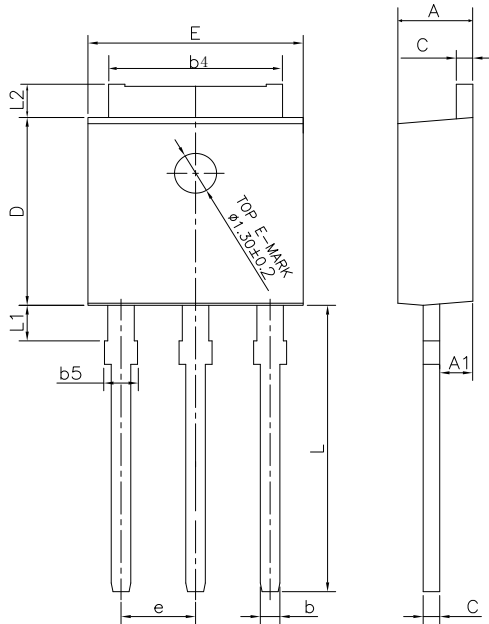
SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	—	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	—	0.65
c2	0.45	—	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

PACKAGE OUTLINE

TO-251J-3L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	2.18	2.30	2.39
A1	0.89	1.00	1.14
b	0.56	---	0.89
b4	4.95	5.33	5.46
b5	---	---	1.05
c	0.46	---	0.61
D	5.97	6.10	6.27
E	6.35	6.60	6.73
e	2.29 BCS		
L	8.89	9.30	9.65
L1	0.95	---	1.50
L2	0.89	---	1.27

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Part No.:	SVFP7N65CFJD/D/MJ	Document Type:	Datasheet
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Rev.: 1.2
Revision History:
1. Add TO-251J-3L

Rev.: 1.1
Revision History:
1. Add TO-252-2L

Rev.: 1.0
Revision History:
1. First release
