

100A, 70V N-CHANNEL MOSFET

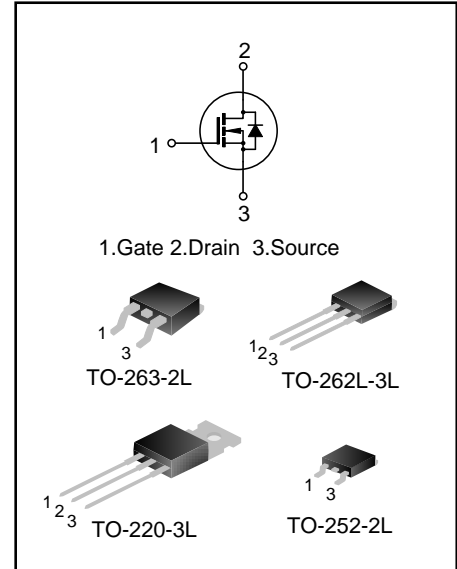
DESCRIPTION

SVG076R5NT(S)(D)(KL) is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance.

This device is widely used in UPS, Power Management for Inverter Systems.

FEATURES

- ◆ 100A, 70V, $R_{DS(on)(typ.)}=5.4m\Omega @ V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low C_{rss}
- ◆ Fast switching
- ◆ Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVG076R5NT	TO-220-3L	076R5NT	Pb free	Tube
SVG076R5NS	TO-263-2L	076R5NS	Halogen free	Tube
SVG076R5NSTR	TO-263-2L	076R5NS	Halogen free	Tape & Reel
SVG076R5NDTR	TO-252-2L	076R5ND	Halogen free	Tape & Reel
SVG076R5NKL	TO-262L-3L	076R5NKL	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, T_C=25°C)

Characteristics		Symbol	Ratings		Unit
			SVG076R5NT/NS/NKL	SVG076R5ND	
Drain-Source Voltage		V _{DS}	70		V
Gate-Source Voltage		V _{GS}	±20		V
Drain Current	T _C =25°C	I _D	100		A
	T _C =100°C		63		
Drain Current Pulsed		I _{DM}	400		A
Power Dissipation (T _C =25°C) -Derate above 25°C		P _D	114	96	W
			0.91	0.77	W/°C
Single Pulsed Avalanche Energy (Note 1)		E _{AS}	280		mJ
Operation Junction Temperature Range		T _J	-55~+150		°C
Storage Temperature Range		T _{stg}	-55~+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVG076R5NT/NS/NKL	SVG076R5ND	
Thermal Resistance, Junction-to-Case	R _{θJC}	1.1	1.3	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	62.0	°C/W

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, T_C=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	70	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =70V, V _{GS} =0V	--	--	1.0	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} =V _{DS} , I _D =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =40A	--	5.4	6.5	mΩ
Gate Resistance	R _G	f=1MHz	--	2.1	--	Ω
Input Capacitance	C _{iss}	f=1MHz, V _{GS} =0V, V _{DS} =35V	--	3052	--	pF
Output Capacitance	C _{oss}		--	479	--	
Reverse Transfer Capacitance	C _{rss}		--	24	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =35V, V _{GS} =10V, R _G =2.7Ω, I _D =40A (Note 2,3)	--	20	--	ns
Turn-on Rise Time	t _r		--	35	--	
Turn-off Delay Time	t _{d(off)}		--	37	--	
Turn-off Fall Time	t _f		--	12	--	
Total Gate Charge	Q _g	V _{DD} =56V, V _{GS} =10V, I _D =40A (Note 2,3)	--	50	--	nC
Gate-Source Charge	Q _{gs}		--	20	--	
Gate-Drain Charge	Q _{gd}		--	12	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction	--	--	100	A
Pulsed Source Current	I_{SM}	Diode in the MOSFET	--	--	400	
Diode Forward Voltage	V_{SD}	$I_S=40A$, $V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=40A$, $V_{GS}=0V$, $dI_F/dt=100A/\mu s$ (Note 2)	--	45	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.06	--	μC

Notes:

1. $L=0.5mH$, $I_{AS}=32A$, $V_{DD}=56V$, $R_G=25\Omega$, starting $T_J=25^\circ C$;
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. Output Characteristics

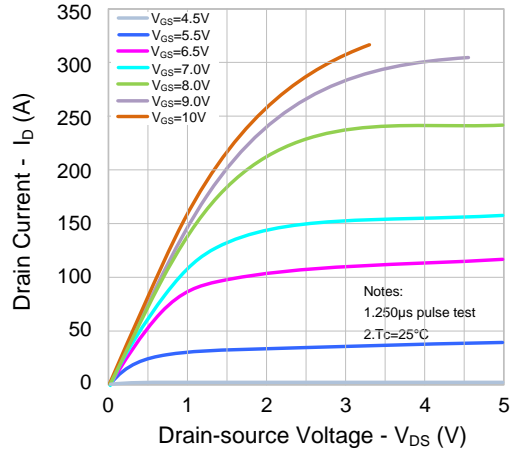


Figure 2. Transfer Characteristics

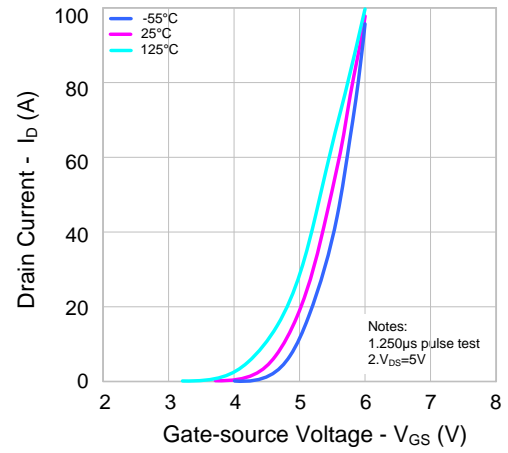


Figure 3. On-resistance vs. Drain Current

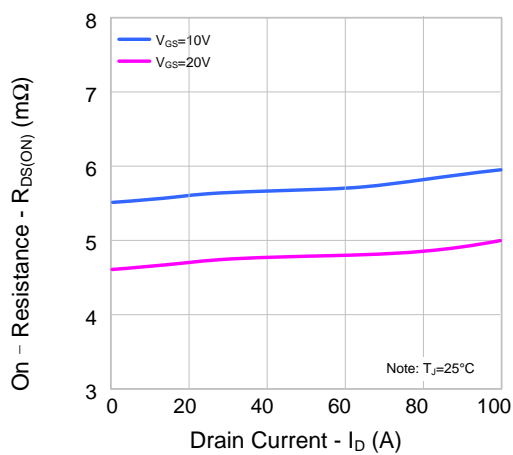


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

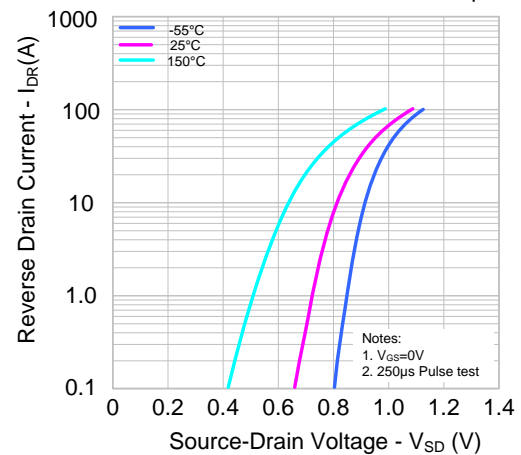


Figure 5. Capacitance Characteristics

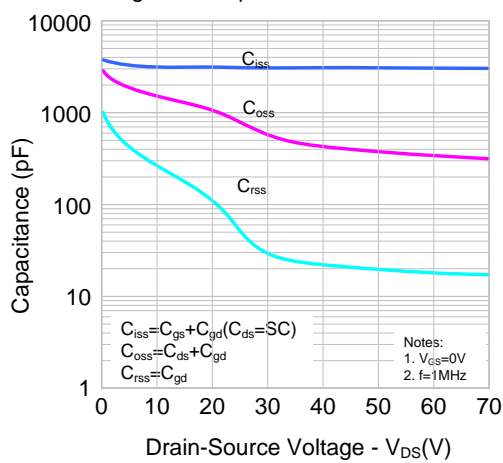
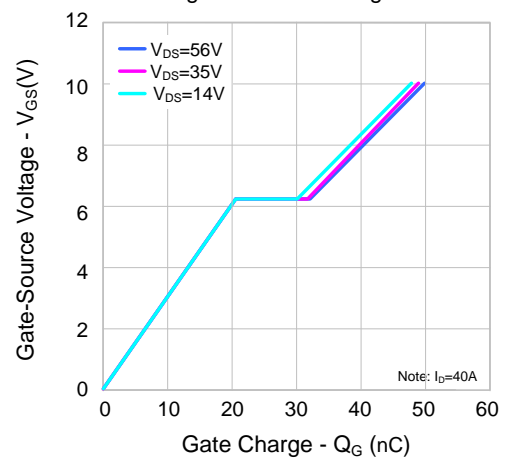
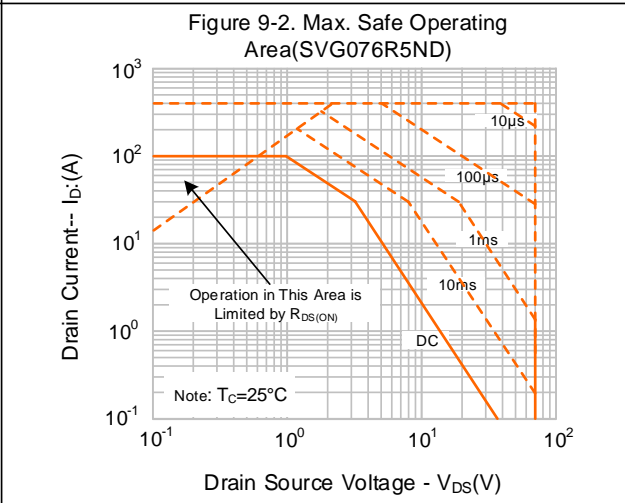
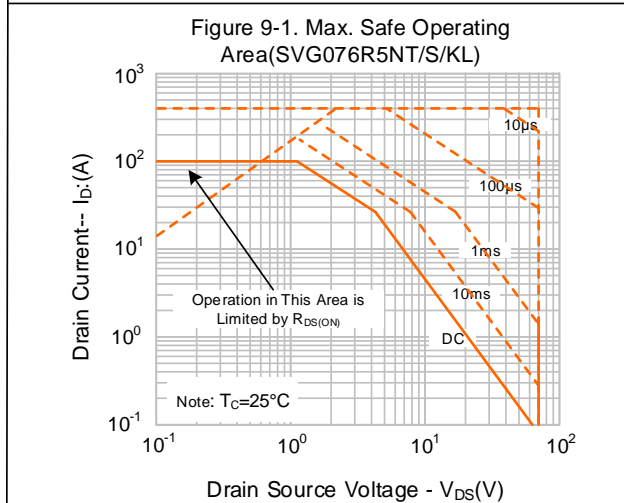
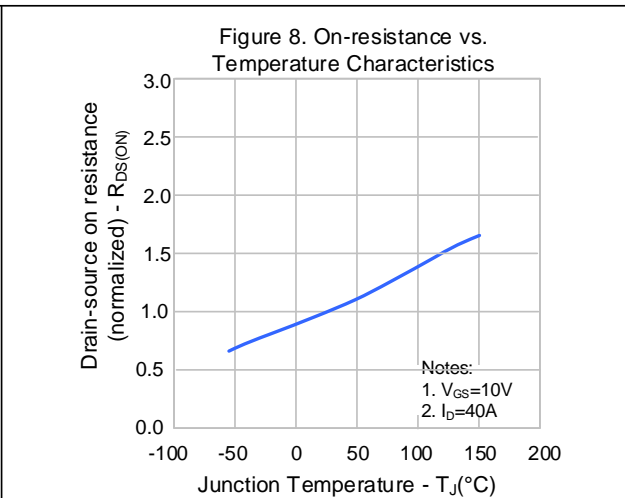
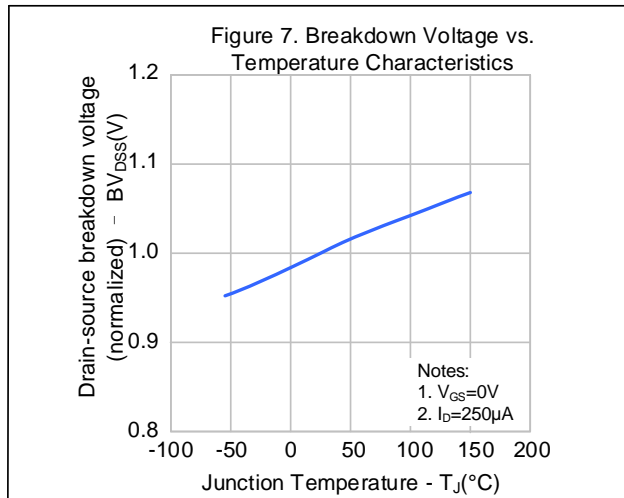


Figure 6. Gate Charge

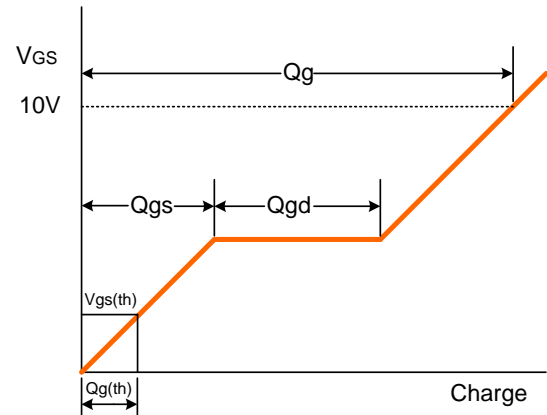
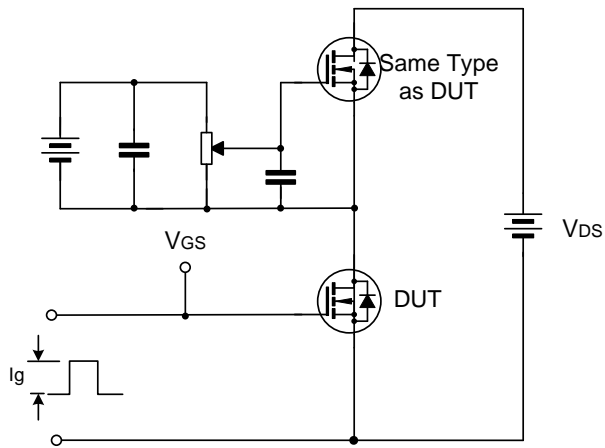


TYPICAL CHARACTERISTICS (CONTINUED)

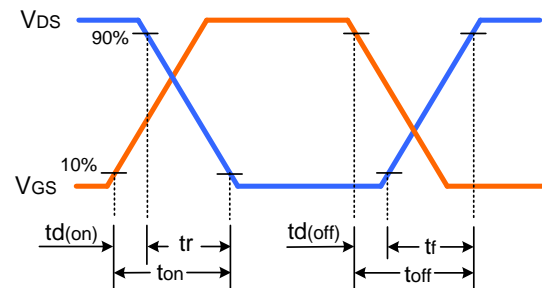
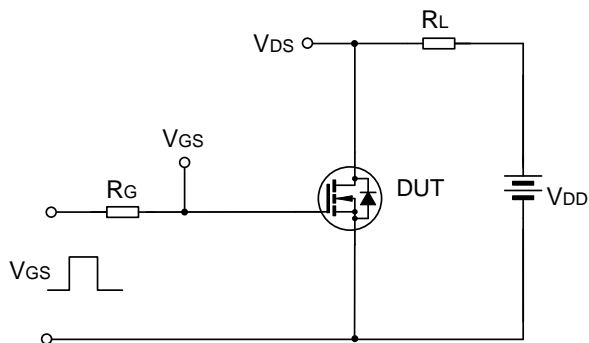


TYPICAL TEST CIRCUIT

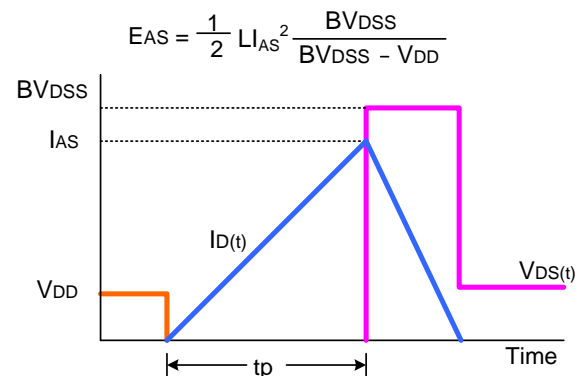
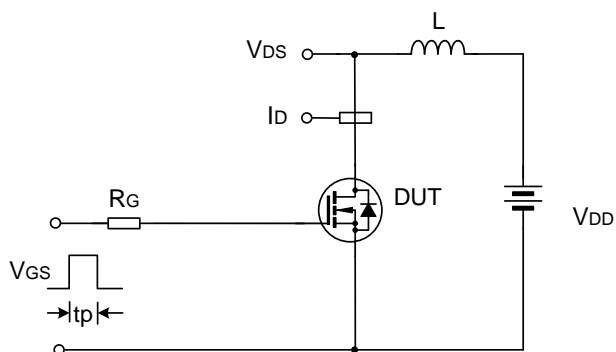
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



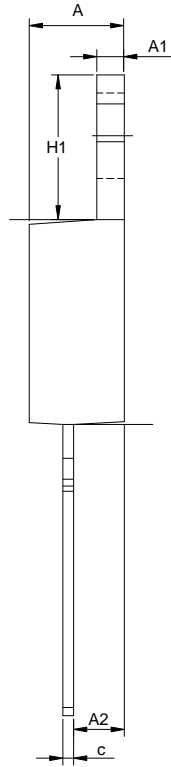
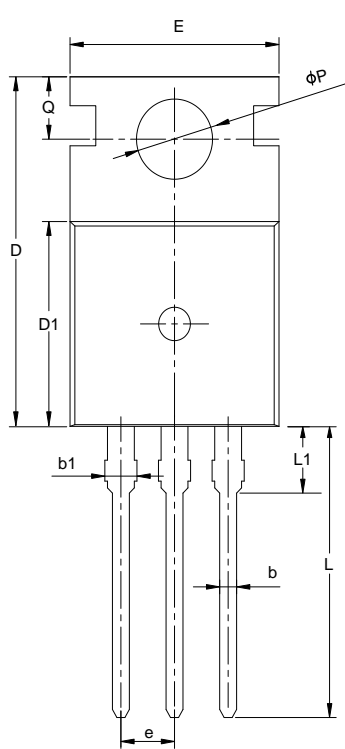
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220-3L

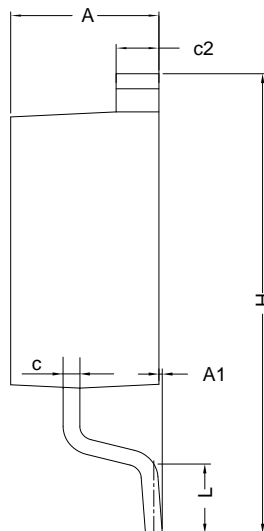
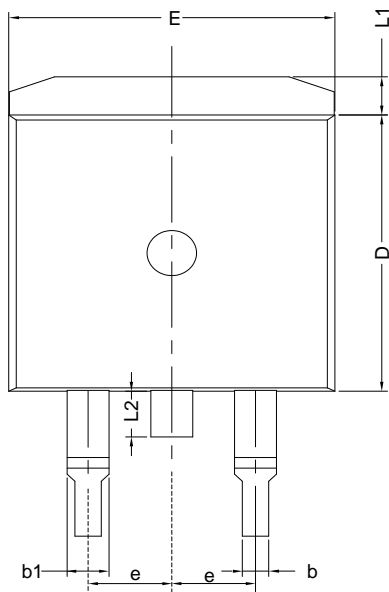
UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ΦP	3.40	3.70	3.90
Q	2.60	—	3.20

TO-263-2L

UNIT: mm

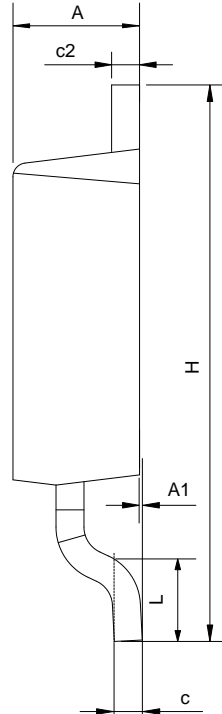
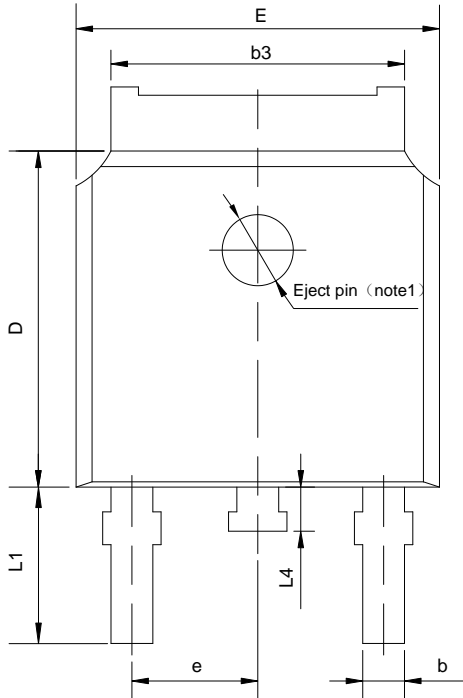


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
b1	1.17	—	1.50
c	0.30	—	0.60
c2	1.17	1.27	1.37
D	8.50	—	9.35
E	9.80	—	10.45
e	2.54BSC		
H	14.70	—	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	—	—	1.75

PACKAGE OUTLINE (CONTINUED)

TO-252-2L

UNIT: mm

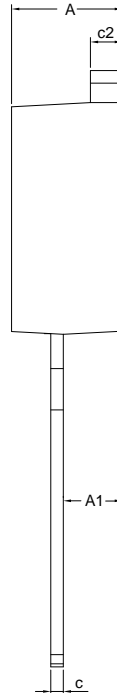
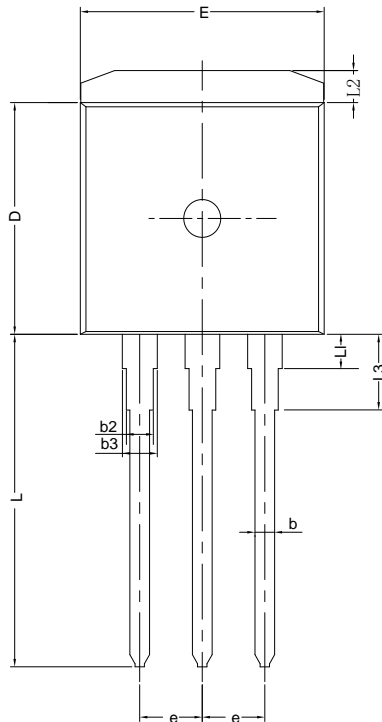


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	—	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	—	0.65
c2	0.45	—	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

TO-262L-3L

UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	2.20	—	2.92
b	0.71	0.80	0.88
b2	0.90	1.01	1.08
b3	1.20	—	1.50
c	0.34	—	0.76
c2	1.22	1.30	1.35
D	8.38	—	9.30
E	9.80	10.16	10.54
e	2.54 BSC		
L	12.80	—	14.10
L1	1.40	1.50	1.60
L2	1.12	—	1.42
L3	3.00	3.20	3.40

**MOS DEVICES OPERATE NOTES:**

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Important notice :

1. Silan reserves the right to make changes of this instruction without notice.
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Revision History:

1. Update typical characteristics
2. Update important notice

Rev.: **1.2**

Revision History:

1. Add package of SVG076R5NKL
2. Update typical test circuit and important notice
3. Delete nomenclature

Rev.: **1.1**

Revision History:

1. Add package outline of To-263-2L and To-252-2L
2. Modify electrical diagram and typical circuit diagram
3. Add SOA curve of SVG076R5ND

Rev.: **1.0**

Revision History:

1. First release