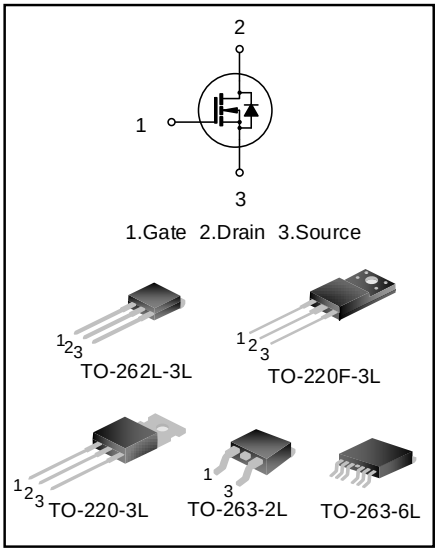
120A, 100V N-CHANNEL MOSFET

DESCRIPTION

SVG104R5NT(S)(F)(KL)(S6) is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance.

This device is widely used in UPS, Power Management for Inverter Systems.



FEATURES

- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVG104R5NT	TO-220-3L	104R5NT	Pb free	Tube
SVG104R5NS	TO-263-2L	104R5NS	Halogen free	Tube
SVG104R5NSTR	TO-263-2L	104R5NS	Halogen free	Tape&Reel
SVG104R5NF	TO-220F-3L	104R5NF	Pb free	Tube
SVG104R5NKL	TO-262L-3L	104R5NKL	Pb free	Tube
SVG104R5NS6	TO-263-6L	104R5NS6	Halogen free	Tube
SVG104R5NS6TR	TO-263-6L	104R5NS6	Halogen free	Tape&Reel

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, T_J=25°C)

Characteristics		Symbol	Ratings		Unit
			SVG104R5NT/S/KL/S6	SVG104R5NF	
Drain-Source Voltage		V_{DS}	100		V
Gate-Source Voltage		V_{GS}	±20		V
Drain Current	T_C=25°C	I_D	120		A
	T_C=100°C		110		
Drain Current Pulsed		I_{DM}	480		A
Power Dissipation(T_C=25°C)		P_D	208	38	W
-Derate above 25°C			1.7	0.3	W/°C
Single Pulsed Avalanche Energy (Note 1)	L=0.5mH	E_{AS}	780		mJ
	L=0.1mH		450		mJ
Operation Junction Temperature Range		T_J	-55~+150		°C
Storage Temperature Range		T_{stg}	-55~+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVG104R5NT/S/KL/S6	SVG104R5NF	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.6	3.3	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.0	°C/W

ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, T_J=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	100	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=50A (TO-220-3L) (TO-220F-3L) (TO-262L-3L)	--	3.6	4.5	mΩ
		V_{GS}=10V, I_D=50A (TO-263-2L)(TO-263-6L)	--	3.4	4.2	mΩ
Gate Resistance	R_G	f=1MHz	--	2.4	--	Ω
Input Capacitance	C_{iss}	f=1MHz, V_{GS}=0V, V_{DS}=50V	--	7266	--	pF
Output Capacitance	C_{oss}		--	864	--	
Reverse Transfer Capacitance	C_{rss}		--	24	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=50V, V_{GS}=10V, R_G=3Ω, I_D=50A (Note 2,3)	--	32	--	ns
Turn-on Rise Time	t_r		--	50	--	
Turn-off Delay Time	$t_{d(off)}$		--	83	--	
Turn-off Fall Time	t_f		--	31	--	
Total Gate Charge	Q_g	V_{DD}=50V, V_{GS}=10V, I_D=20A (Note 2,3)	--	114	--	nC
Gate-Source Charge	Q_{gs}		--	37	--	
Gate-Drain Charge	Q_{gd}		--	26	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	120	A
Pulsed Source Current	I_{SM}		--	--	480	
Diode Forward Voltage	V_{SD}	I_S=50A, V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=50A, V_{GS}=0V, dIF/dt=100A/μs (Note 2)	--	77	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.18	--	μC

Notes:

1.V_{DD}=80V, R_G=25Ω, starting T_J=25°C;

2.Pulse Test: Pulse width≤300μs,Duty cycle≤2%;

3.Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. Output Characteristics

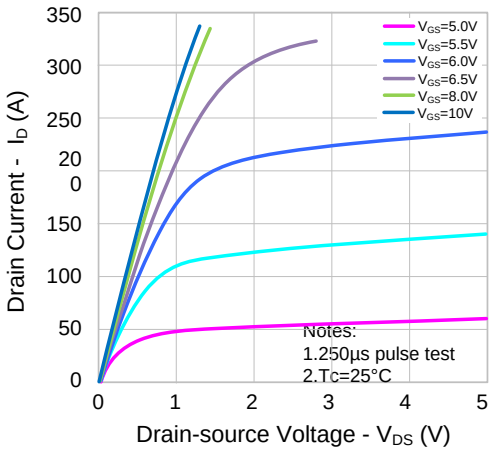


Figure 2. Transfer Characteristics

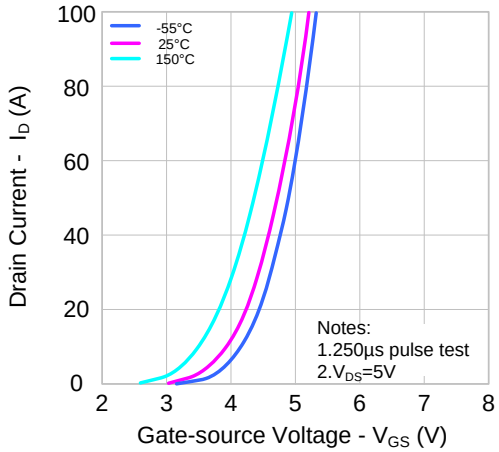


Figure 3. On-resistance vs. Drain Current

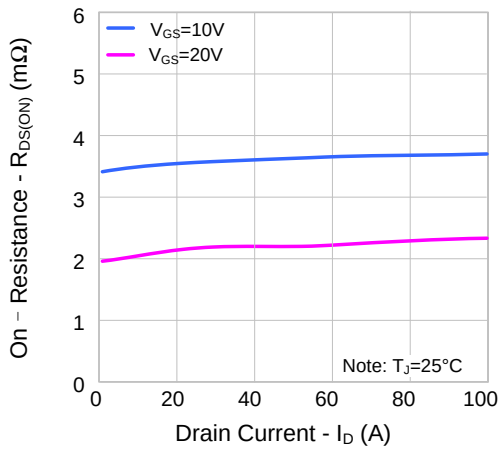


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

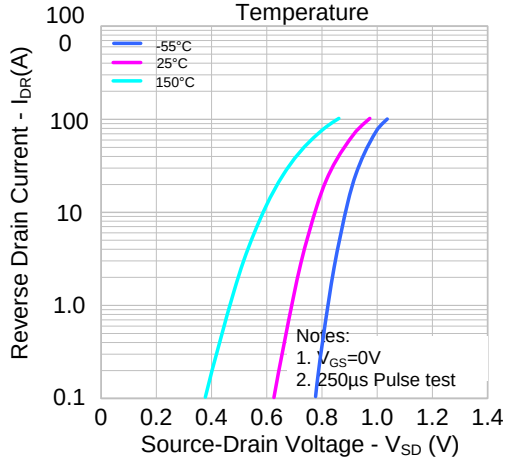


Figure 5. Capacitance Characteristics

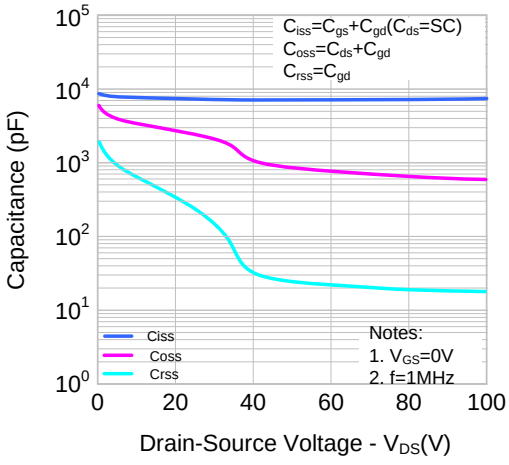
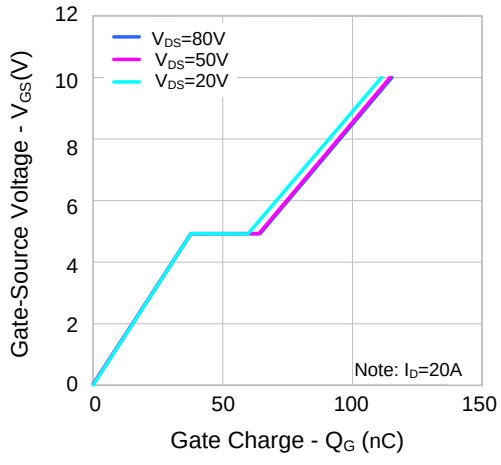


Figure 6. Gate Charge



TYPICAL CHARACTERISTICS (CONTINUED)

Figure 7. Breakdown Voltage vs. Temperature Characteristics

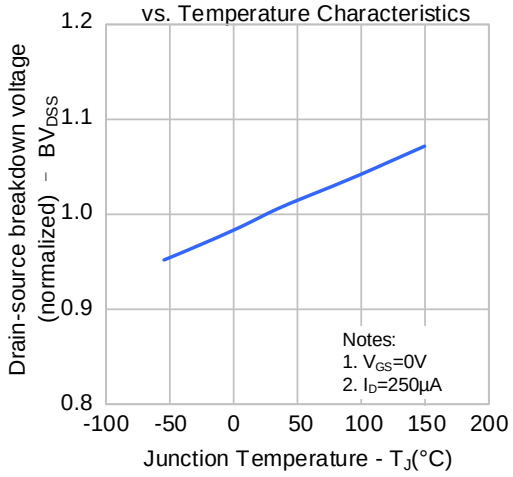


Figure 8. On-resistance vs. Temperature Characteristics

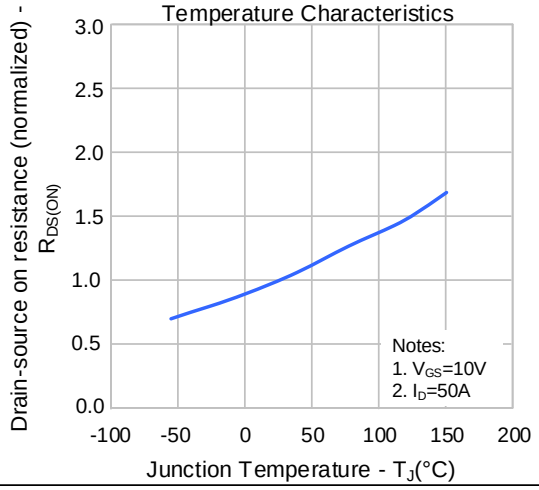


Figure 9-1. Max. Safe Operating Area (SVG104R5NT/S/KL/S6)

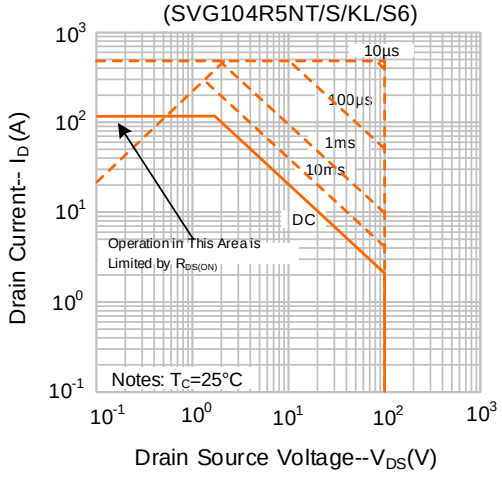
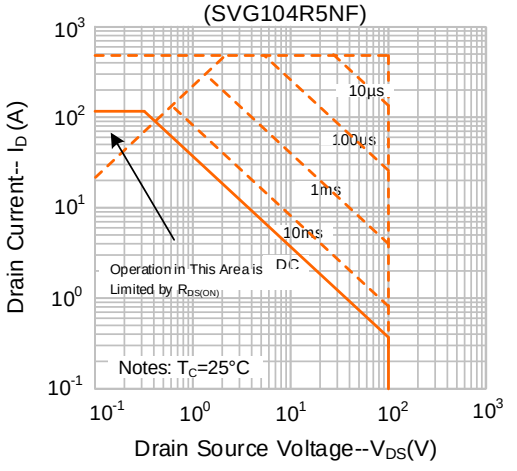
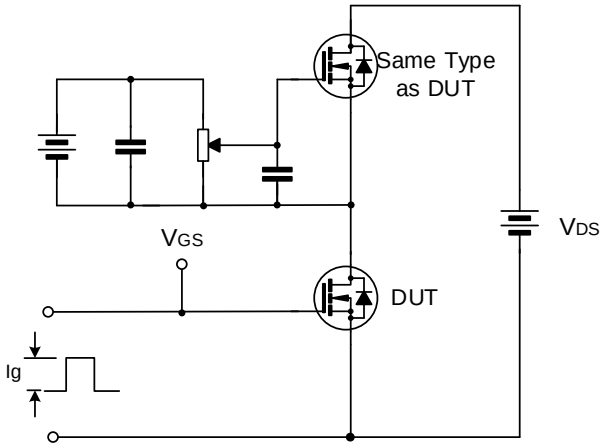


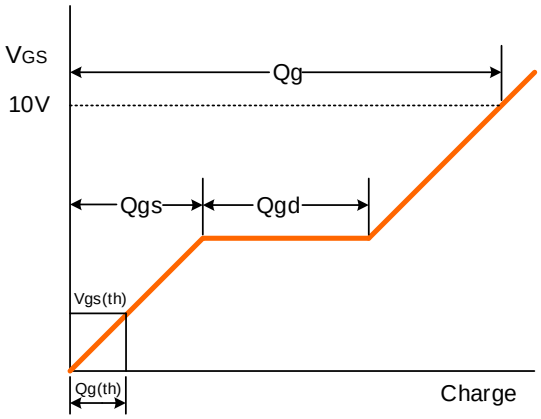
Figure 9-2. Max. Safe Operating Area (SVG104R5NF)



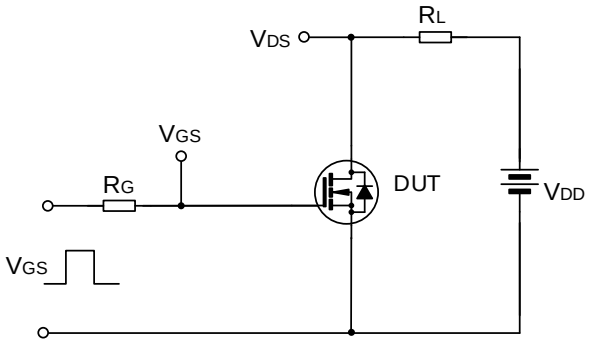
TYPICAL TEST CIRCUIT

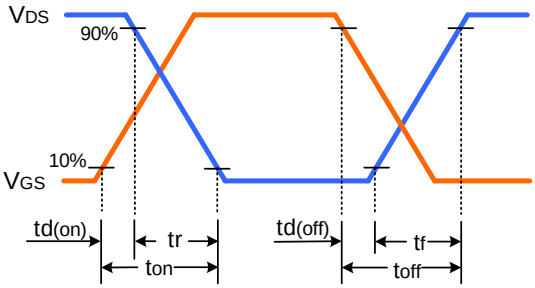
Gate Charge Test Circuit & Waveform



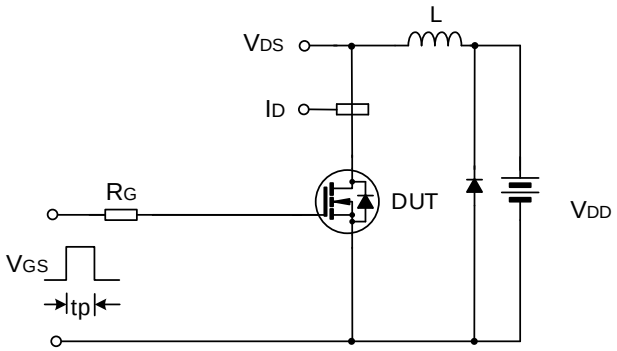


Resistive Switching Test Circuit & Waveform

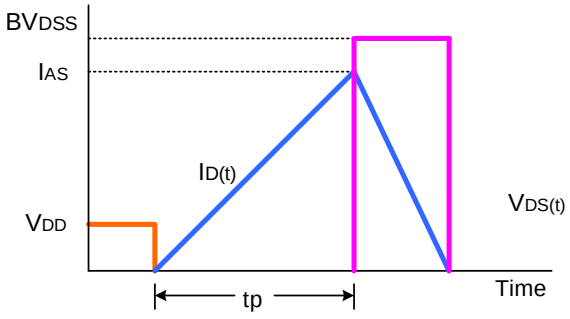




Unclamped Inductive Switching Test Circuit & Waveform

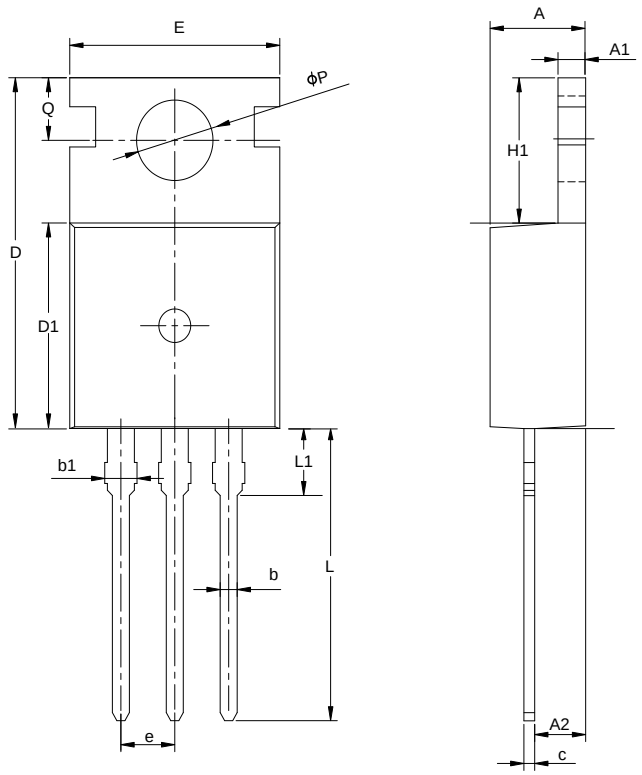


$$E_{AS} = \frac{1}{2} LI_{AS}^2$$



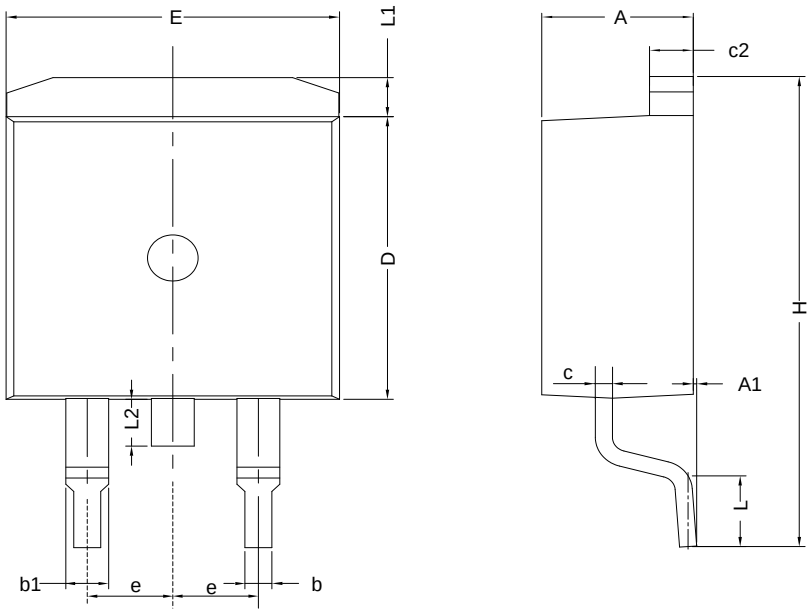
PACKAGE OUTLINE

TO-220-3L **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ϕP	3.40	3.70	3.90
Q	2.60	—	3.20

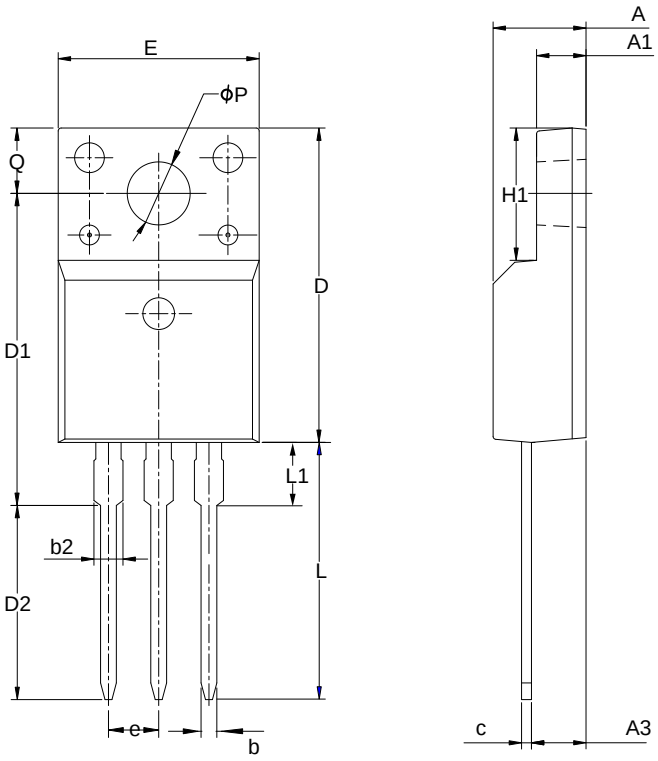
TO-263-2L **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
b1	1.17	—	1.50
c	0.30	—	0.60
c2	1.17	1.27	1.37
D	8.50	—	9.35
E	9.80	—	10.45
e	2.54BSC		
H	14.70	—	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	—	—	1.75

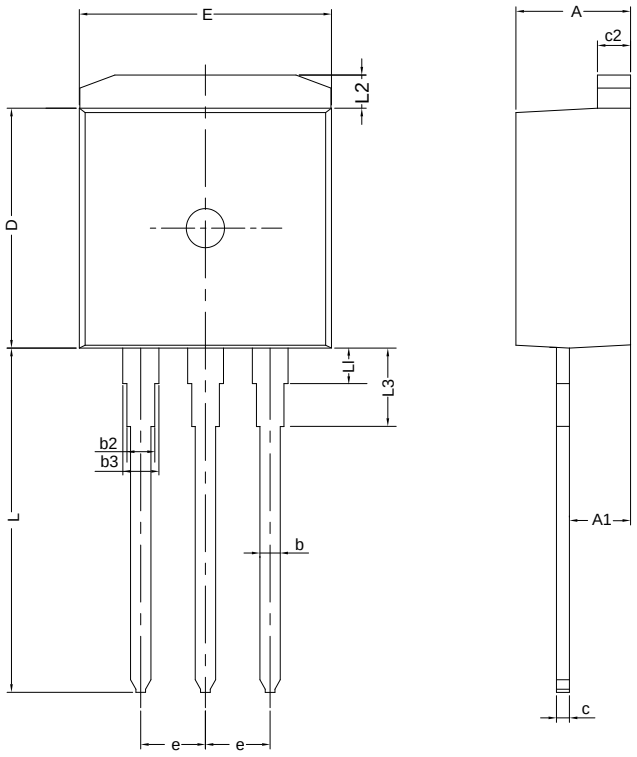
PACKAGE OUTLINE (CONTINUED)

TO-220F-3L **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	–	–	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	–	–	3.50
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

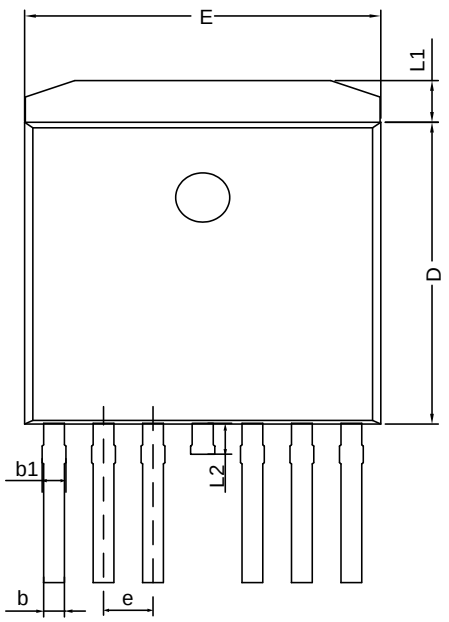
TO-262L-3L **UNIT: mm**

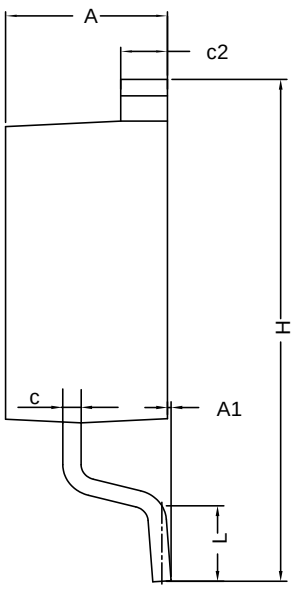


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	2.20	—	2.92
b	0.71	0.80	0.88
b2	0.90	1.01	1.08
b3	1.20	—	1.50
c	0.34	—	0.76
c2	1.22	1.30	1.35
D	8.38	—	9.30
E	9.80	10.16	10.54
e	2.54 BSC		
L	12.80	—	14.10
L1	1.40	1.50	1.60
L2	1.12	—	1.42
L3	3.00	3.20	3.40

PACKAGE OUTLINE (CONTINUED)

TO-263-6L **UNIT: mm**





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.20	4.40	4.60
A1	0	0.13	0.25
b	0.50	0.60	0.70
b1	0.55	0.70	0.90
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.25	9.50
E	9.80	10.00	10.20
e	1.27 BSC		
H	14.50	15.00	15.50
L	2.40	2.70	3.00
L1	0.80	1.00	1.20
L2	0.80	1.00	1.20

MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Important notice :

1. Silan reserves the right to make changes of this instruction without notice.
2. Customers should obtain the latest relevant information when purchasing and should verify whether such information is latest and complete. Please read this instruction and application manual and related materials carefully before using products, including the circuit operation precautions, etc.
3. The products belong to consumer electronic products. Silan does not give any warranties as to the suitability of the Silan's product for any specific use. The design intent, design definition and design of the product are not intended for application (the application stated in this instruction includes use, etc.) in transportation equipment, medical equipment, life-saving equipment, aerospace equipment, , non-civil equipment or non-civil use, etc. (the equipment stated in this instruction includes systems, devices, etc., all referred to as equipment).The product should not be used in any equipment or system whose manufacture, use or sale is prohibited under any applicable laws or regulations ("unintended use"). If the product is used for unintended use, therefore the full risks of such products application are borne by the customer and Silan assumes no liability for the product used for the unintended use. If the customer intends to use the Silan's product in a application where malfunction or failure can be reasonably be expected to result in personal injury, or serious property, or environment damage, the customer shall make adequate assessment, testing and verification, and Silan shall not be liable for such applications.
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7. Please use and apply product in compliance with all applicable laws and regulations, including but not limited to trade control regulations etc. The product is civil electronic product, please do not use it in non-civil fields.
8. Product promotion is endless, our company will wholeheartedly provide customers with better products!
9. Website: http: //www.silan.com.cn

Part No.:	SVG104R5NT(S)(F)(KL)(S6)	Document Type:	Datasheet
Copyright:	HANGZHOU SILAN MICROELECTRONICS CO.,LTD	Website:	http: //www.silan.com.cn

Rev.: 1.7

Revision History:

1. Add TO-263-6L package

Rev.: 1.6

Revision History:

1. Modify feature parameter
2. Update important notice

Rev.: 1.5

Revision History:

1. Increase the package of SVG104R5NKL(TO-262L-3L)

Rev.: 1.4

Revision History:

1. Increase the package of SVG104R5NF
2. Update curve template
3. Update the typical test circuit and important notice

Rev.: 1.3

Revision History:

1. Update Electrical schematic and typical test circuit

Rev.: 1.2

Revision History:

1. Add EAS value of L=0.1mH

Rev.: 1.1

Revision History:

1. Add TO-263-2L

Rev.: 1.0

Revision History:

1. First release