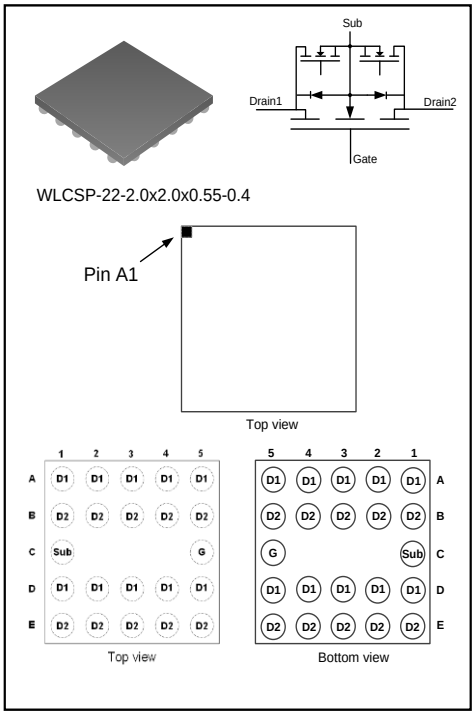
10A, 28V N-CHANNEL MOSFET

DESCRIPTION

SVGP03100NCS is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance.

This device is widely used in power management.



FEATURES

- 10A, 28V, $R_{DS(on)(typ.)}$=12mΩ@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVGP03100NCSTR	WLCSP-22-2.0x2.0x0.55-0.4	N	Halogen free	Tape&reel

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, T_C=25°C)

Characteristics		Symbol	Ratings	Unit
Drain-source Voltage		V_{DS}	28	V
Gate-source Voltage		V_{GS}	±15	V
Drain Current	T_C=25°C	I_D	10	A
	T_C=100°C		6.4	
Drain Current Pulsed		I_{DM}	15	A
Power Dissipation (T_C=25°C)		P_D	4.1	W
Operation Junction Temperature Range		T_J	-55～+150	°C
Storage Temperature Range		T_{stg}	-55～+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-ambient	$R_{\theta JA}$	32.7*	°C/W

Note: at room temperature 25°C (open environment), θ JA is measured based on thermal resistance test standard JEDEC 51-7.

KEY PERFORMANCE PARAMETERS (UNLESS OTHERWISE NOTED, T_C=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain-source Breakdown Voltage	BV_{D1SS}	V_{GS}=0V, V_{D2}=0V, I_{D1}=250μA	28	--	--	V
Drain-source Breakdown Voltage	BV_{D2SS}	V_{GS}=0V, V_{D1}=0V, I_{D2}=250μA	28	--	--	V
Drain 1 -source Leakage Current	I_{D1SS}	V_{D1S}=24V, V_{GS}=0V, V_{D2}=0V	--	--	1.0	μA
Drain 2 -source Leakage Current	I_{D2SS}	V_{D2S}=24V, V_{GS}=0V, V_{D1}=0V	--	--	1.0	μA
Gate-source Leakage Current	I_{GSS}	V_G=10V, V_{D1}= V_{D2}=V_{Sub}=0V	--	--	100	nA
	I_{SGS}	V_G=-10V, V_{D1}= V_{D2}=V_{Sub}=0V	--	--	100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{D1}=V_{Sub}=0V, V_G=V_{D2} , I_{D2}=250μA	1.0	--	2.0	V
	$V_{GS(th)}$	V_{D2}=V_{Sub}=0V, V_G=V_{D1} , I_{D1}=250μA	1.0	--	2.0	V
Static Drain-source On State Resistance	$R_{D1D2(on)}$	V_{GS}=5V, I_D=4A	--	9.5	15	mΩ
		V_{GS}=10V, I_D=4A	--	7.5	12	
Input Capacitance	C_{iss}	f=1MHz,V_{GS}=0V, V_{DS}=15V	2586	3362	4371	pF
Output Capacitance	C_{oss}		638	829	1078	
Reverse Transfer Capacitance	C_{rss}		355	461	599	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=20V, V_{GS}=10V, R_G=6Ω, I_D=5A (Notes 1,2)	--	9.3	--	ns
Turn-on Rise Time	t_r		--	40	--	
Turn-off Delay Time	$t_{d(off)}$		--	91	--	
Turn-off Fall Time	t_f		--	70	--	
Total Gate Charge	Q_g	V_{DD}=22V, V_{GS}=10V, I_D=10A (Notes 1,2)	--	70	--	nC
Gate-source Charge	Q_{gs}		--	15	--	
Gate-drain Charge	Q_{gd}		--	13	--	
Diode Forward Voltage	V_{SD1}	I_{Sub}=20mA,V_G=V_{Sub}=V_{D2}=0V	--	--	1.2	V
	V_{SD2}	I_{Sub}=20mA,V_G=V_{Sub}=V_{D1}=0V	--	--	1.2	V

Notes:

1. Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
2. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. Typical Output Characteristics

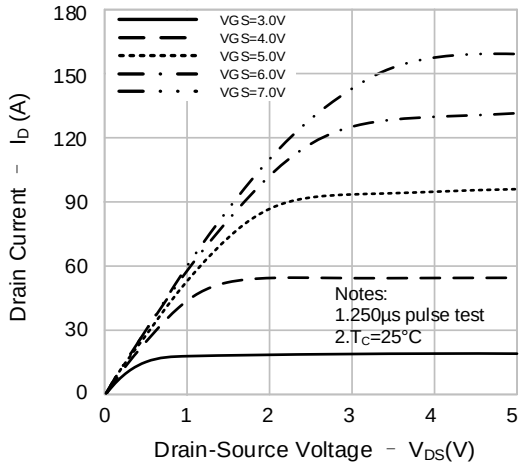


Figure 2. Transfer Characteristics

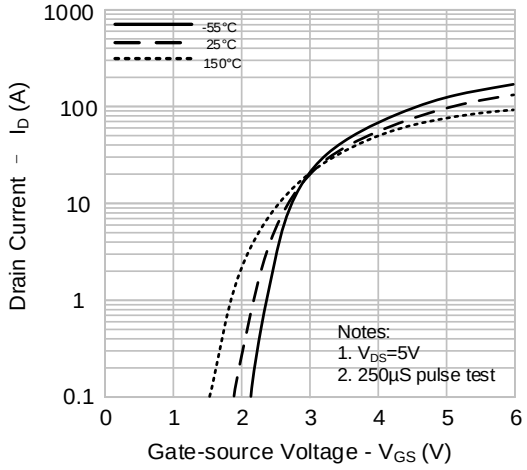


Figure 3. On-resistance vs. Drain Current

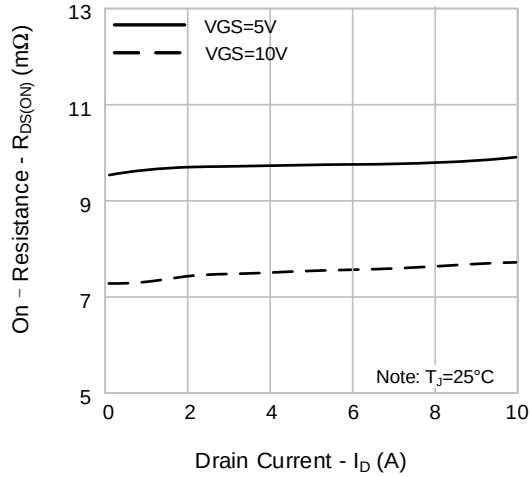


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

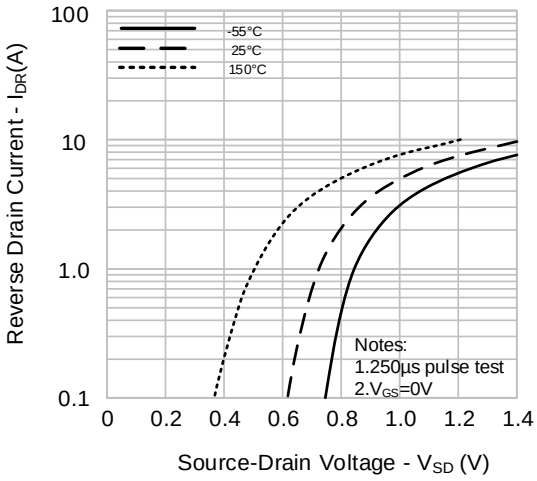


Figure 5. Capacitance Characteristics

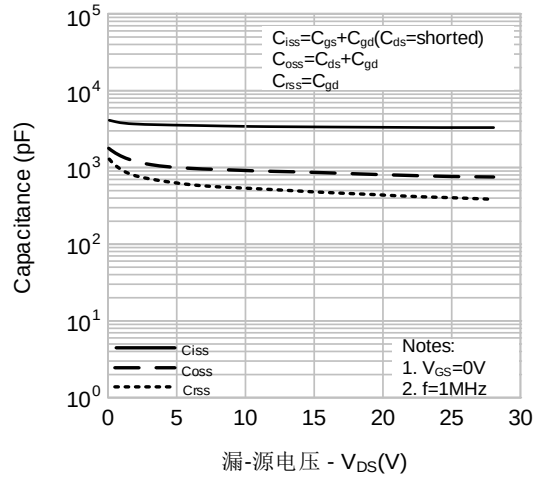
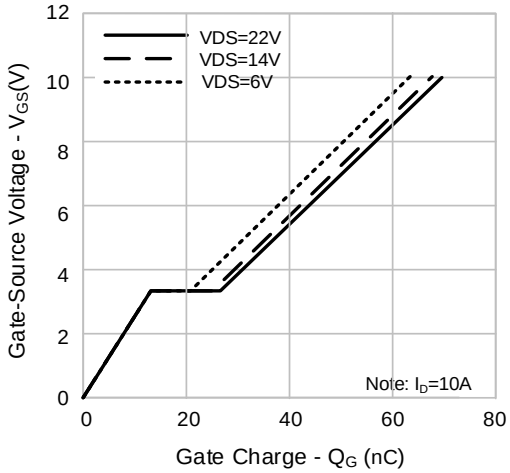


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS (CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

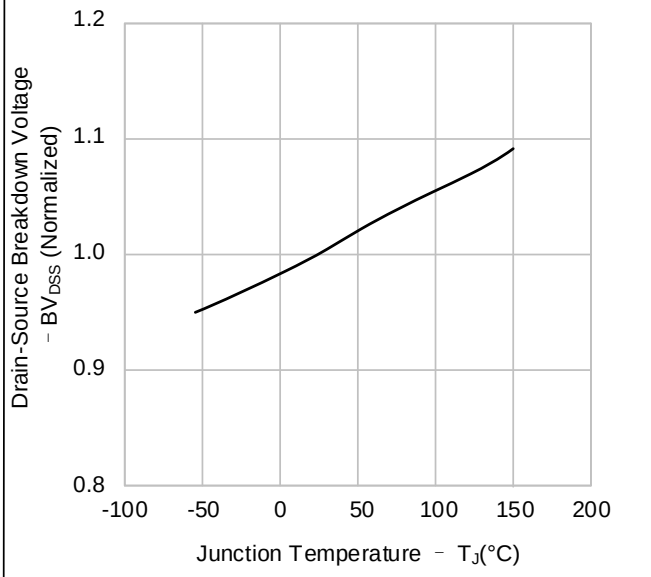
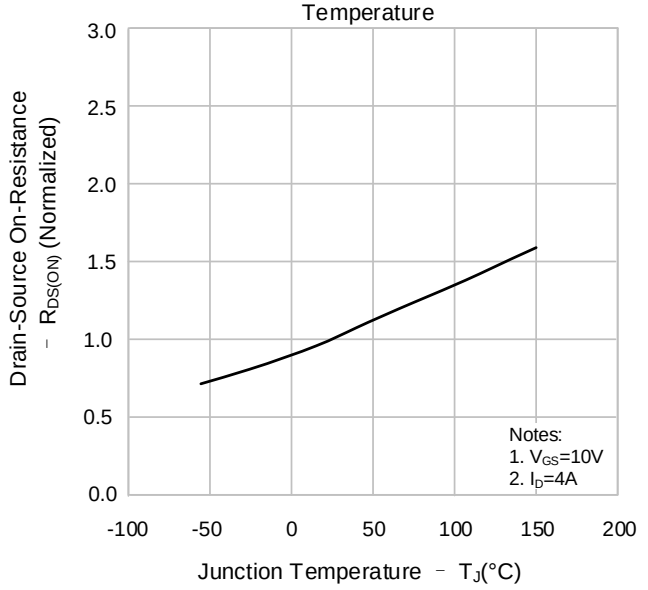
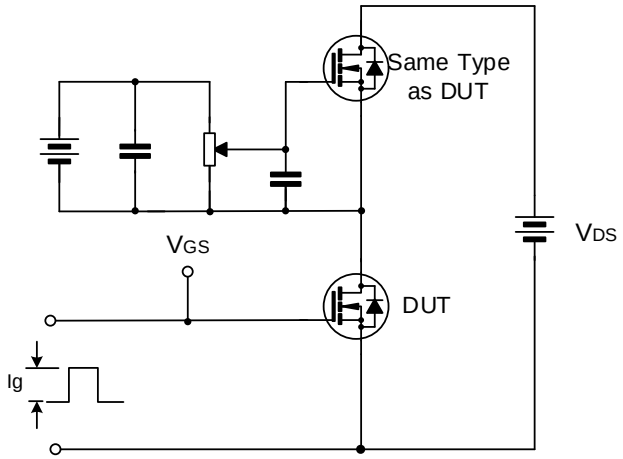


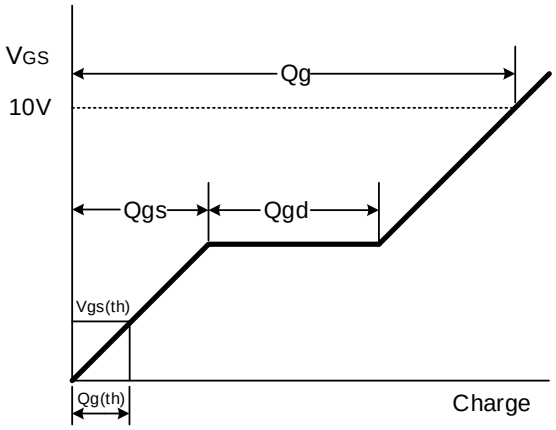
Figure 8. On-resistance Variation vs. Temperature



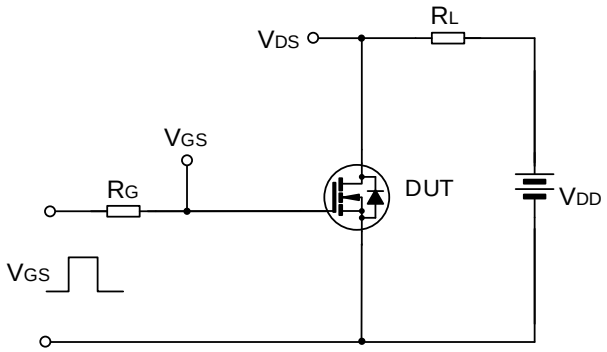
TYPICAL TEST CIRCUIT

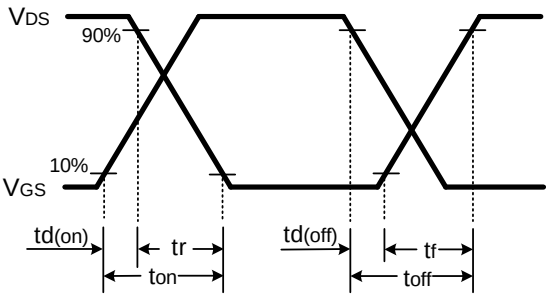
Gate Charge Test Circuit & Waveform



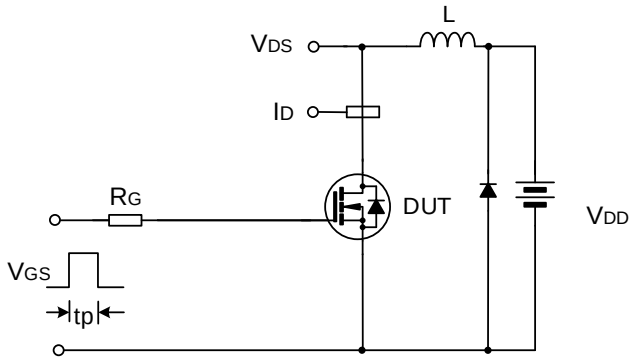


Resistive Switching Test Circuit & Waveform

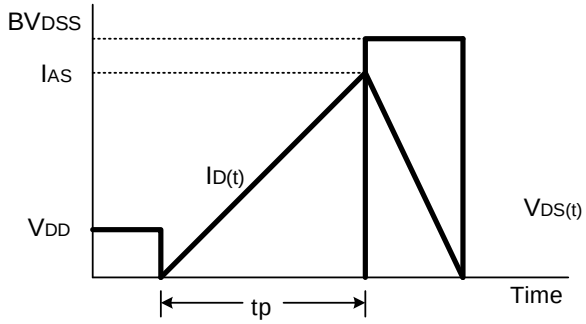




Unclamped Inductive Switching Test Circuit & Waveform

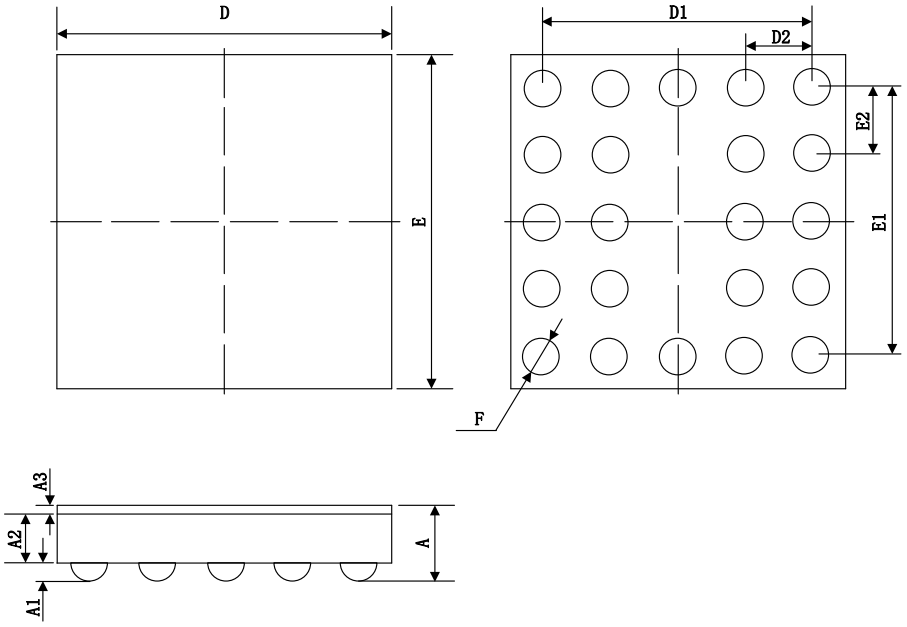


$$E_{AS} = \frac{1}{2} L I_{AS}^2$$



PACKAGE OUTLINE

WLCSP-22-2.0x2.0x0.55-0.4 **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.5125	0.550	0.5875
A1	0.175	0.195	0.215
A2	0.3175	0.330	0.3425
A3	0.020	0.025	0.030
D	1.975	2.000	2.025
E	1.975	2.000	2.025
F	0.248	0.268	0.288
D1	——	1.600	——
D2	——	0.400	——
E1	——	1.600	——
E2	——	0.400	——

MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Important notice:

1. Silan reserves the right to make changes of this instruction without notice.
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Rev.: 1.0

Revision History:

1. First release