

### 180A, 100V N-CHANNEL MOSFET

### DESCRIPTION

SVGP103R0NT(P7) is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance.

This device is widely used in power management for UPS and Inverter Systems.

### FEATURES

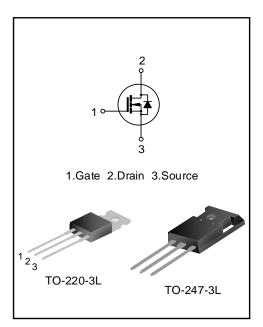
- 180A, 100V, R<sub>DS(on)(typ.)</sub>=2.5mΩ@V<sub>GS</sub>=10V
- Low gate charge
- Low Crss
- Fast switching
- Extreme dv/dt rated
- 100% avalanche tested
- Pb-free lead plating
- RoHS compliant

### FEATURES

Characteristics	Ratings	Unit
V <sub>DS</sub>	100	V
V <sub>GS(th)</sub>	2.2~3.8	V
R <sub>DS(on),max</sub> .	3.0	mΩ
I <sub>D</sub>	180	А
Q <sub>g.typ.</sub>	145	nC

### **ORDERING INFORMATION**

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVGP103R0NT	TO-220-3L	P103R0NT	Halogen free	Tube
SVGP103R0NP7	TO-247-3L	P103R0NP7	Halogen free	Tube





### ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, TJ=25°C)

				Ratings		
Characteristics	Symbol	Test conditions	Min.	Тур.	Max.	Unit
Drain-source Voltage	V <sub>DS</sub>		100			V
Gate-source Voltage	V <sub>GS</sub>		-20		20	V
Drain Current (Note 1)		T <sub>C</sub> =25°C			180	A
Drain Current (Note 1)	ID	T <sub>C</sub> =100°C			128	А
Drain Current Pulsed (Note 2)	I <sub>DM</sub>	T <sub>C</sub> =25°C			720	А
Power Dissipation(TO-220-3L) (Note 3)	P <sub>D</sub>	T <sub>c</sub> =25°C			216	W
Power Dissipation(TO-247-3L) (Note 3)	P <sub>D</sub>	T <sub>C</sub> =25°C			278	W
Single Pulsed Avalanche Energy	E <sub>AS</sub>	L=0.5mH, V <sub>DD</sub> =80V, R <sub>G</sub> =25Ω,			900	mJ
Single Pulsed Avalanche Current	I <sub>AS</sub>	starting temperature T <sub>J</sub> =25°C			60	А
Single Pulsed Avalanche Energy	E <sub>AS</sub>	L=0.1mH, V <sub>DD</sub> =80V, R <sub>G</sub> =25Ω,			551	mJ
Single Pulsed Avalanche Current	I <sub>AS</sub>	starting temperature TJ=25°C			105	А
Operation Junction Temperature Range	TJ		-55		150	°C
Storage Temperature Range	T <sub>stg</sub>		-55		150	°C

### THERMAL CHARACTERISTICS

#### Table 1. TO-220-3L (SVGP103R0NT) Thermal characteristics

Characteristics	Symbol	mbol Test conditions	Ratings			Unit
Gliaracteristics	Symbol	Test conditions	Min.	Тур.	Max.	Onit
Thermal Resistance,	Paul				0.58	°C/W
Junction-case, Bottom	$R_{ extsf{ heta}JC}$				0.56	-0/00
Thermal Resistance,	R <sub>0JA</sub>				60 F	°C/W
Junction-ambient	ΓθJA				62.5	-0/00
Soldering Temperature (in line)	T <sub>sold</sub>	$15_{-0}^{+2}$ sec, 1time			260	°C

Table 2. TO-247-3L(SVGP103R0NP7) Thermal characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
Gliaracteristics	Symbol	Test conditions	Min.	Тур.	Max.	Onic
Thermal Resistance,	Paul				0.45	°C/W
Junction-case, Bottom	$R_{\theta JC}$				0.45	-0/00
Thermal Resistance,	R <sub>0JA</sub>				50	°C/W
Junction-ambient	κθja				50	°C/W
Soldering Temperature (in line)	T <sub>sold</sub>	$15_{-0}^{+2}$ sec, 1time			260	°C



### ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, TJ=25°C)

#### Static characteristics

Characteristics	Symbol Test conditions		Ratings			Unit
Gilaracteristics	Symbol		Min.	Тур.	Max.	Omt
Drain-source Breakdown Voltage	$BV_{DSS}$	V <sub>GS</sub> =0V, I <sub>D</sub> =250µA	100			V
Drain-source Leakage Current	1	$V_{DS}$ =100V, $V_{GS}$ =0V, $T_{J}$ =25°C		-	1.0	μA
Diam-source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V, T <sub>J</sub> =125°C		4.5		μA
Gate-source Leakage Current	I <sub>GSS</sub>	$V_{GS}=\pm 20V$ , $V_{DS}=0V$		-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{GS}=V_{DS}$ , $I_{D}=250\mu A$	2.2		3.8	V
Static Drain-source On State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =90A		2.5	3.0	mΩ
Gate Resistance	Rg	f=1MHz		2.6		Ω

### **Dynamic characteristics**

Characteristics	Symbol	Test conditions		Ratings		Unit
Characteristics	Symbol	rest conditions	Min.	Тур.	Max.	Unit
Input Capacitance	C <sub>iss</sub>			9422		
Output Capacitance	Coss	f=1MHz, V <sub>GS</sub> =0V, V <sub>DS</sub> =50V		1188		pF
Reverse Transfer Capacitance	Crss			17		
Turn-on Delay Time	t <sub>d(on)</sub>			42		
Turn-on Rise Time	tr	$V_{DD}$ =50V, $V_{GS}$ =10V, $R_{G}$ =3.0 $\Omega$ , $I_{D}$ =90A		65		20
Turn-off Delay Time	t <sub>d(off)</sub>	(Notes 4,5)		92		ns
Turn-off Fall Time	t <sub>f</sub>	(110185 4,5)		37		
Total Gate Charge	Qg			145		
Gate-source Charge	Q <sub>gs</sub>	$V_{DD}$ =50V, $V_{GS}$ =10V, $I_{D}$ =90A		57		nC
Gate-drain Charge	Q <sub>gd</sub>	(Notes 4,5)		35		
Gate-plateau Voltage	V <sub>plateau</sub>			5.9		V

#### **Reverse diode characteristics**

Characteristics Svm		Symbol Test conditions		Ratings			
Gharacteristics	Symbol	Test conditions	Min.	Тур.	Max.	Unit	
Continuous Diode Forward Current	I <sub>S</sub>	T <sub>C</sub> =25°C, integral reverse P-N	-		180	А	
Diode Pulse Current	I <sub>S,pulse</sub>	junction diode in the MOSFET			720	A	
Diode Forward Voltage	$V_{\text{SD}}$	I <sub>S</sub> =90A, V <sub>GS</sub> =0V			1.4	V	
Reverse Recovery Time	Trr	I <sub>S</sub> =90A, V <sub>GS</sub> =0V, V <sub>R</sub> =50V		91		ns	
Reverse Recovery Charge	Q <sub>rr</sub>	dI⊧/dt=100A/µs (Note 4)		225		nC	

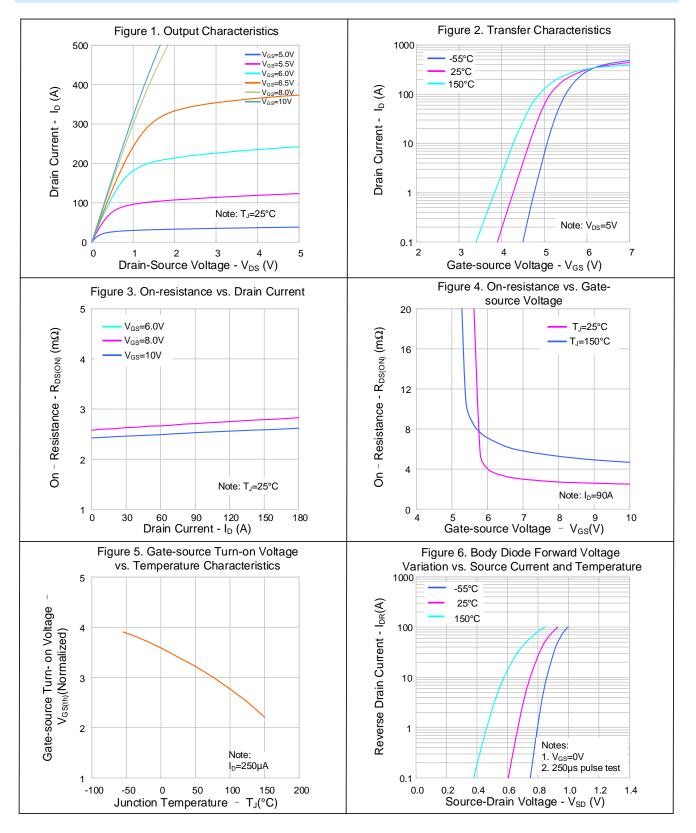
#### Notes:

1. The rated value only refers to the maximum absolute value at the case temperature of 25°C in the specification. If the case temperature is higher than 25°C, it should be derated according to the actual environmental conditions;

- 2. Pulse time 5µs; pulse width is limited by the maximum junction temperature;
- 3. The dissipation power will change with temperature, derating above 25°C: 1.72W/°C(TO-220-3L)/ 2.22W/°C(TO-247-3L);
- 4. Pulse Test: Pulse width ≤300µs, Duty cycle≤2%;
- 5. Essentially independent of operating temperature.

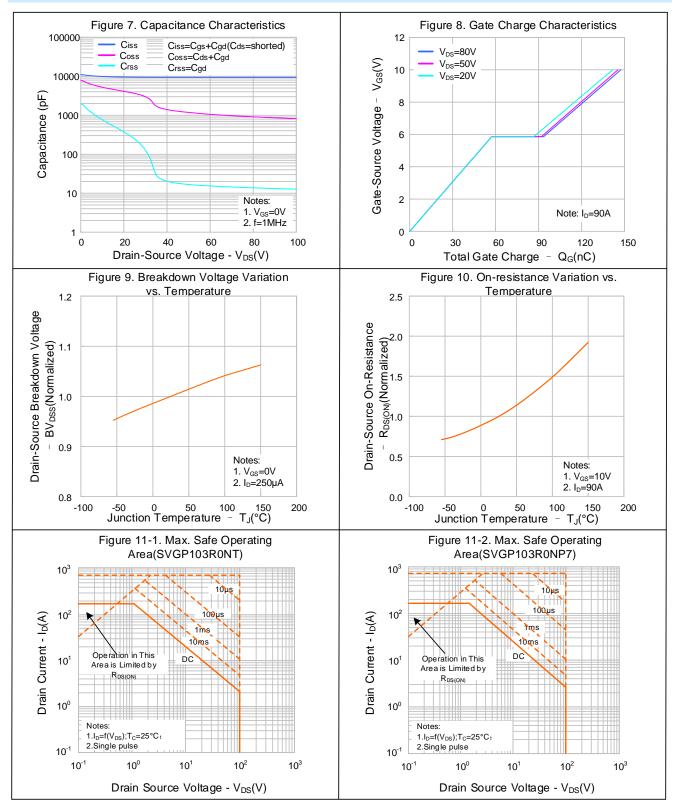


### **TYPICAL CHARACTERISTICS**



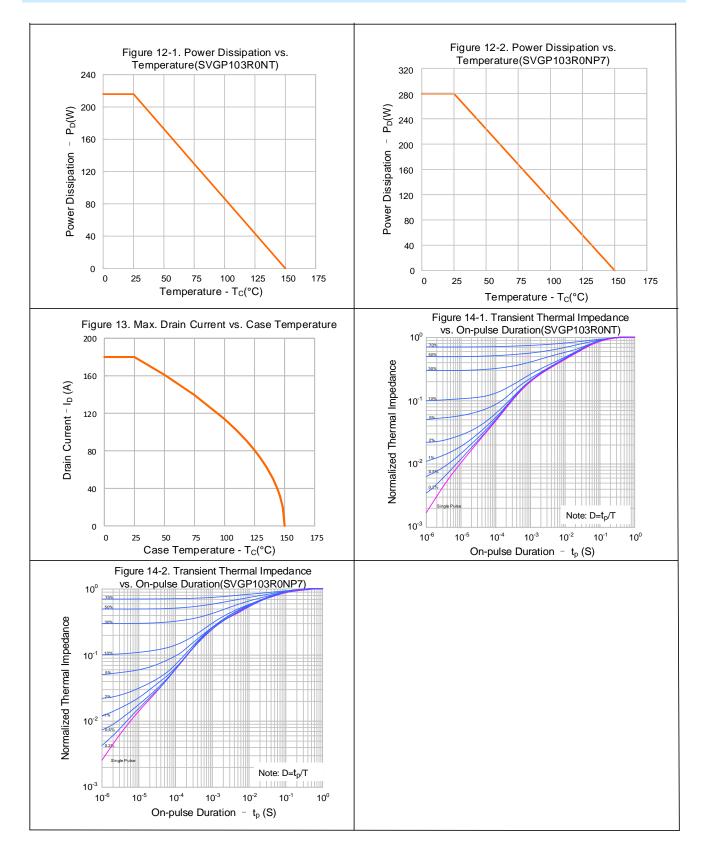


### **TYPICAL CHARACTERISTICS (CONTINUED)**



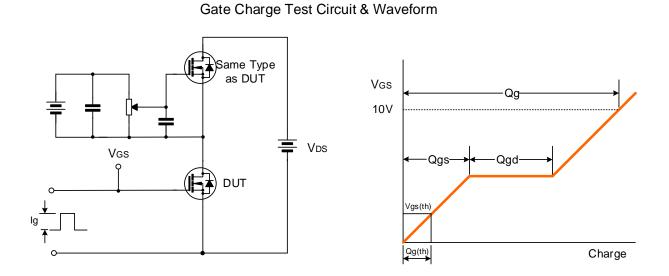


### **TYPICAL CHARACTERISTICS (CONTINUED)**

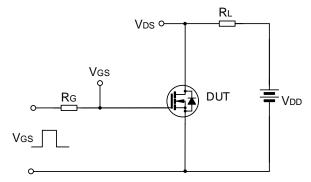


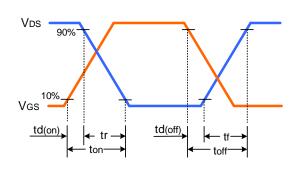


### **TYPICAL TEST CIRCUIT**

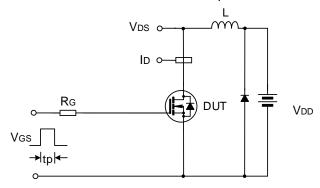


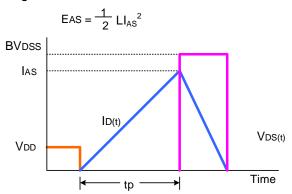
Resistive Switching Test Circuit & Waveform





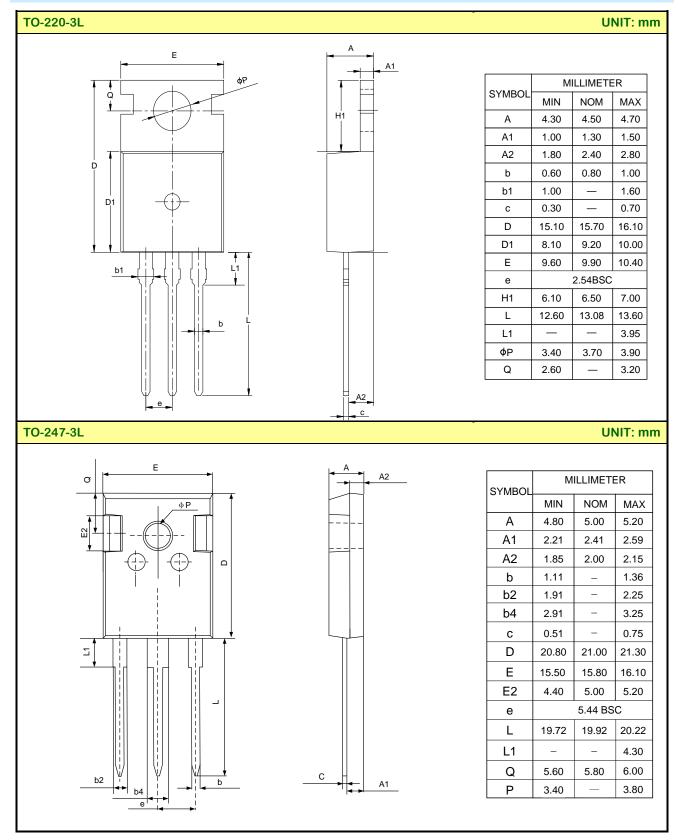
### Unclamped Inductive Switching Test Circuit & Waveform







### PACKAGE OUTLINE







### MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.



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Revisior	n History:		
1.	Modify some parameters		
2.	Update curve		
3.	Update important notice		
Rev.:	1.1		
Revisior	n History:		
1.	Add SVGP103R0NP7(TO-247-3L) package		
2.	Add curve 11-2、12-2、14-2		
Rev.:	1.0		
Revisior	n History:		
1.	First release		