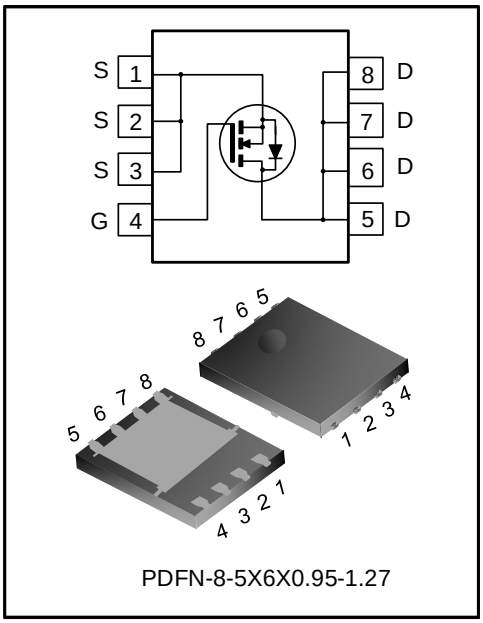
136A, 100V N-CHANNEL MOSFET

DESCRIPTION

SVGP104R1NL5 is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance.

This device is widely used in power management for UPS and Inverter Systems.



PDFN-8-5X6X0.95-1.27

FEATURES

- 136A, 100V, $R_{DS(on)(typ.)}$=3.4mΩ@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Extreme dv/dt rated
- 100% avalanche tested
- Pb-free lead plating
- RoHS compliant

KEY PERFORMANCE PARAMETERS

Characteristics	Ratings	Unit
V_{DS}	100	V
$V_{GS(th)}$	2.3~3.9	V
$R_{DS(on),max.}$	4.0	mΩ
I_D	136	A
$Q_{g.typ.}$	63	nC

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVGP104R1NL5TR	PDFN-8-5X6X0.95-1.27	P104R1NL5	Halogen free	Tape&Reel

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, T_J=25°C)

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Drain-source Voltage	V_{DS}	--	100	--	--	V
Gate-source Voltage	V_{GS}	--	-20	--	20	V
Drain Current (Note 1)	I_D	T_C=25°C	--	--	136	A
		T_C=100°C	--	--	86	A
Drain Current Pulsed (Note 2)	I_{DM}	T_C=25°C	--	--	544	A
Power Dissipation (Note 3)	P_D	T_C=25°C	--	--	147	W
Single Pulsed Avalanche Energy	E_{AS}	L=0.5mH, V_{DD}=80V, R_G=25Ω, starting temperature T_J=25°C	--	--	289	mJ
Single Pulsed Avalanche Current	I_{AS}	--	--	--	34	A
Operation Junction Temperature Range	T_J	--	-55	--	150	°C
Storage Temperature Range	T_{stg}	--	-55	--	150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Thermal Resistance, Junction-case, Bottom	$R_{\theta JC}$	--	--	--	0.85	°C/W
Thermal Resistance, Junction-ambient	$R_{\theta JA}$	--	--	--	50	°C/W
Soldering Temperature (SMD)	T_{sold}	Reflow soldering: 10±1sec,3times	--	--	260	°C

ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, T_J=25°C)

Static characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Drain-source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	100	--	--	V
Drain-source Leakage Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V, T_J=25°C	--	--	1.0	μA
		V_{DS}=100V, V_{GS}=0V, T_J=125°C	--	5.0	--	
Gate-source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	2.3	--	3.9	V
Static Drain-source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=50A	--	3.4	4.0	mΩ
		V_{GS}=6V, I_D=25A	--	4.0	5.6	mΩ
Gate Resistance	R_g	f=1MHz	--	3.3	--	Ω

Dynamic characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Input Capacitance	C_{iss}	f=1MHz, V_{GS}=0V, V_{DS}=50V	--	4760	--	pF
Output Capacitance	C_{oss}		--	620	--	
Reverse Transfer Capacitance	C_{rss}		--	17	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=50V, V_{GS}=10V, R_G=3Ω, I_D=50A (Notes 4, 5)	--	31	--	ns
Turn-on Rise Time	t_r		--	96	--	
Turn-off Delay Time	$t_{d(off)}$		--	60	--	
Turn-off Fall Time	t_f		--	25	--	
Total Gate Charge	Q_g	V_{DD}=50V, V_{GS}=10V, I_D=50A (Notes 4, 5)	--	63	--	nC
Gate-source Charge	Q_{gs}		--	30	--	
Gate-drain Charge	Q_{gd}		--	9.0	--	
Gate-plateau Voltage	$V_{plateau}$		--	5.9	--	V

Reverse diode characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Continuous Diode Forward Current	I_S	Integral reverse P-N junction diode in the MOSFET	--	--	136	A
Diode Pulse Current	$I_{S,pulse}$		--	--	544	
Diode Forward Voltage	V_{SD}	I_S=50A, V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=50A, V_{GS}=0V, V_R=50V	--	60	--	ns
Reverse Recovery Charge	Q_{rr}	dI_F/dt=100A/μs (Note 4)	--	99	--	nC

Notes:

1. The rated value only refers to the maximum absolute value at the case temperature of 25°C in the specification. If the case temperature is higher than 25°C, it should be derated according to the actual environmental conditions;
2. Pulse time 5μs, pulse width is limited by the maximum junction temperature;
3. The dissipation power will change with temperature, derating above 25°C: 1.18W/°C;
4. Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

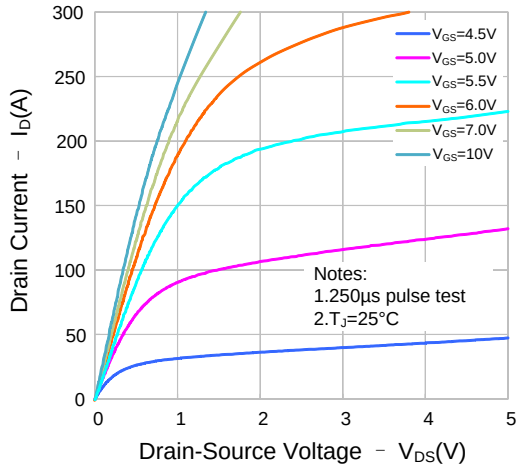


Figure 2. Transfer Characteristics

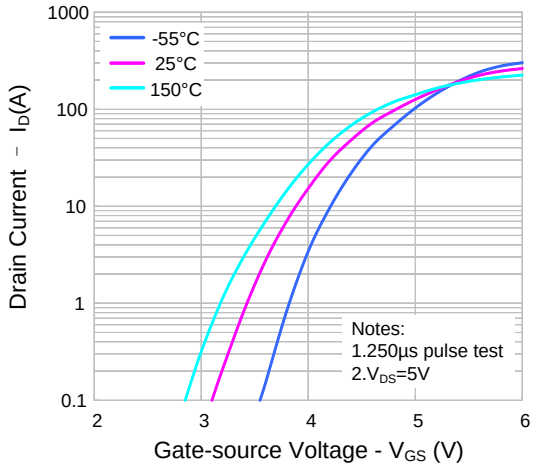


Figure 3. On-resistance vs. Drain Current

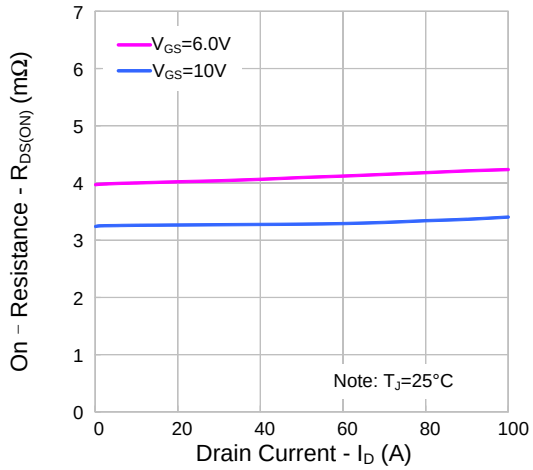


Figure 4. On-resistance vs. Gate-source Voltage

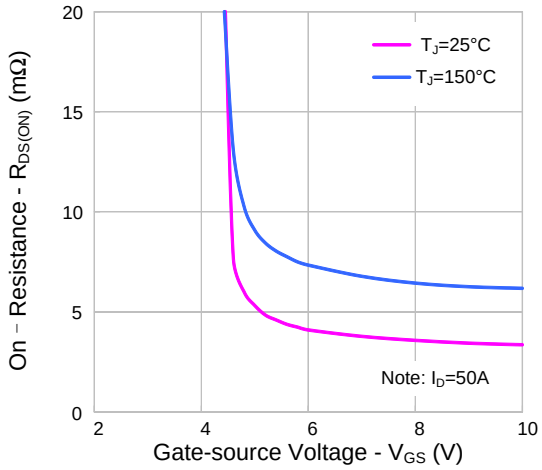


Figure 5. Turn-on Voltage vs. Temperature characteristics

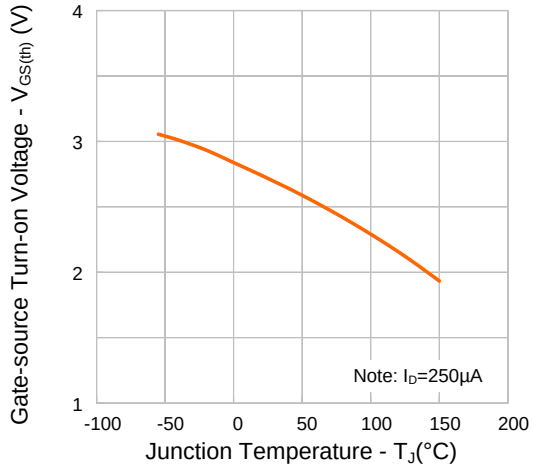
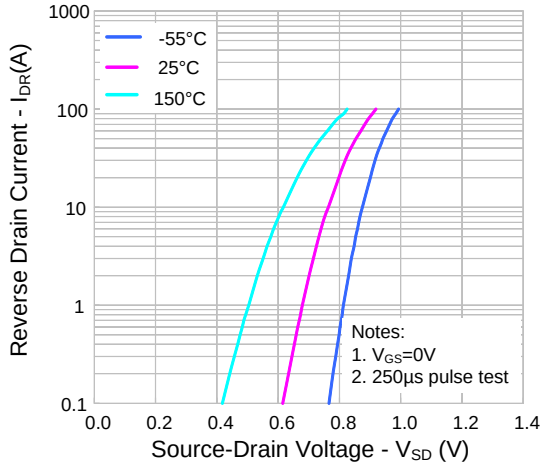


Figure 6. Body Diode Forward Voltage Variation vs. Source Current and Temperature



TYPICAL CHARACTERISTICS (CONTINUED)

Figure 7. Capacitance Characteristics

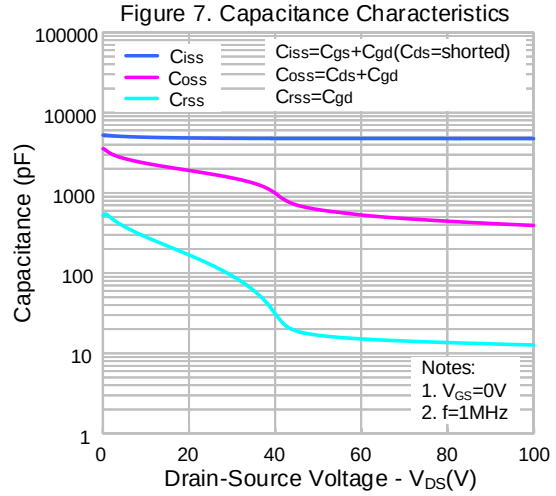


Figure 8. Gate Charge

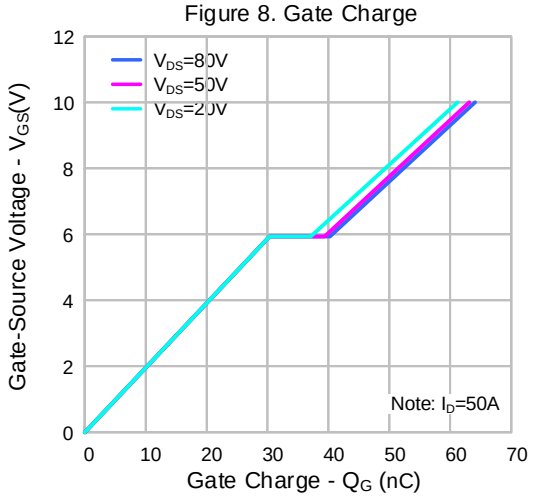


Figure 9. Breakdown Voltage Variation vs. Temperature

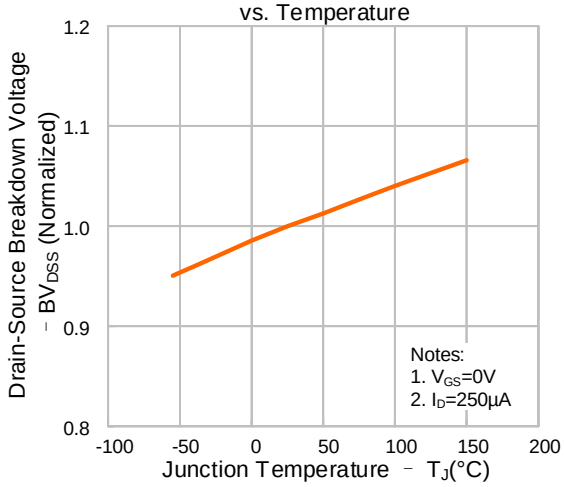


Figure 10. On-resistance Variation vs. Temperature

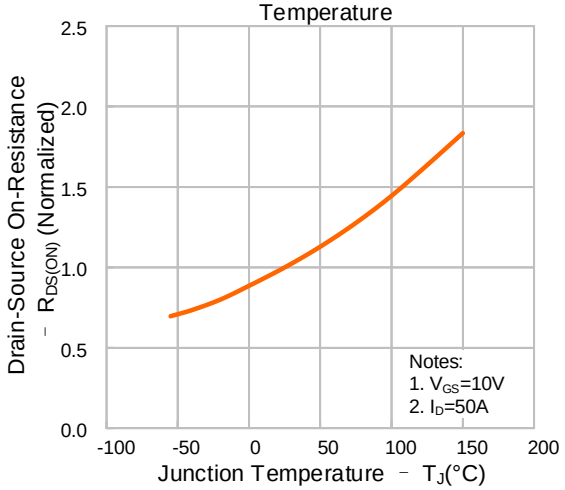


Figure 11. Max. Safe Operating Area

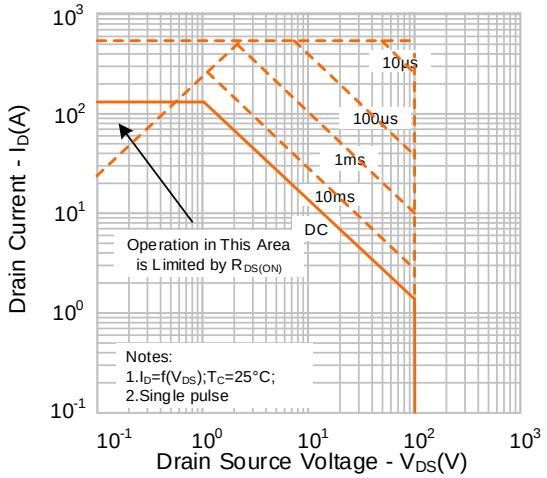
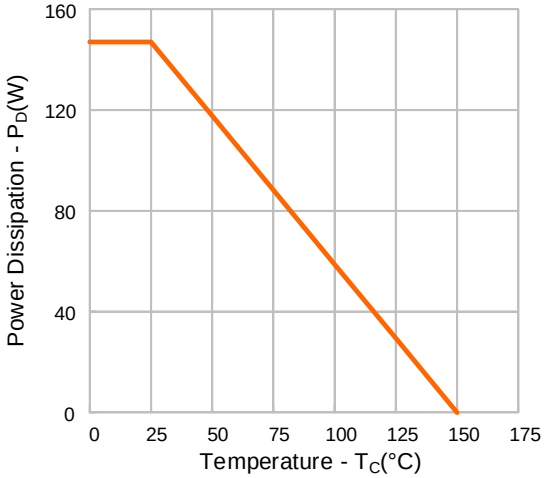


Figure 12. Power Dissipation vs. Case Temperature



TYPICAL CHARACTERISTICS (CONTINUED)

Figure 13. Drain Current vs. Case Temperature

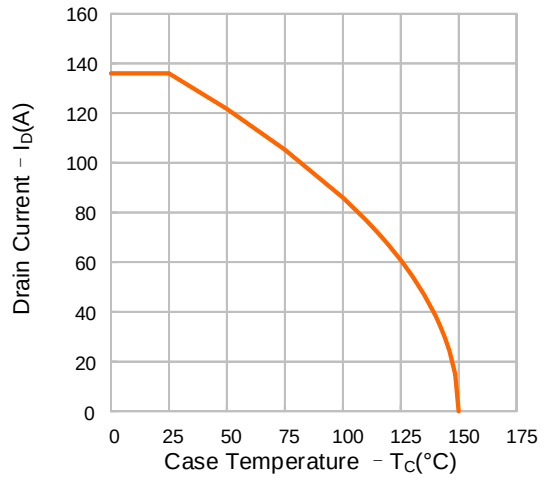
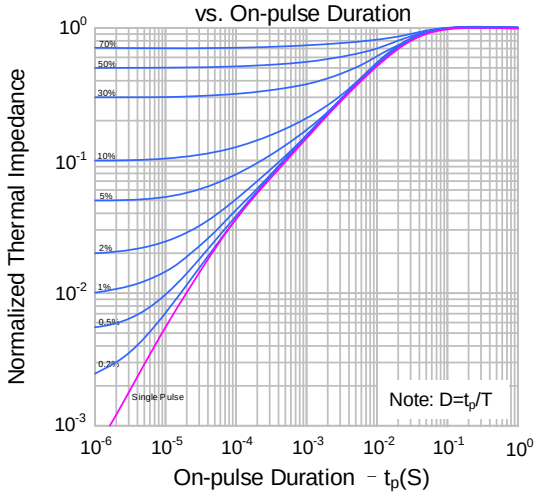
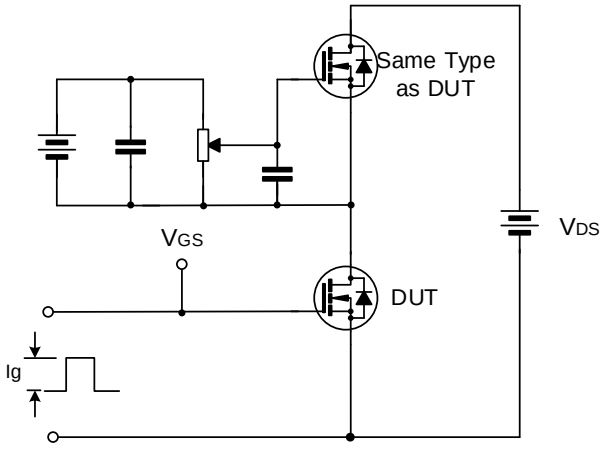


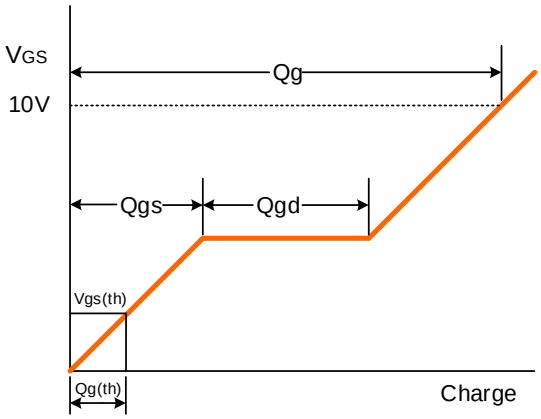
Figure 14. Transient Thermal Impedance vs. On-pulse Duration



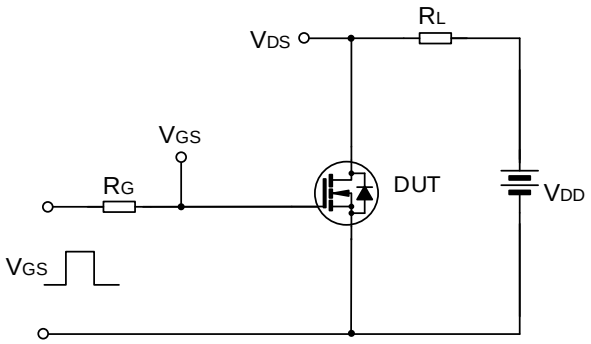
TYPICAL TEST CIRCUIT

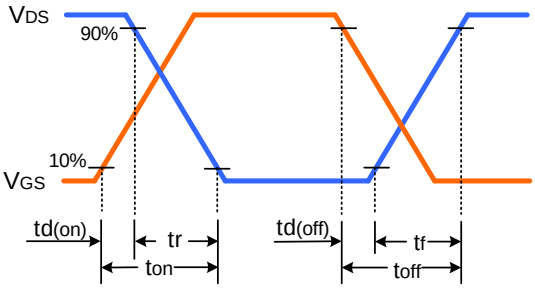
Gate Charge Test Circuit & Waveform



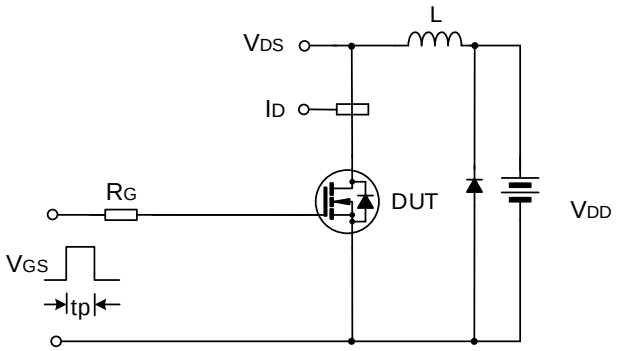


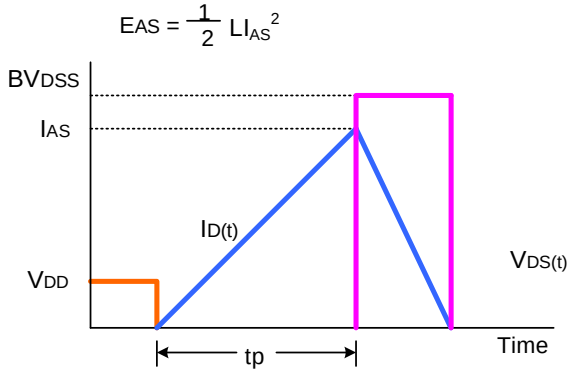
Resistive Switching Test Circuit & Waveform





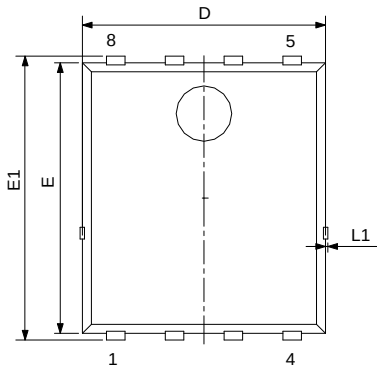
Unclamped Inductive Switching Test Circuit & Waveform



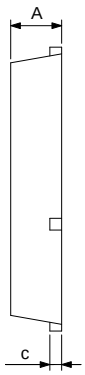


PACKAGE OUTLINE

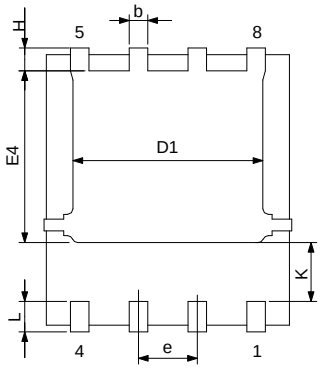
PDFN-8-5X6X0.95-1.27 **UNIT: mm**



Top View



Side View



Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.90	—	1.20
c	0.154	0.25	0.354
D	4.80	—	5.40
E	5.66	—	6.06
D1	3.76	—	4.30
E1	5.90	—	6.35
b	0.30	—	0.55
K	1.10	1.30	1.50
e	1.07	1.27	1.37
E4	3.34	—	3.92
L	0.30	0.60	0.71
L1	—	—	0.12
H	0.40	—	0.71

MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Important notice :

1. Silan reserves the right to make changes of this instruction without notice.
2. Customers should obtain the latest relevant information when purchasing and should verify whether such information is latest and complete. Please read this instruction and application manual and related materials carefully before using products, including the circuit operation precautions, etc.
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Rev.: 1.3

Revision History:

1. Delete the wave soldering condition
2. Update the typical test circuit
3. Update the important notice

Rev.: 1.2

Revision History:

1. Update I_D and SOA
2. Add figure 13 and figure 14

Rev.: 1.1

Revision History:

1. Update electrical characteristics
2. Update figure 7 and figure 8

Rev.: 1.0

Revision History:

1. First release