

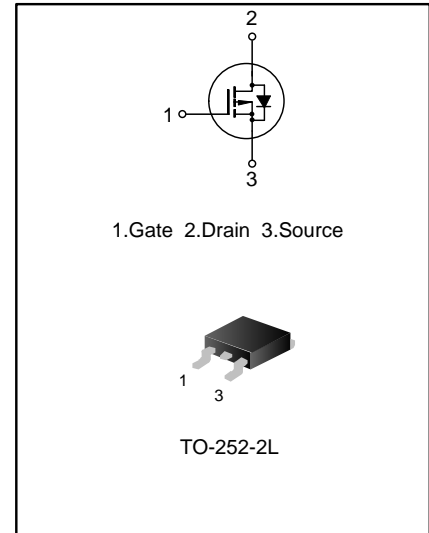
-80A, -60V P-CHANNEL MOSFET

DESCRIPTION

SVGQ06130PD is an P-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance and high avalanche breakdown tolerance. This device is widely used in power management for UPS and Inverter Systems.

FEATURES

- ◆ Compliant with AEC-Q101 standards.
- ◆ -80A, -60V, $R_{DS(on)(typ.)}=8.0m\Omega @ V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low C_{rss}
- ◆ Fast switching
- ◆ Extreme dv/dt rated
- ◆ 100% avalanche tested
- ◆ Pb-free lead plating
- ◆ RoHS compliant
- ◆ Max. junction temperature: $T_{jmax.}=175\text{ }^{\circ}\text{C}$



KEY PERFORMANCE PARAMETERS

Characteristics	Ratings	Unit
V_{DS}	-60	V
$V_{GS(th)}$	-1.0~-2.5	V
$R_{DS(on),max}$	13	$m\Omega$
I_D	-80	A
$Q_{g,typ.}$	45	nC

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVGQ06130PDTR	TO-252-2L	Q06130PD	Halogen free	Tape & Reel

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, $T_J=25^{\circ}\text{C}$)

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Gate-source Voltage	V_{GS}	--	-20	--	20	V
Drain Current (Note 1)	I_D	$T_C=25^{\circ}\text{C}$	--	--	-80	A
		$T_C=100^{\circ}\text{C}$	--	--	-56	A
Drain Current Pulsed (Note 2)	I_{DM}	$T_C=25^{\circ}\text{C}$	--	--	-320	A
Power Dissipation (Note 3)	P_D	$T_C=25^{\circ}\text{C}$	--	--	150	W
Single Pulsed Avalanche Energy	E_{AS}	$L=0.1\text{mH}$, $V_{DD}=-50\text{V}$, $R_G=25\Omega$, starting temperature $T_J=25^{\circ}\text{C}$	--	--	156	mJ
Single Pulsed Avalanche Current	I_{AS}	--	--	--	-56	A
Operation Junction Temperature Range	T_J	--	-55	--	175	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	--	-55	--	175	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Thermal Resistance, Junction-case, Bottom	$R_{\theta JC}$	--	--	--	1.0	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-ambient	$R_{\theta JA}$	--	--	--	62.0	$^{\circ}\text{C/W}$
Soldering Temperature(SMD)	T_{sld}	Reflow soldering: 10 ± 1 sec, 3times	--	--	260	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, $T_J=25^{\circ}\text{C}$)

Static characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Drain-source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-60	--	--	V
Drain-source Leakage Current	I_{DSS}	$V_{DS}=-60V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	--	--	-1.0	μA
		$V_{DS}=-60V, V_{GS}=0V, T_J=125^{\circ}\text{C}$	--	5.0	--	
Gate-source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	--	-2.5	V
Static Drain-source On State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-25A$	--	8.0	13	$m\Omega$
		$V_{GS}=-4.5V, I_D=-25A$	--	12	21	
Gate Resistance	R_g	$f=1\text{MHz}$	--	3.9	--	Ω

Dynamic characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Input Capacitance	C_{iss}	$f=1\text{MHz}, V_{GS}=0V, V_{DS}=-30V$	--	3258	--	pF
Output Capacitance	C_{oss}		--	534	--	
Reverse Transfer Capacitance	C_{rss}		--	15	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-20V, V_{GS}=-10V,$ $R_G=10\Omega, I_D=-50A$ (Notes 4, 5)	--	11	--	ns
Turn-on Rise Time	t_r		--	21	--	
Turn-off Delay Time	$t_{d(off)}$		--	68	--	
Turn-off Fall Time	t_f		--	14	--	
Total Gate Charge	Q_g	$V_{DD}=-20V, V_{GS}=-10V, I_D=-50A$ (Notes 4, 5)	--	45	--	nC
Gate-source Charge	Q_{gs}		--	15	--	
Gate-drain Charge	Q_{gd}		--	3.9	--	
Gate-plateau Voltage	$V_{plateau}$		--	4.3	--	V

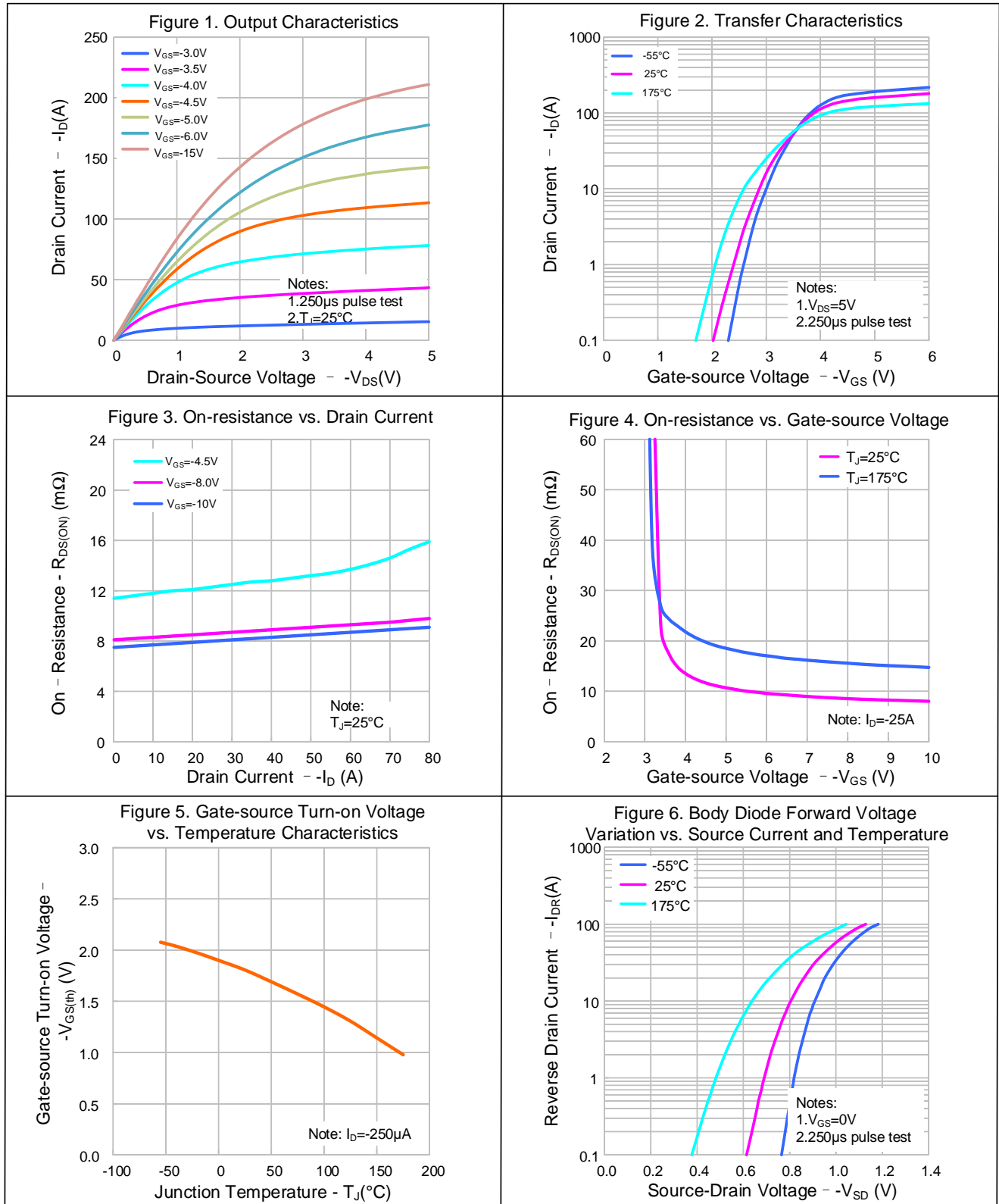
Reverse diode characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Continuous Diode Forward Current	I_S	$T_C=25^{\circ}\text{C}$, Integral reverse P-N junction diode in the MOSFET	--	--	-80	A
Diode Pulse Current	$I_{S,pulse}$		--	--	-320	
Source-Drain Diode Voltage Drop	V_{SD}	$I_S=-25A, V_{GS}=0V$	--	--	-1.4	V
Reverse Recovery Time	T_{rr}	$I_S=-50A, V_{GS}=0V,$	--	38	--	ns
Reverse Recovery Charge	Q_{rr}	$dI_F/dt=100A/\mu s$ (Note 4)	--	46	--	nC

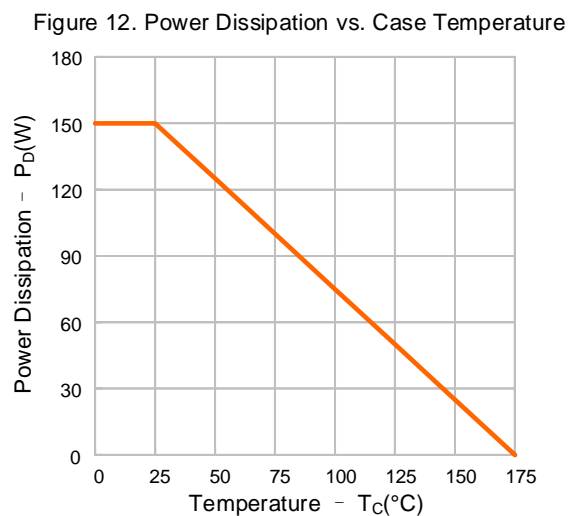
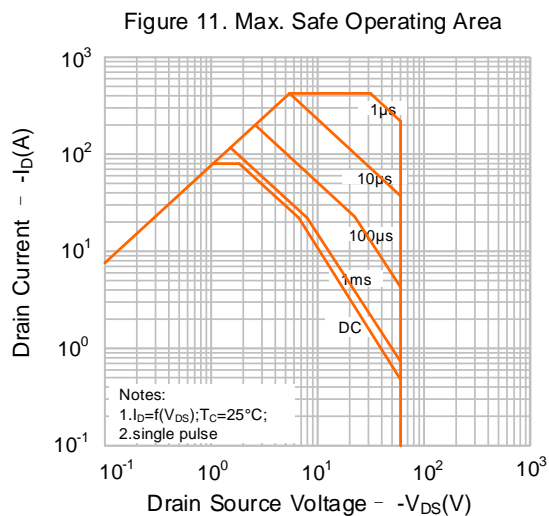
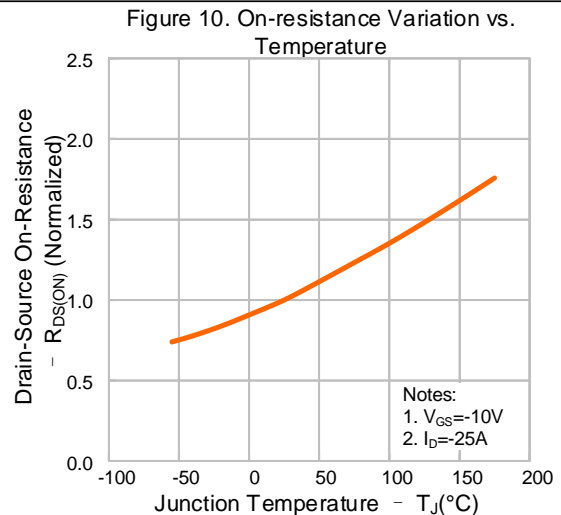
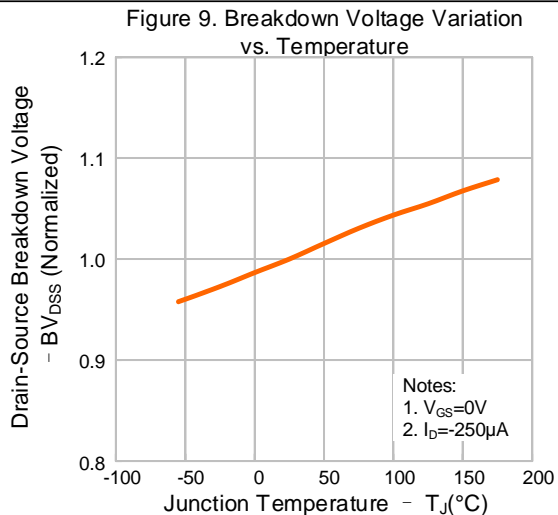
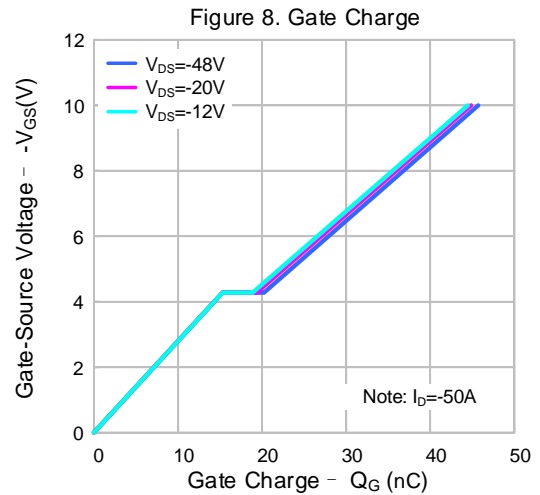
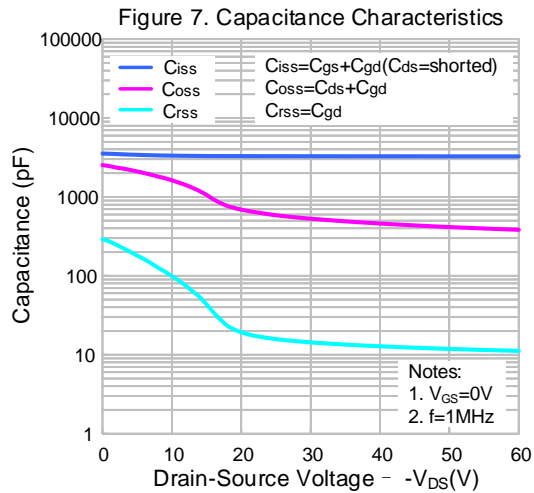
Notes:

- The rated value only refers to the maximum absolute value at the case temperature of 25°C in the specification. If the case temperature is higher than 25°C , it should be derated according to the actual environmental conditions;
- Pulse time $5\mu s$;
- The dissipation power will change with temperature, derating above 25°C : $1.0W/^{\circ}\text{C}$;
- Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;
- Essentially independent of operating temperature.

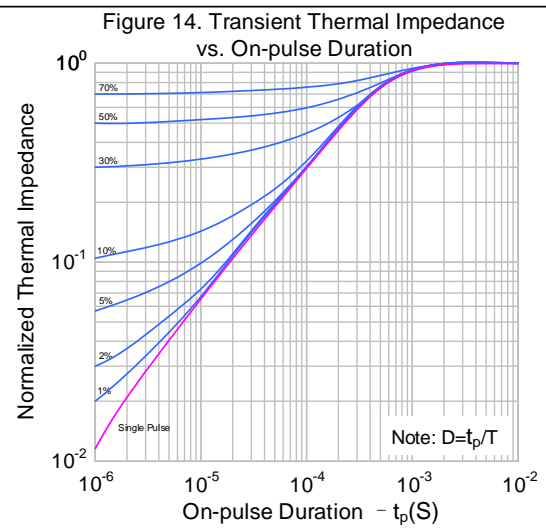
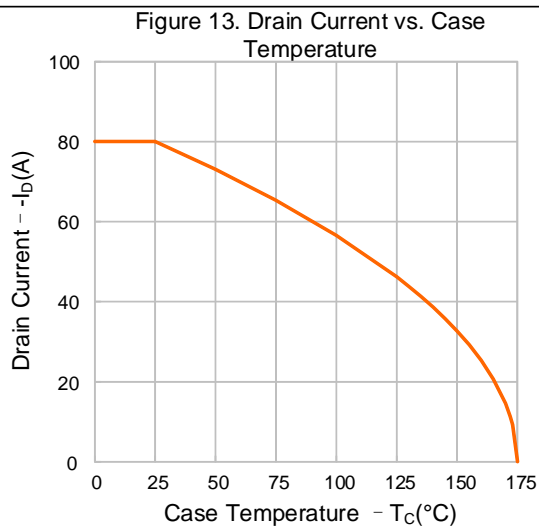
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (CONTINUED)

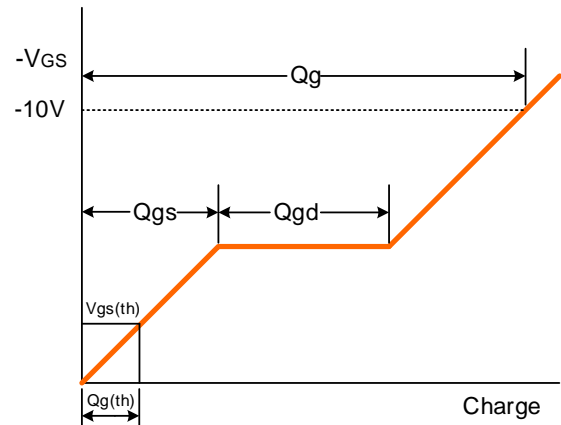
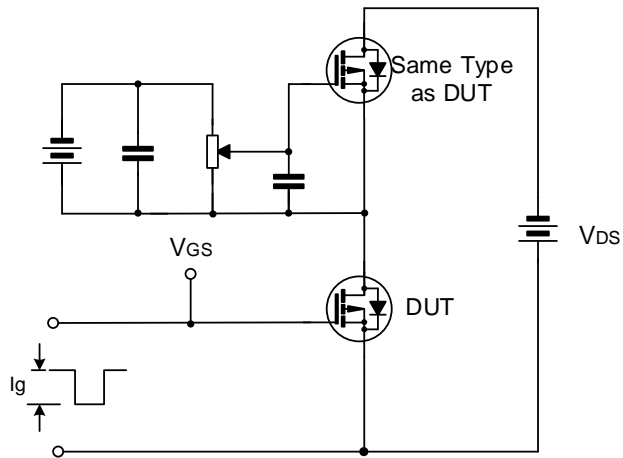


TYPICAL CHARACTERISTICS (CONTINUED)

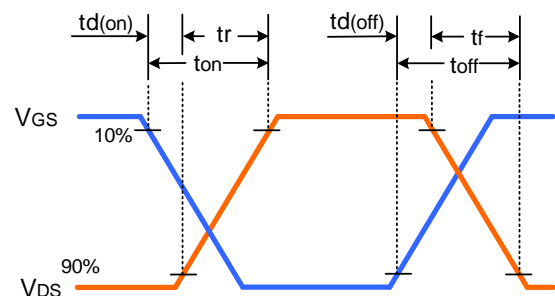
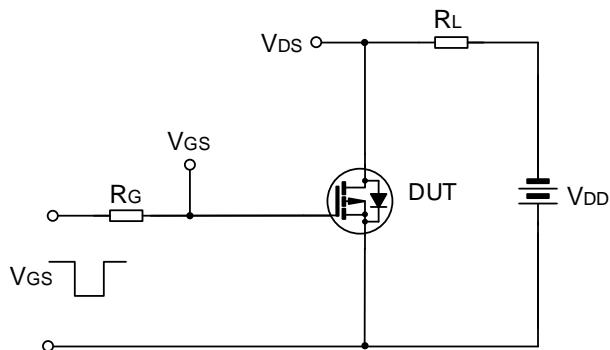


TYPICAL TEST CIRCUIT

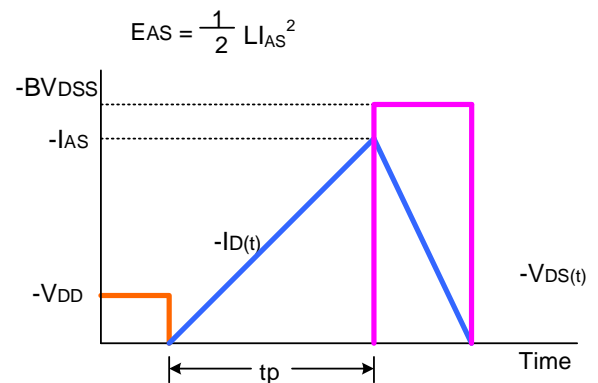
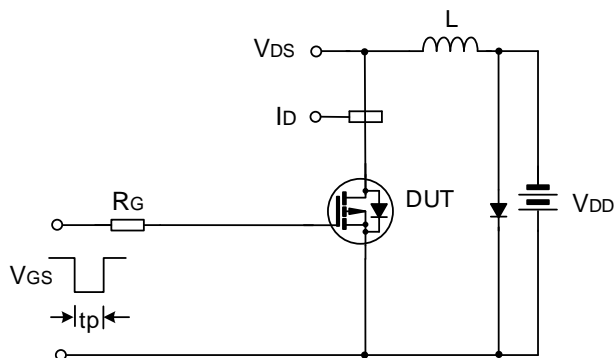
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



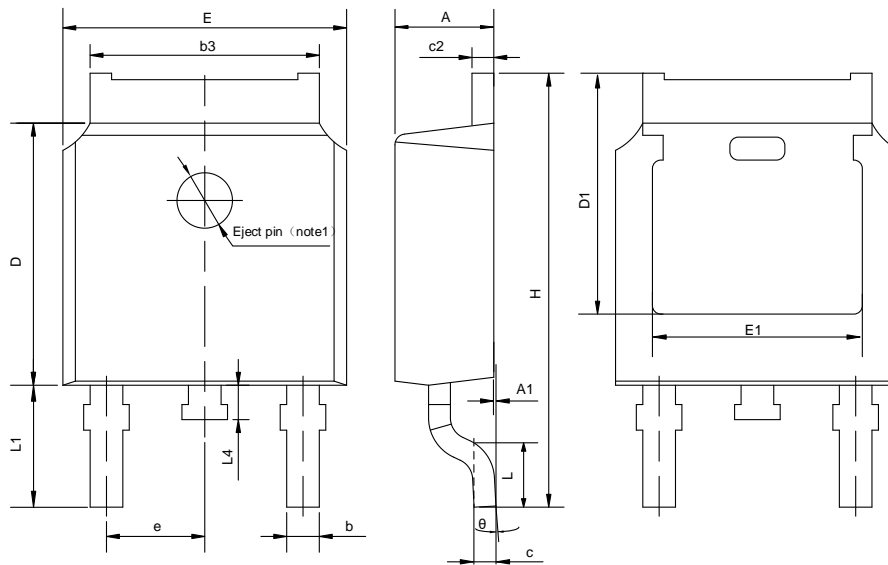
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-252-2L

UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0	—	0.10
b	0.72	0.76	0.85
b3	5.13	5.33	5.46
c	0.47	0.51	0.60
c2	0.47	0.51	0.60
D	6.00	6.10	6.20
D1	5.00	5.24	5.60
E	6.50	6.60	6.70
E1	5.15	5.35	5.55
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.70	2.90	3.10
L4	0.60	0.80	1.00
θ	0°	—	8°



MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Important notice :

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Rev.: 1.3

Revision History:

1. Update the feature
2. Update the curve
3. Update the important notice

Rev.: 1.2

Revision History:

1. Delete the wave soldering condition
2. Add Figure 13
3. Update the typical test circuit
4. Update the important notice

Rev.: 1.1

Revision History:

1. Add E_{AS} and I_{AS} when $L=0.1mH$
2. Update package outline

Rev.: 1.0

Revision History:

1. First release