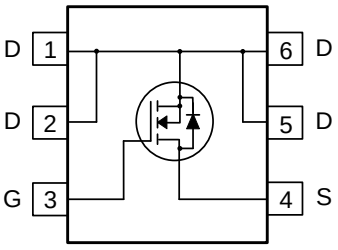
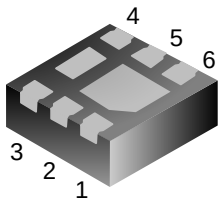
12A, 30V N-CHANNEL MOSFET

DESCRIPTION

The SVT03120NL2 is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance.

This device is widely used in the fields of uninterruptible power supplies and power management of inverter systems.





DFN-6-2x2x0.75-0.65

FEATURES

- 12A, 30V, $R_{DS(on)(typ.)}$=9.5mΩ@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability
- 100% avalanche tested
- Pb-free lead plating
- RoHS compliant

KEY PERFORMANCE PARAMETERS

Characteristics	Ratings	Unit
V_{DS}	30	V
$V_{GS(th)}$	1.0~1.8	V
$R_{DS(on),max}$	12	mΩ
I_D	12	A
$Q_{g.typ}$	11	nC

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVT03120NL2TR	DFN-6-2x2x0.75-0.65	03	Halogen free	Tape&Reel

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, T_J=25°C)

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Drain-source Voltage	V_{DS}	--	30	--	--	V
Gate-source Voltage	V_{GS}	--	-20	--	20	V
Drain Current	I_D	T_A=25°C, t≤5s	--	--	12	A
		T_A=100°C	--	--	7.6	A
Drain Current Pulsed (Note 1)	I_{DM}	T_A=25°C	--	--	48	A
Power Dissipation (Note 2)	P_D	T_A=25°C	--	--	3.3	W
Single Pulsed Avalanche Energy	E_{AS}	L=0.5mH, V_{DD}=10V, R_G=25Ω, starting temperature T_J=25°C	--	--	36	mJ
Single Pulsed Avalanche Current	I_{AS}	--	--	--	12	A
Operation Junction Temperature Range	T_J	--	-55	--	150	°C
Storage Temperature Range	T_{stg}	--	-55	--	150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Thermal Resistance, Junction-ambient	$R_{\theta JA}$	--	--	--	270	°C/W
		t≤5s	--	--	38	°C/W
Soldering Temperature(SMD)	T_{sold}	Reflow soldering: 10±1 sec, 3times	--	--	260	°C

ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, T_J=25°C)

Static characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Drain-source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	30	--	--	V
Drain-source Leakage Current	I_{DSS}	V_{DS}=30V, V_{GS}=0V, T_J=25°C	--	--	1.0	μA
		V_{DS}=30V, V_{GS}=0V, T_J=125°C	--	0.5	--	μA
Gate-source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	1.0	--	1.8	V
Static Drain-source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=7.0A	--	9.5	12	mΩ
		V_{GS}=4.5V, I_D=5.0A	--	13.5	16.5	mΩ
Gate Resistance	R_G	f=1MHz	--	2.3	--	Ω

Dynamic characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Input Capacitance	C_{iss}	f=1MHz, V_{GS}=0V, V_{DS}=15V	--	876	--	pF
Output Capacitance	C_{oss}		--	149	--	
Reverse Transfer Capacitance	C_{rss}		--	137	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=20V, V_{GS}=10V, R_G=6Ω, I_D=6.0A (Notes 3, 4)	--	4.7	--	ns
Turn-on Rise Time	t_r		--	34	--	
Turn-off Delay Time	$t_{d(off)}$		--	33	--	
Turn-off Fall Time	t_f		--	15	--	
Total Gate Charge	Q_g	V_{DD}=15V, V_{GS}=4.5V, I_D=6.0A (Notes 3, 4)	--	11	--	nC
Gate-source Charge	Q_{gs}		--	2.7	--	
Gate-drain Charge	Q_{gd}		--	5.1	--	
Gate-plateau Voltage	$V_{plateau}$		--	2.7	--	V

Reverse diode characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Continuous Diode Forward Current	I_S	T_C=25°C, Integral reverse P-N junction diode in the MOSFET	--	--	12	A
Diode Pulse Current	$I_{S,pulse}$		--	--	48	
Diode Forward Voltage	V_{SD}	I_S=1.9A, V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=6.0A, V_{GS}=0V, V_R=30V dIF/dt=100A/μs (Note 3)	--	10	--	ns
Reverse Recovery Charge	Q_{rr}		--	4.2	--	nC

Notes:

1. Pulse time 5μs;
2. The dissipation power will change with temperature, derating above 25°C: 0.03W/°C;
3. Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
4. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. Output Characteristics

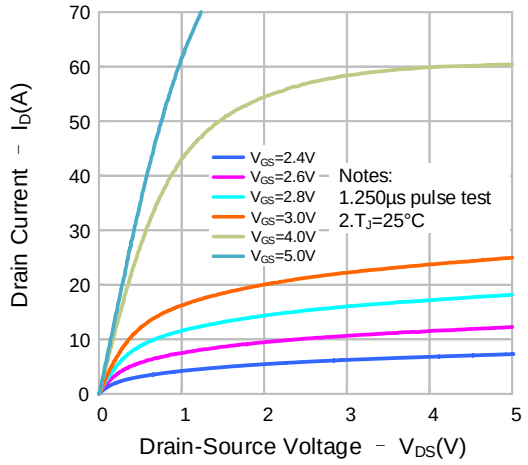


Figure 2. Transfer Characteristics

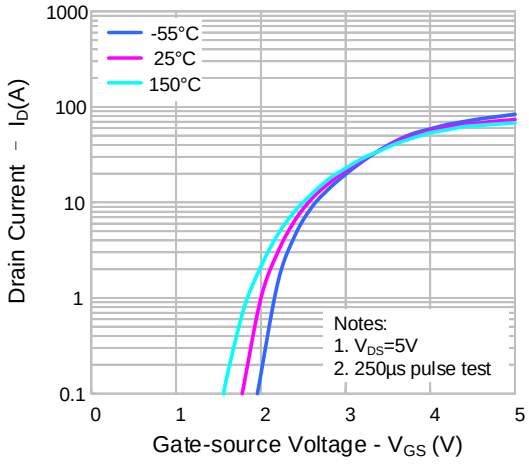


Figure 3. On-resistance vs. Drain Current

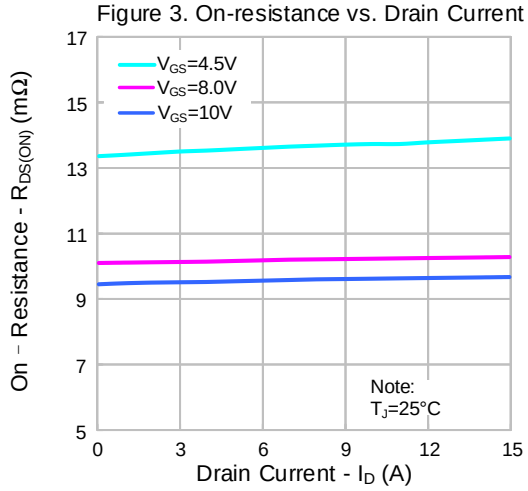


Figure 4. On-resistance vs. Gate-source Voltage

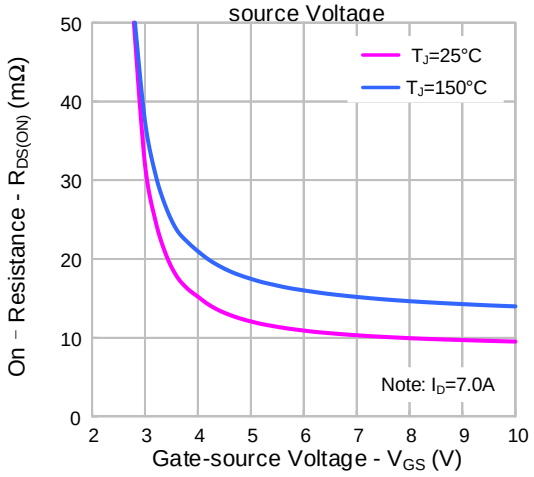


Figure 5. Turn-on Voltage vs. Temperature characteristics

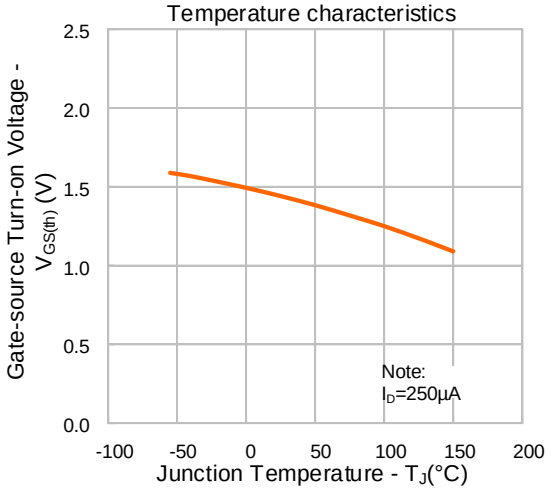
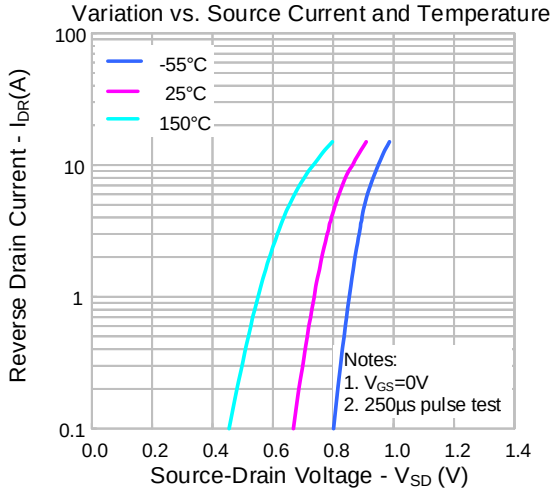


Figure 6. Body Diode Forward Voltage Variation vs. Source Current and Temperature



TYPICAL CHARACTERISTICS (CONTINUED)

Figure 7. Capacitance Characteristics

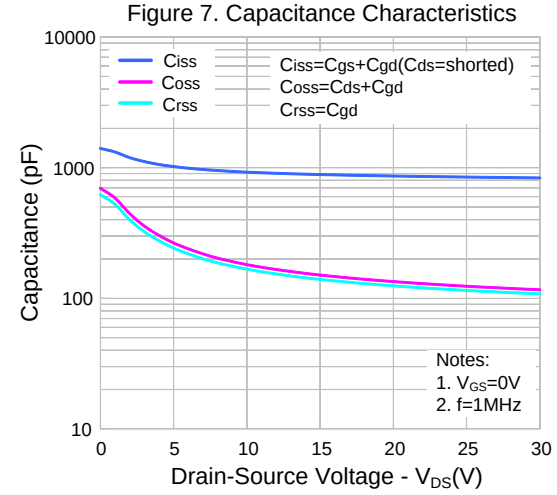


Figure 8. Gate Charge

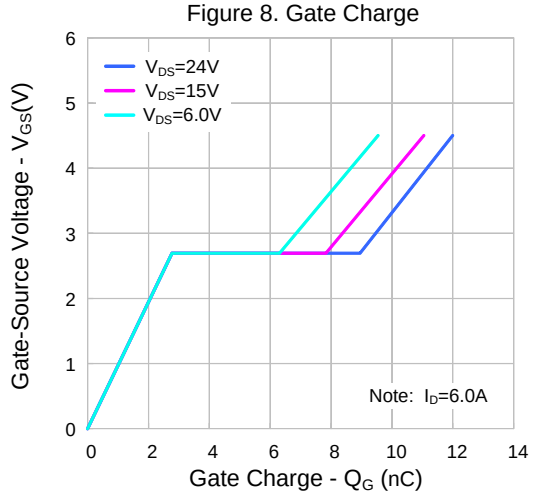


Figure 9. Breakdown Voltage Variation vs. Temperature

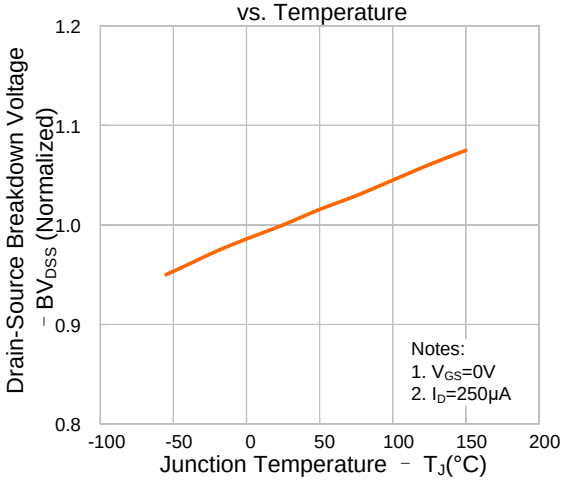


Figure 10. On-resistance Variation vs. Temperature

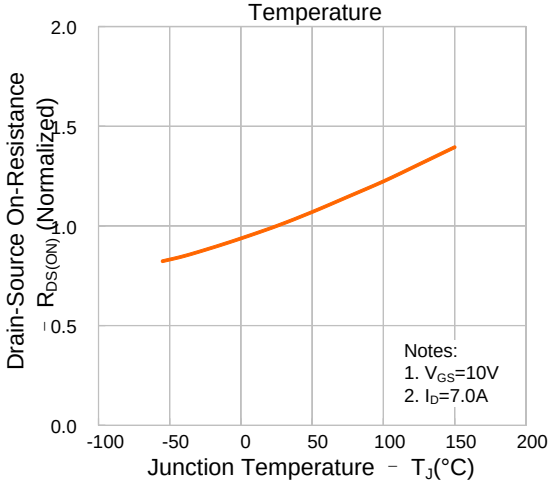


Figure 11. Max. Safe Operating Area

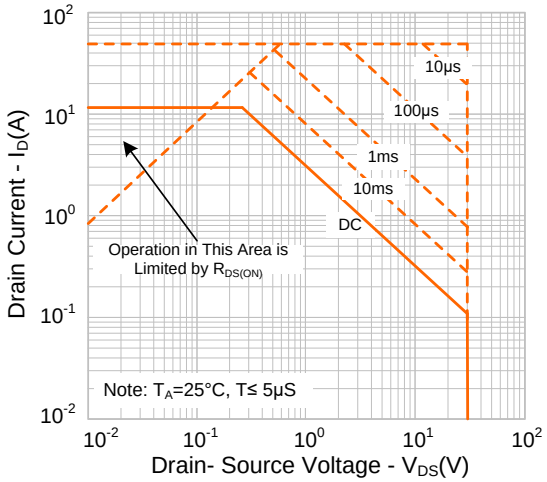
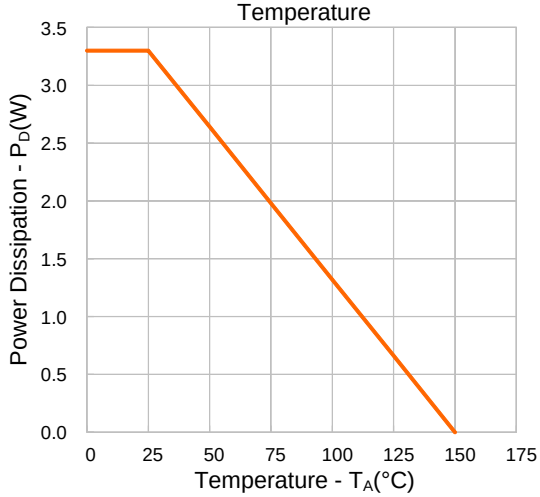
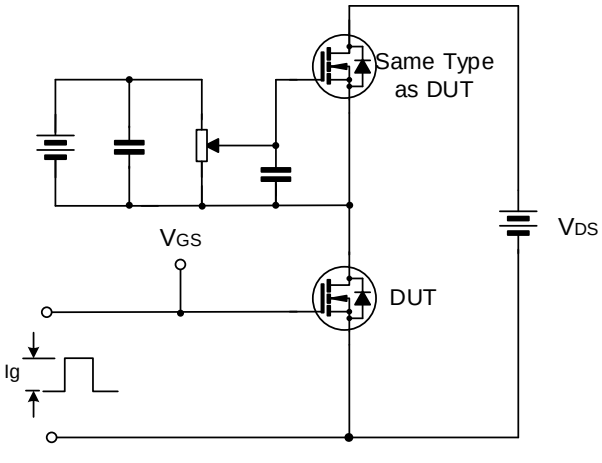


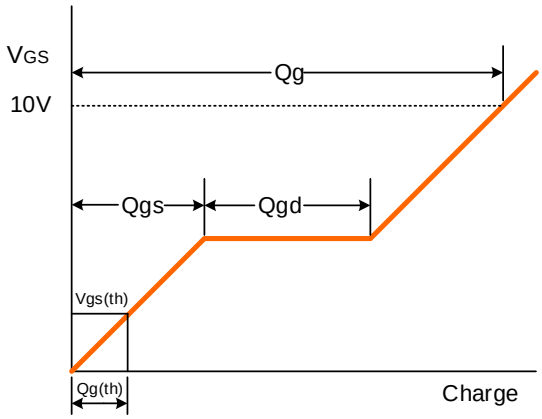
Figure 12. Power Dissipation vs. Case Temperature



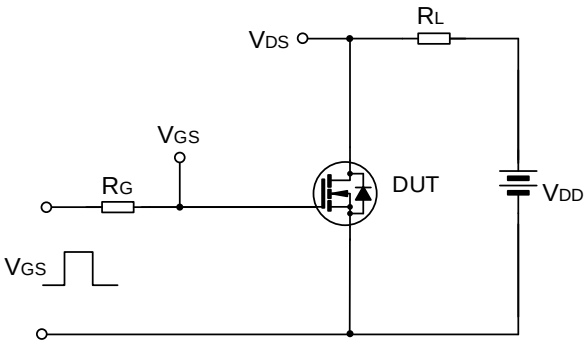
TYPICAL TEST CIRCUIT

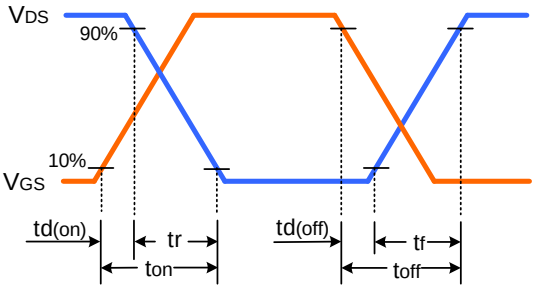
Gate Charge Test Circuit & Waveform



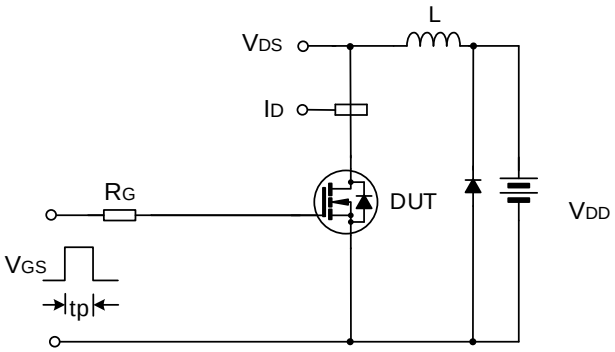


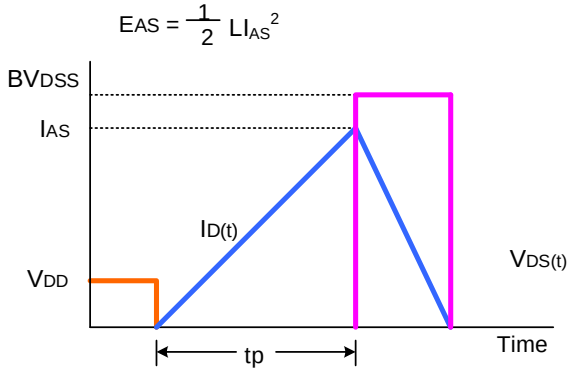
Resistive Switching Test Circuit & Waveform





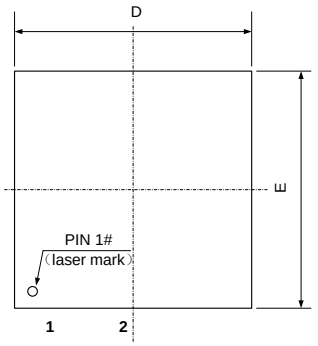
Unclamped Inductive Switching Test Circuit & Waveform



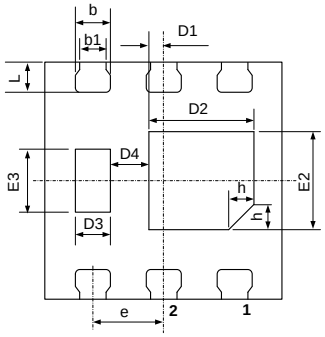


PACKAGE OUTLINE

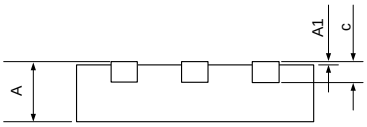
DFN-6-2x2x0.75-0.65 **UNIT: mm**



Top View



Bottom View



Side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.25	0.30	0.35
b1		0.20REF	
c		0.203REF	
D	1.90	2.00	2.10
D1	0.08	0.125	0.18
D2	0.85	0.90	0.95
D3	0.25	0.30	0.35
D4	0.33	0.375	0.43
e		0.65BSC	
E	1.90	2.00	2.10
E2	0.95	1.00	1.05
E3	0.55	0.60	0.65
L	0.20	0.25	0.30
h		0.25REF	

MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Important notice :

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Rev.: 1.2

Revision History:

1. Update the value of $R_{DS(on)}$

Rev.: 1.1

Revision History:

1. Delete wave soldering condition
2. Update the typical test circuit
3. Update the important notice

Rev.: 1.0

Revision History:

1. First release