



100A, 30V N-CHANNEL MOSFET

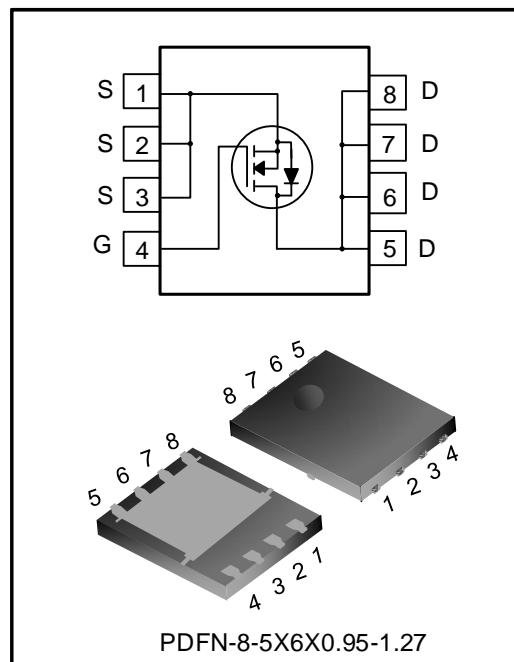
DESCRIPTION

The SVT035R5NL5 is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance.

This device is widely used in the fields of uninterruptible power supplies and power management of inverter systems.

FEATURES

- 100A, 30V, $R_{DS(on)(typ.)}=4.0\text{m}\Omega @ V_{GS}=10\text{V}$
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVT035R5NL5TR	PDFN-8-5X6X0.95-1.27	035R5NL5	Halogen free	Tape&Reel

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, $T_A=25^\circ\text{C}$)

Characteristics	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current	I_D	100	A
		63	
Drain Current Pulsed	I_{DM}	400	A
Power Dissipation ($T_C=25^\circ\text{C}$) -Derate above 25°C	P_D	66	W
		0.53	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy (Note 1)	E_{AS}	200	mJ
Operation Junction Temperature Range	T_J	-55~+150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55~+150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.9	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$



ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, $T_J=25^\circ\text{C}$)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	30	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{\text{DS}}=30\text{V}, V_{\text{GS}}=0\text{V}$	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	--	--	± 100	nA
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}}=V_{\text{DS}}, I_{\text{D}}=250\mu\text{A}$	1	1.6	2.5	V
Static Drain-Source On State Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}$ $V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=15\text{A}$	--	4.0	5.5	$\text{m}\Omega$
Gate Resistance	R_{G}	$f=1\text{MHz}$	--	4.9	--	Ω
Input Capacitance	C_{iss}	$f=1\text{MHz}, V_{\text{GS}}=0\text{V}, V_{\text{DS}}=25\text{V}$	--	2190	--	pF
Output Capacitance	C_{oss}		--	268	--	
Reverse Transfer Capacitance	C_{rss}		--	206	--	
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=20\text{V}, V_{\text{GS}}=4.5\text{V}, R_{\text{G}}=1.8\Omega, I_{\text{D}}=60\text{A}$ (Notes 2,3)	--	12	--	ns
Turn-on Rise Time	t_{r}		--	88	--	
Turn-off Delay Time	$t_{\text{d}(\text{off})}$		--	140	--	
Turn-off Fall Time	t_{f}		--	83	--	
Total Gate Charge	Q_{g}	$V_{\text{DD}}=24\text{V}, V_{\text{GS}}=10\text{V}, I_{\text{D}}=30\text{A}$ (Notes 2,3)	--	47	--	nC
Gate-Source Charge	Q_{gs}		--	8.5	--	
Gate-Drain Charge	Q_{gd}		--	9.9	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

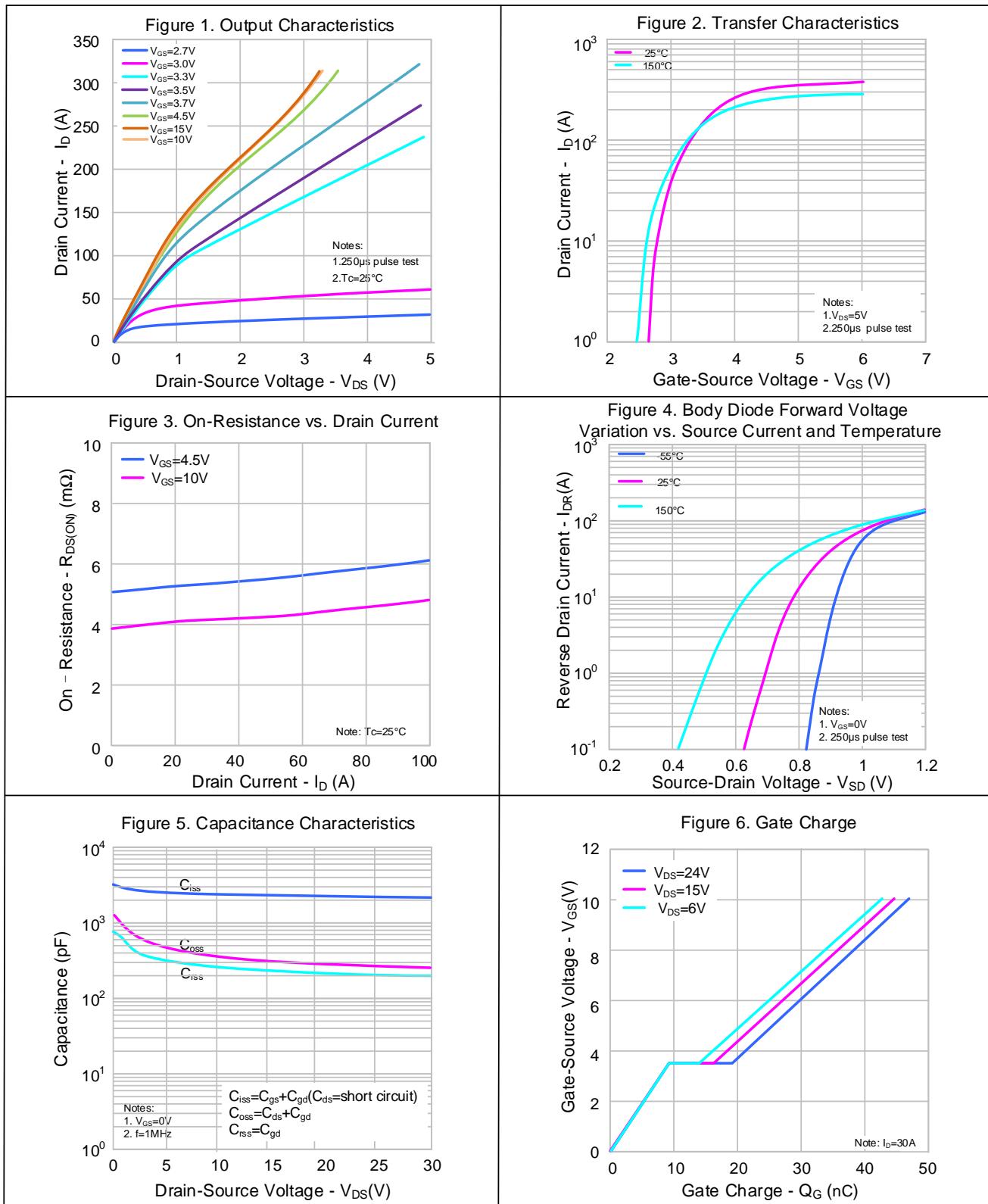
Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_{s}	Integral Reverse P-N Junction Diode in the MOSFET	--	--	100	A
Pulsed Source Current	I_{SM}		--	--	400	
Diode Forward Voltage	V_{SD}	$I_{\text{s}}=20\text{A}, V_{\text{GS}}=0\text{V}$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_{\text{s}}=30\text{A}, V_{\text{GS}}=0\text{V}, \text{dI}/\text{dt}=100\text{A}/\mu\text{s}$ (Notes 2)	--	16	--	ns
Reverse Recovery Charge	Q_{rr}		--	6.9	--	nC

Notes:

1. $L=0.5\text{mH}, V_{\text{DD}}=15\text{V}, V_{\text{G}}=10\text{V}, R_{\text{G}}=25\Omega$, starting $T_J=25^\circ\text{C}$;
2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$;
3. Essentially independent of operating temperature.



TYPICAL CHARACTERISTICS





TYPICAL CHARACTERISTICS (CONTINUED)

Figure 7. Breakdown Voltage vs.
Temperature Characteristics

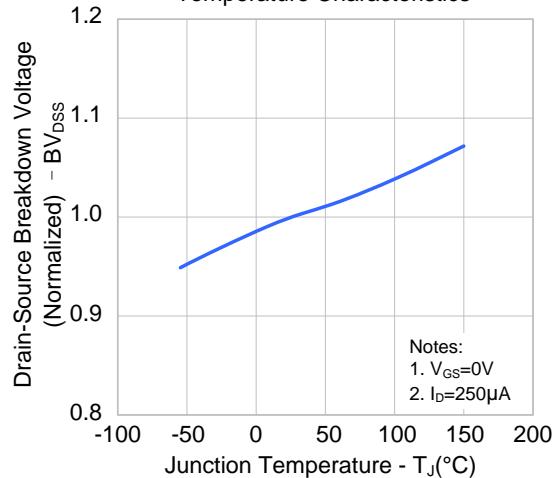


Figure 8. On-Resistance vs.
Temperature Characteristics

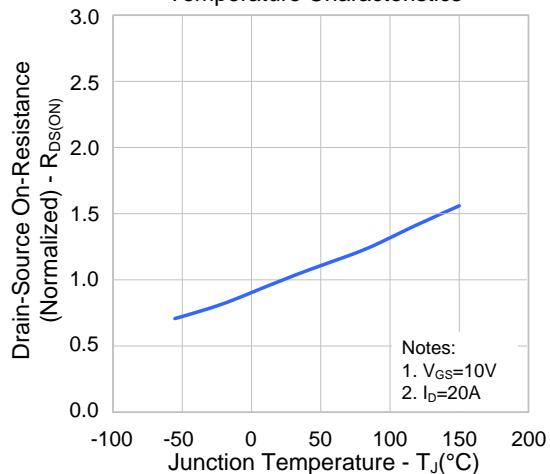
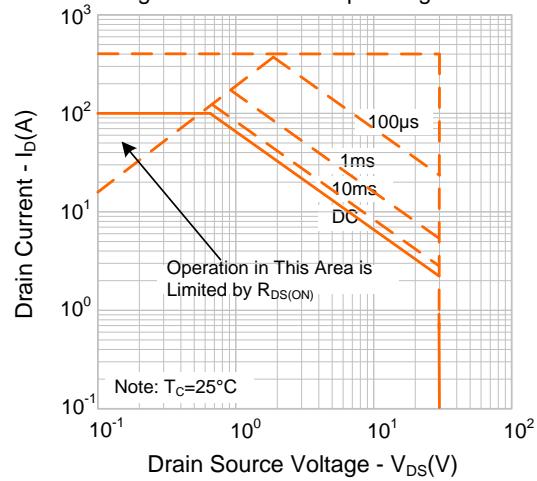
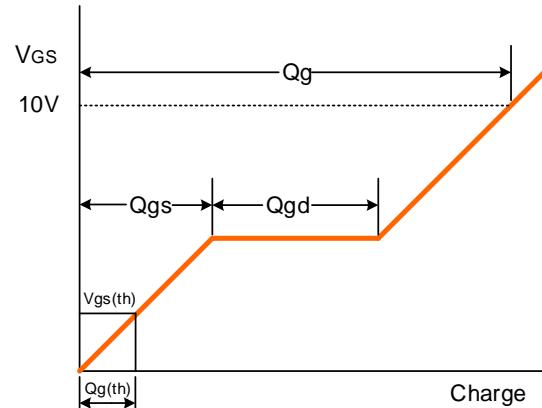
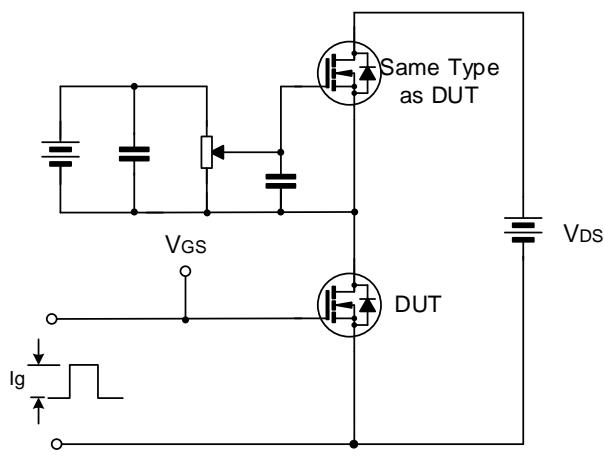


Figure 9. Max. Safe Operating Area

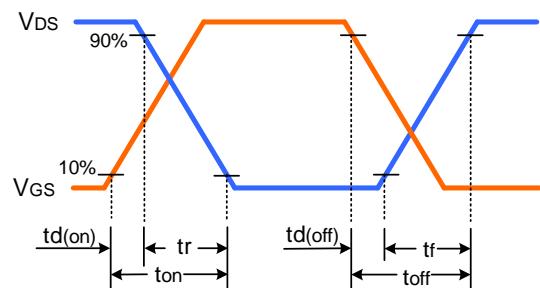
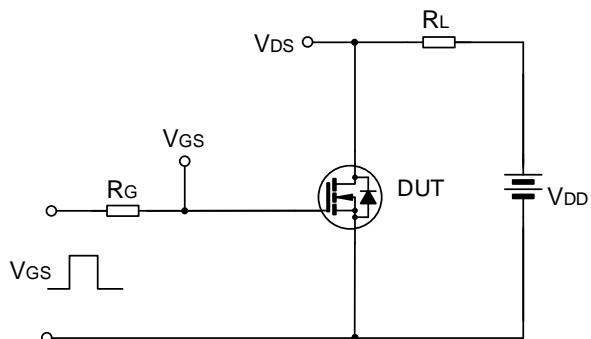


TYPICAL TEST CIRCUIT

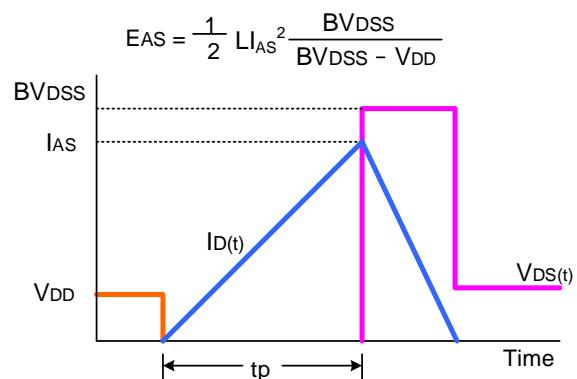
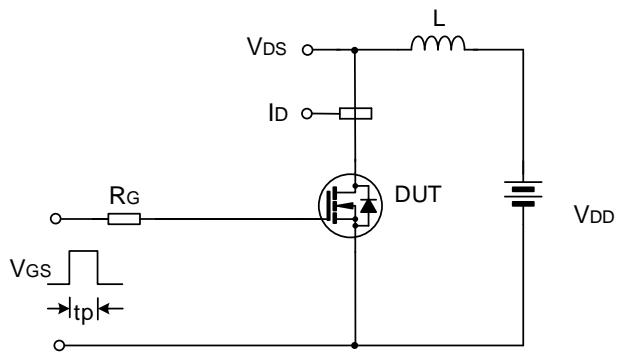
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform

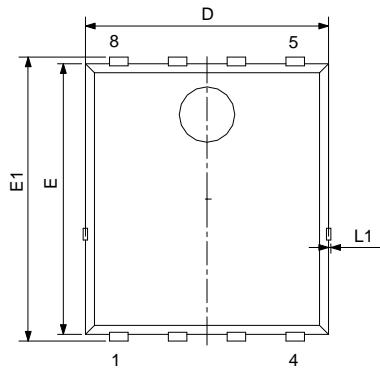




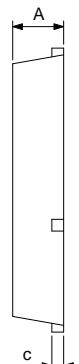
PACKAGE OUTLINE

PDFN-8-5X6X0.95-1.27

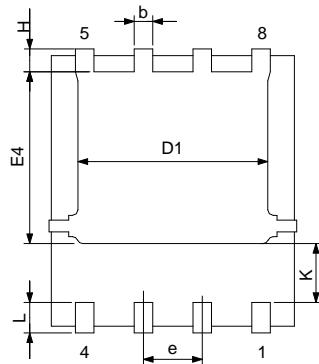
UNIT: mm



Top View



Side View



Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.90	—	1.20
c	0.154	0.25	0.354
D	4.80	—	5.40
E	5.66	—	6.06
D1	3.76	—	4.30
E1	5.90	—	6.35
b	0.30	—	0.55
K	1.10	1.30	1.50
e	1.07	1.27	1.37
E4	3.34	—	3.92
L	0.30	0.60	0.71
L1	—	—	0.12
H	0.40	—	0.71

Important notice :

1. The instructions are subject to change without notice!
2. Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current. Please read the instructions carefully before using our products, including the circuit operation precautions.
3. Our products are consumer electronic products or the other civil electronic products.
4. When using our products, please do not exceed the maximum rating of the products, otherwise the reliability of the whole machine will be affected. There is a certain possibility of failure or malfunction of any semiconductor product under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design, sample and whole machine manufacturing, so as to avoid potential failure risk that may cause personal injury or property loss.
5. It is strongly recommended to identify the trademark when buying our products. Please contact us if there is any question.
6. Product promotion is endless, our company will wholeheartedly provide customers with better products!
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Rev.: **1.1**

Revision History:

1. Update package outline
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Rev.: **1.0**

Revision History:

1. First release
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