

## 80A, 60V N-CHANNEL MOSFET

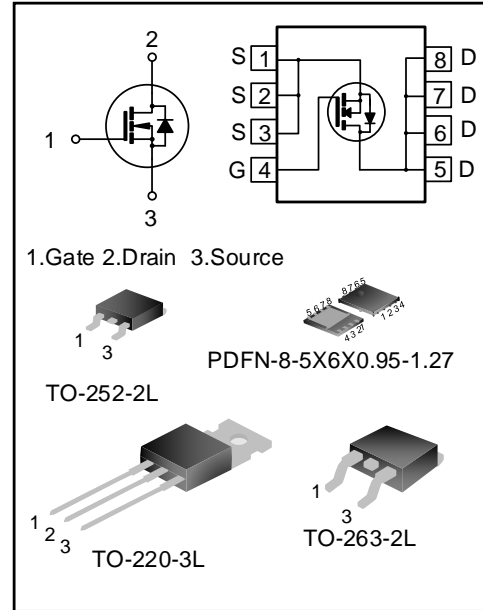
### DESCRIPTION

SVT068R5NT/D/S/L5 is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance.

These devices are widely used in UPS, Power Management for Inverter Systems.

### FEATURES

- ◆ 80A, 60V,  $R_{DS(on)(typ.)}=7.0m\Omega@V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low Crss
- ◆ Fast switching
- ◆ Improved dv/dt capability



### ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVT068R5NT	TO-220-3L	068R5NT	Pb free	Tube
SVT068R5NDTR	TO-252-2L	068R5ND	Halogen free	Tape&Reel
SVT068R5NSTR	TO-263-2L	068R5NS	Halogen free	Tape&Reel
SVT068R5NL5TR	PDFN-8-5x6x0.95-1.27	068R5NL5	Halogen free	Tape&Reel

**ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED,  $T_C=25^\circ\text{C}$ )**

Characteristics	Symbol	Ratings			Unit
		SVT068R5NT/S	SVT068R5ND	SVT068R5NL5	
Drain-Source Voltage	$V_{DS}$	60			V
Gate-Source Voltage	$V_{GS}$	$\pm 20$			V
Drain Current	$I_D$	$T_C=25^\circ\text{C}$			A
		$T_C=100^\circ\text{C}$			
Drain Current Pulsed	$I_{DM}$	320			A
Power Dissipation ( $T_C=25^\circ\text{C}$ ) -Derate above $25^\circ\text{C}$	$P_D$	158	107	100	W
		1.05	0.7	0.67	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy (Note 1)	$E_{AS}$	389			mJ
Operation Junction Temperature Range	$T_J$	-55~+175			$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-55~+175			$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

Characteristics	Symbol	Ratings			Unit
		SVT068R5NT/S	SVT068R5ND	SVT068R5NL5	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.95	1.4	1.5	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.0	50.0	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED,  $T_C=25^\circ\text{C}$ )**

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	60	--	--	V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$	--	--	1.0	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	--	--	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2	--	4	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	--	7.0	8.5	$m\Omega$
Gate Resistance	$R_G$	$f=1MHz$	--	5.5	--	$\Omega$
Input Capacitance	$C_{iss}$	$f=1MHz, V_{GS}=0V,$ $V_{DS}=30V$	--	4890	--	pF
Output Capacitance	$C_{oss}$		--	235	--	
Reverse Transfer Capacitance	$C_{rss}$		--	170	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, V_{GS}=10V,$ $R_G=3\Omega, I_D=30A$ (Notes 2,3)	--	16	--	ns
Turn-on Rise Time	$t_r$		--	44	--	
Turn-off Delay Time	$t_{d(off)}$		--	93	--	
Turn-off Fall Time	$t_f$		--	26	--	
Total Gate Charge	$Q_g$	$V_{DD}=48V, V_{GS}=10V,$ $I_D=20A$ (Notes 2,3)	--	89	--	nC
Gate-Source Charge	$Q_{gs}$		--	26	--	
Gate-Drain Charge	$Q_{gd}$		--	20	--	

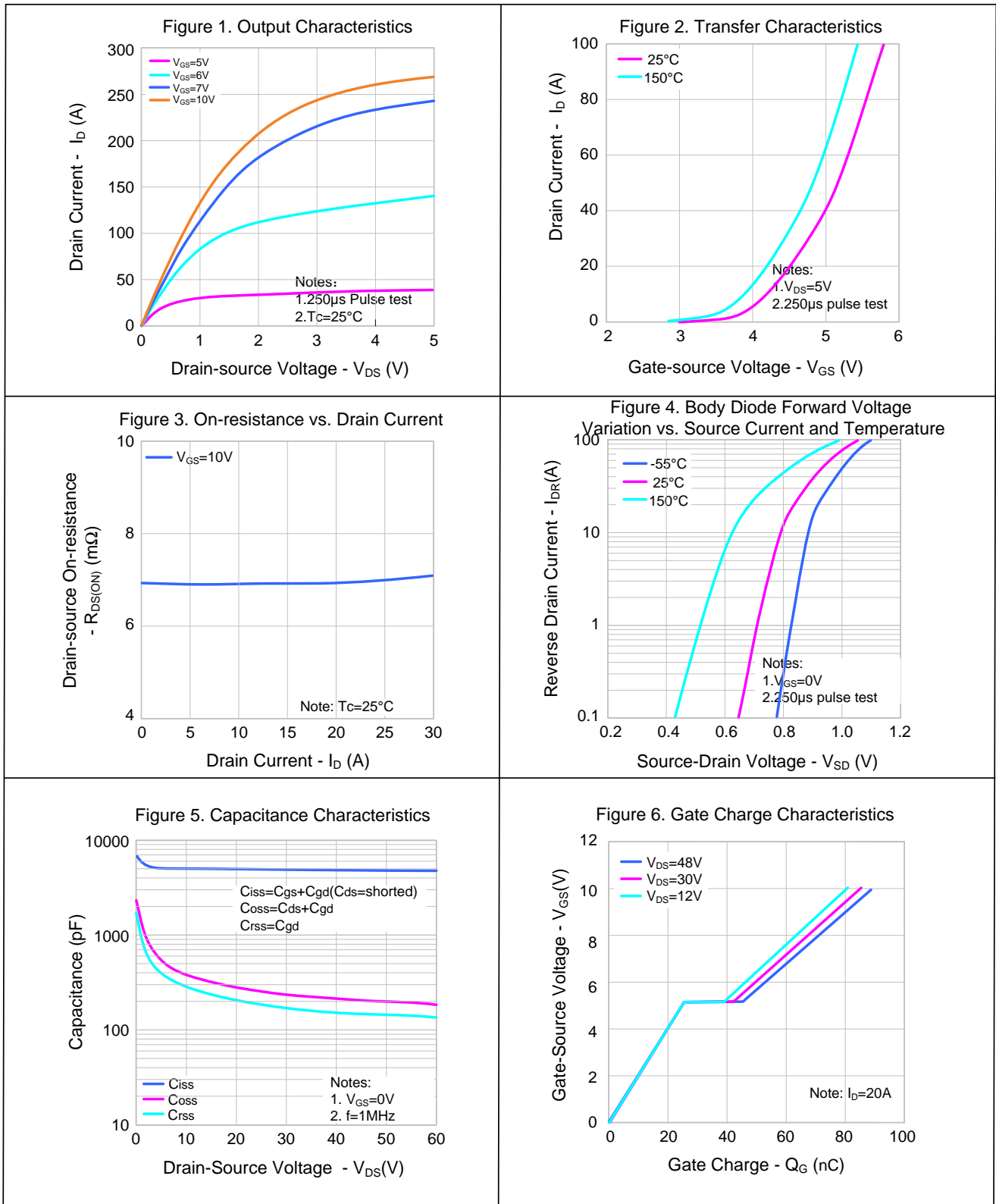
**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS**

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	$I_S$	Integral Reverse P-N Junction Diode in the MOSFET	--	--	60	A
Pulsed Source Current	$I_{SM}$		--	--	240	
Diode Forward Voltage	$V_{SD}$	$I_S=20A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	$T_{rr}$	$I_S=20A, V_{GS}=0V,$	--	29	--	ns
Reverse Recovery Charge	$Q_{rr}$	$dI_F/dt=100A/\mu s$ (Note 2)	--	38	--	nC

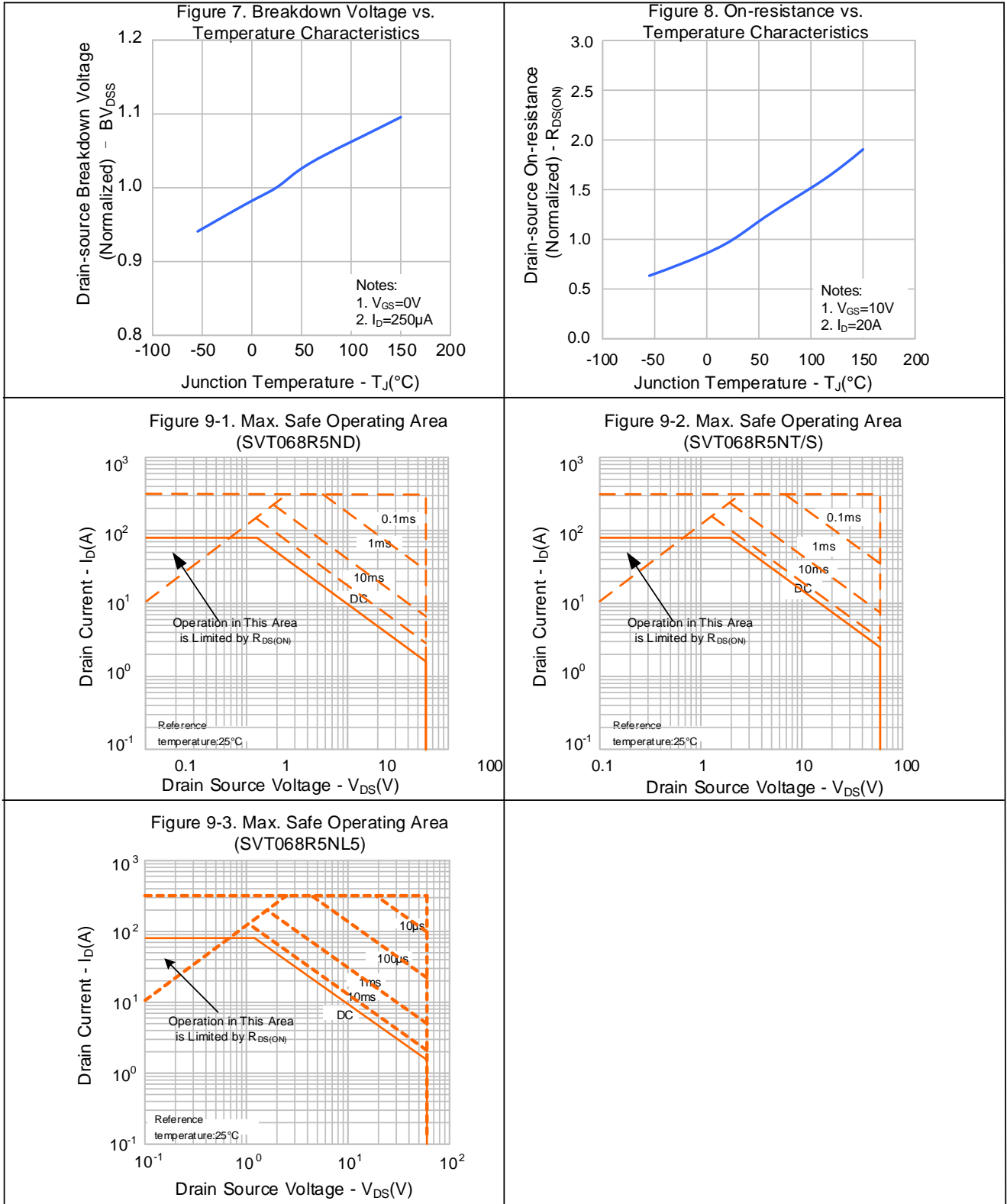
Notes:

- $L=0.5mH, V_{DD}=50V, R_G=10\Omega$ , starting  $T_J=25^\circ\text{C}$ ;
- Pulse Test: Pulse width  $\leq 300\mu s$ , Duty cycles  $\leq 2\%$ ;
- Essentially independent of operating temperature.

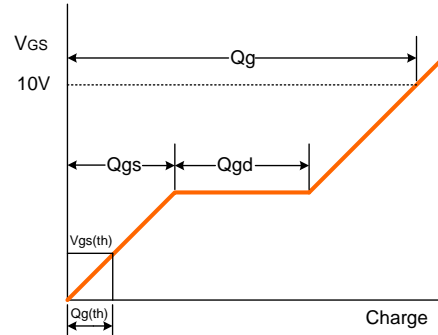
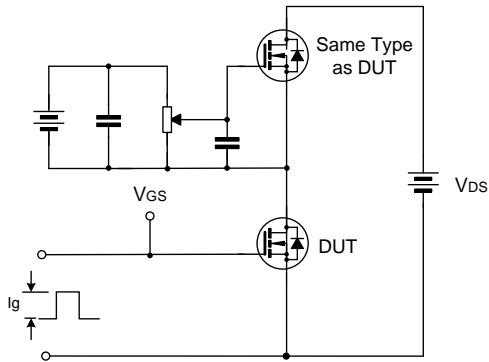
**TYPICAL CHARACTERISTICS**



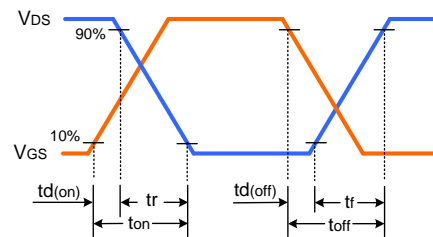
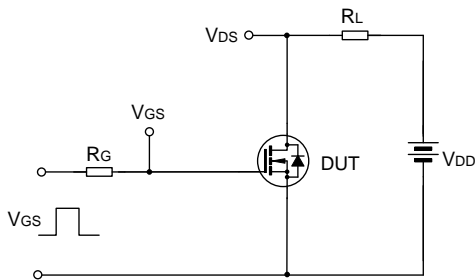
**TYPICAL CHARACTERISTICS (CONTINUED)**



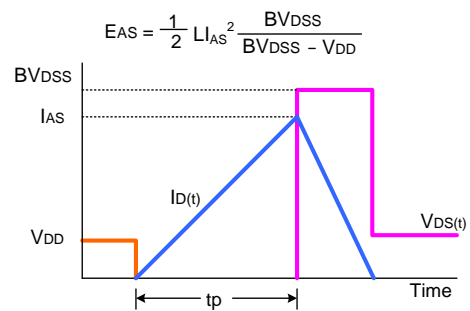
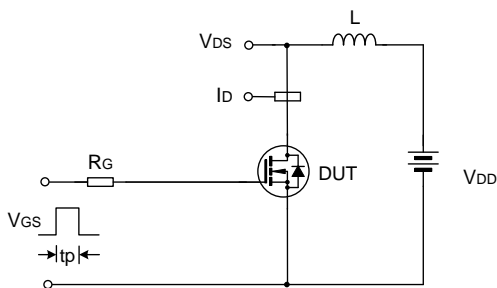
**TYPICAL TEST CIRCUIT**



Gate Charge Test Circuit & Waveform

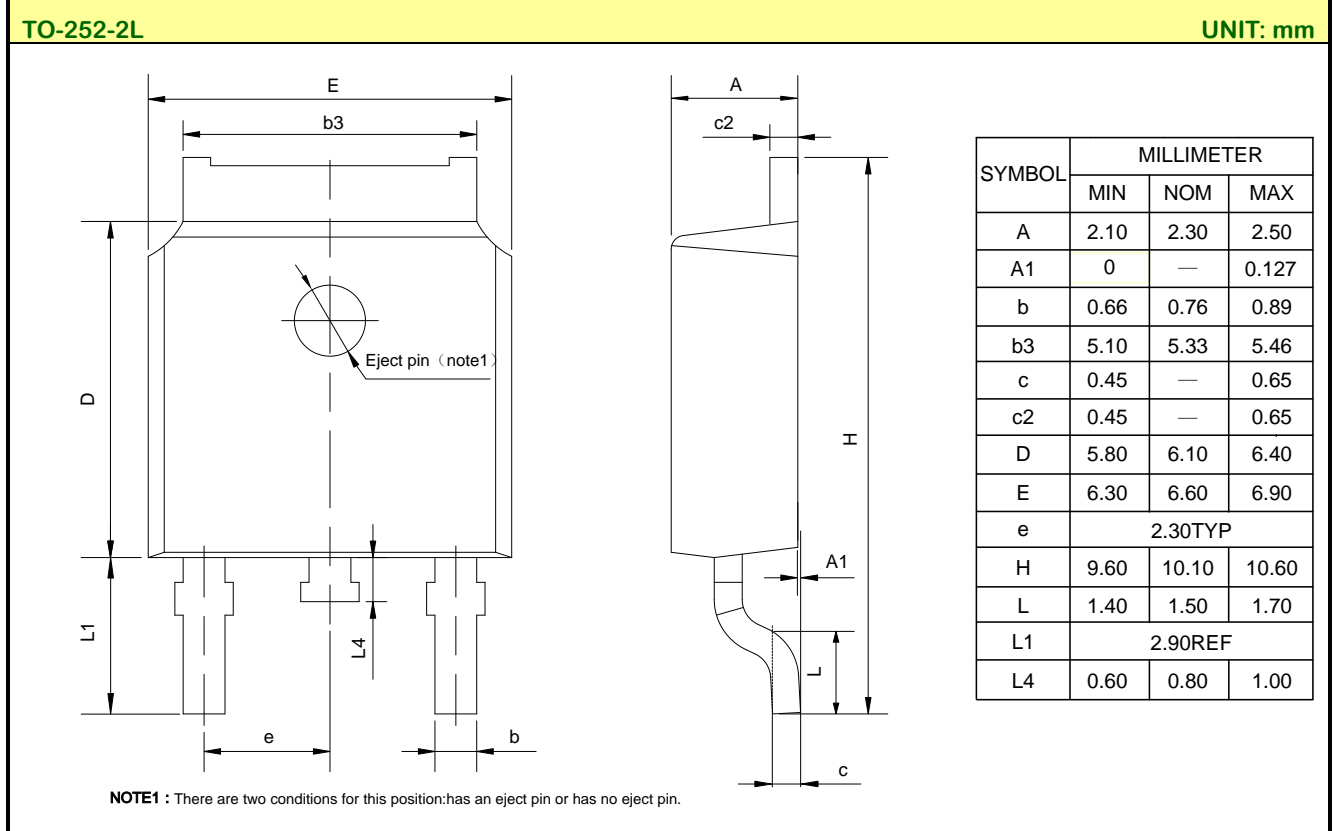
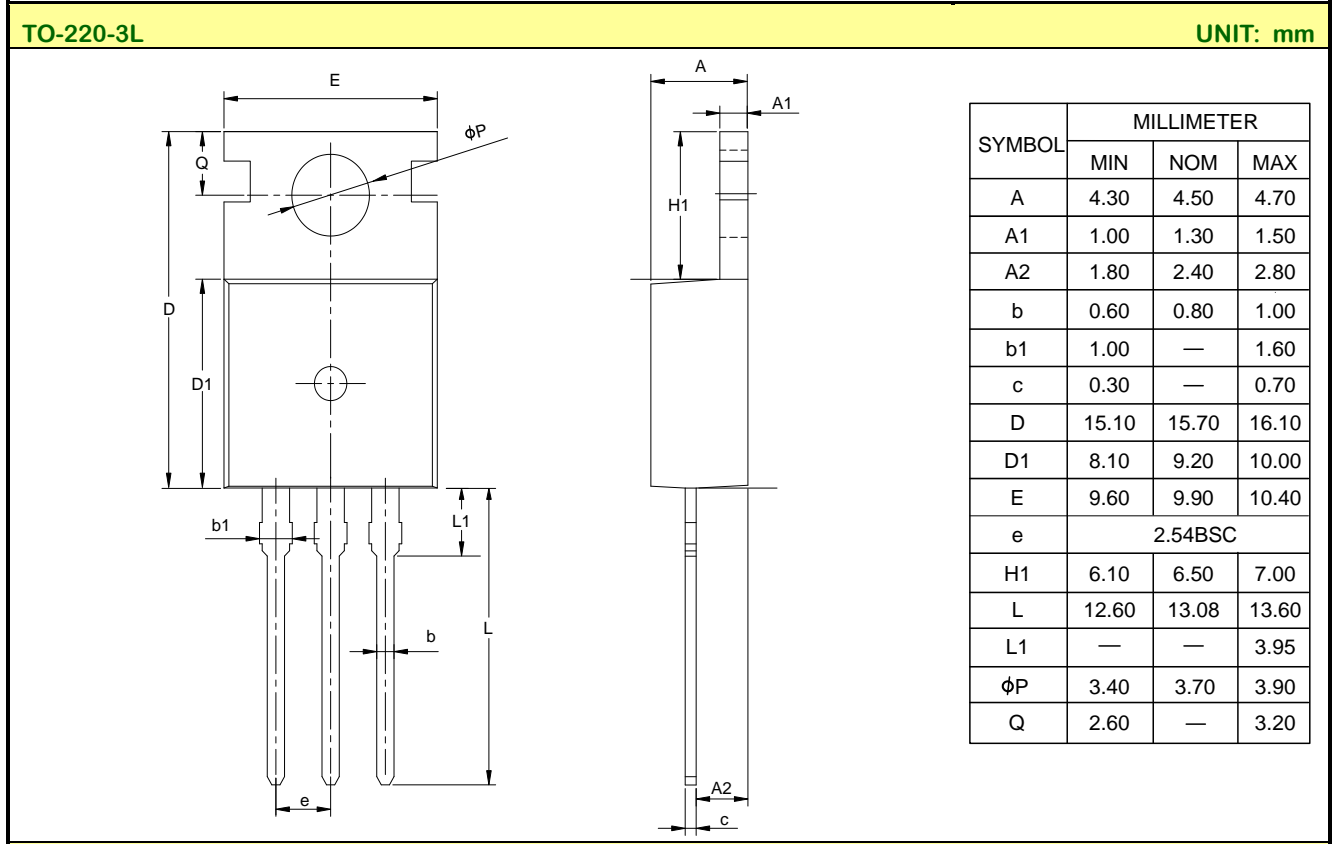


Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform

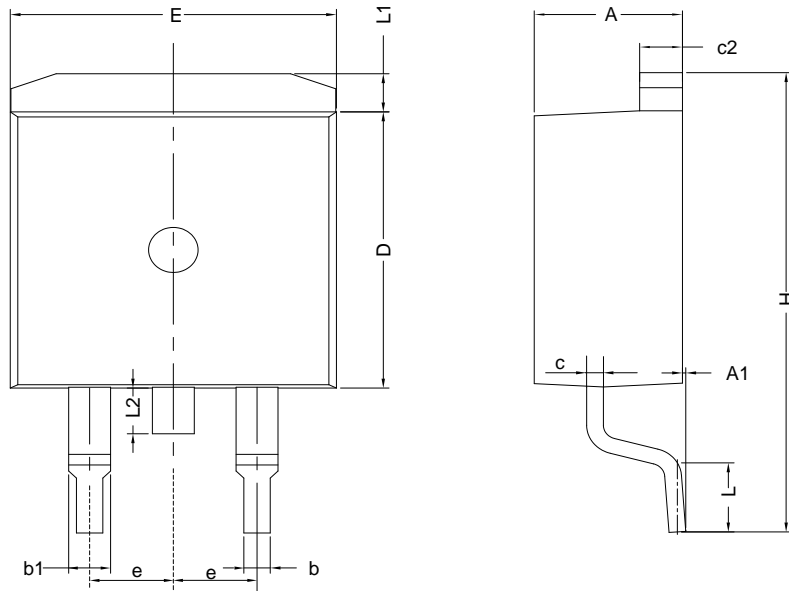
**PACKAGE OUTLINE**



**PACKAGE OUTLINE (CONTINUED)**

**TO-263-2L**

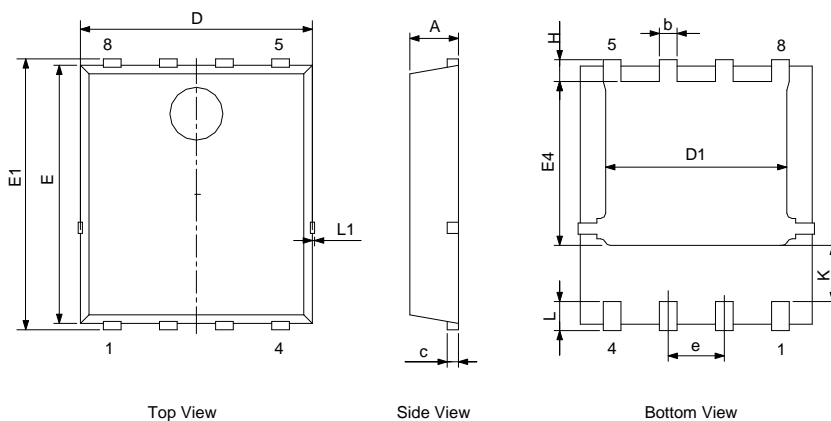
**UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
b1	1.17	—	1.50
c	0.30	—	0.60
c2	1.17	1.27	1.37
D	8.50	—	9.35
E	9.80	—	10.45
e	2.54BSC		
H	14.70	—	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	—	—	1.75

**PDFN-8-5\*6\*0.95-1.27**

**UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.90	—	1.20
b	0.154	0.25	0.354
D	4.80	—	5.40
E	5.66	—	6.06
D1	3.76	—	4.30
E1	5.90	—	6.35
b	0.30	—	0.55
K	1.10	1.30	1.50
e	1.07	1.27	1.37
E4	3.34	—	3.92
L	0.30	0.60	0.71
L1	—	—	0.12
H	0.40	—	0.71





## MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

**Important notice:**

1. Silan reserves the right to make changes of this instruction without notice.
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Rev.: 1.1

Revision History:

1. Add PDFN-8-5x6x0.95-1.27 package
  2. Update typical characteristics
  3. Update important notice
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Rev.: 1.0

Revision History:

1. First release
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