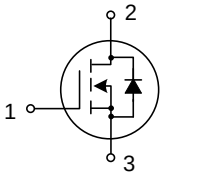
14A, 100V N-CHANNEL MOSFET

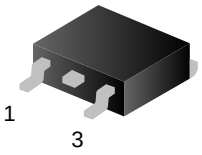
DESCRIPTION

SVT10111ND is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance and withstand high energy pulse in the avalanche and commutation mode.

This device is widely used in UPS, Power Management for Inverter Systems .



1.Gate 2.Drain 3.Source



TO-252-2L

FEATURES

- 14A,100V, $R_{DS(on)(typ.)}$=85mΩ@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

NOMENCLATURE

S V T X X X R X N X

Silan

Low voltage trench MOS products

Nominal voltage, using 2 digits; Example: 04 denotes 40V, 10 denotes 100V

Package information. Example: T:TO-220; D:TO-252; MJ:TO-251J;

Channel polarity: N denotes N channel, P denotes P channel

Resistance: R75 denotes 0.7mΩ; 7R5 denotes 7.5mΩ; 100 denotes 10mΩ; 101 denotes 100mΩ

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVT10111NDTR	TO-252-2L	10111ND	Halogen free	Tape&Reel

ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, T_C=25°C)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current	T_C=25°C	I_D	14	A
	T_C=100°C		9	
Drain Current Pulsed		I_{DM}	56	A
Power Dissipation(T_C=25°C)		P_D	40	W
-Derate above 25°C			0.32	W/°C
Single Pulsed Avalanche Energy(Note 1)	L=1.0mH	E_{AS}	25	mJ
	L=0.5mH		12	mJ
Operation Junction Temperature Range		T_J	-55～+150	°C
Storage Temperature Range		T_{stg}	-55～+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.13	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62	°C/W

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, T_C=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	100	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	1.0	--	3.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=10A	--	85	105	mΩ
		V_{GS}=6V, I_D=10A	--	90	110	mΩ
Gate Resistance	R_G	f=1MHz	--	2.5	--	Ω
Input Capacitance	C_{iss}	f=1MHz,V_{GS}=0V, V_{DS}=25V	--	1107	--	pF
Output Capacitance	C_{oss}		--	50.8	--	
Reverse Transfer Capacitance	C_{rss}		--	38.5	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=50V, V_{GS}=10V, R_G=3Ω, I_D=10A (Note 2,3)	--	3.9	--	ns
Turn-on Rise Time	t_r		--	28.3	--	
Turn-off Delay Time	$t_{d(off)}$		--	30.5	--	
Turn-off Fall Time	t_f		--	16.1	--	
Total Gate Charge	Q_g	V_{DD}=80V, V_{GS}=10V, I_D=10A (Note 2,3)	--	27	--	nC
Gate-Source Charge	Q_{gs}		--	4.4	--	
Gate-Drain Charge	Q_{gd}		--	6.5	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	14	A
Pulsed Source Current	I_{SM}		--	--	56	
Diode Forward Voltage	V_{SD}	I_S=10A,V_{GS}=0V	--	--	1.2	V
Reverse Recovery Time	T_{rr}	I_S=10A,V_{GS}=0V, dIF/dt=100A/μs	--	26.6	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.03	--	μC

Notes:

1.V_{DD}=50V, R_G=10Ω,starting T_J=25°C;

2.Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;

3.Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. Output Characteristics

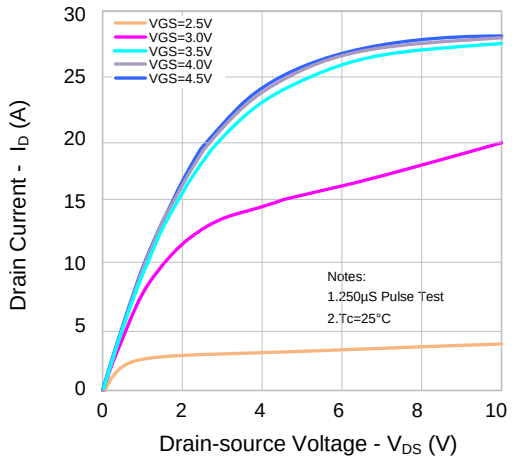


Figure 2. Transfer Characteristics

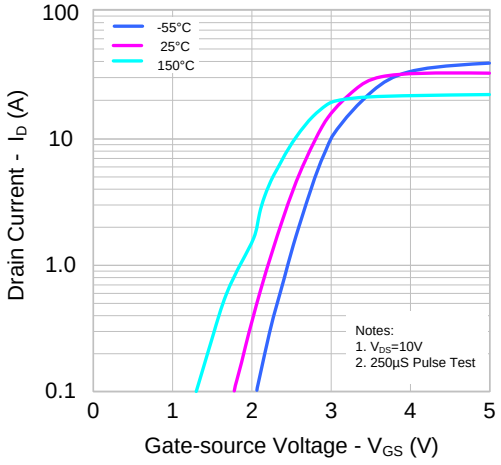


Figure 3. On-resistance vs. Drain Current

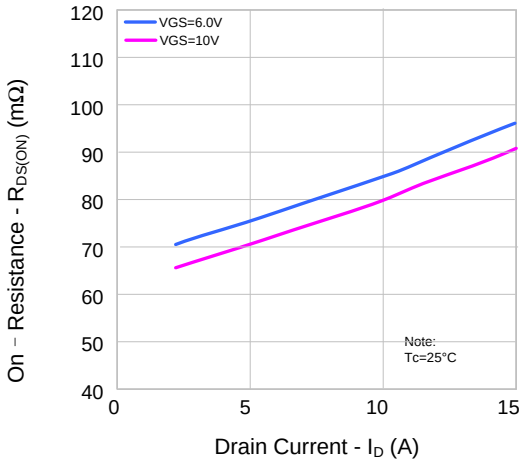


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

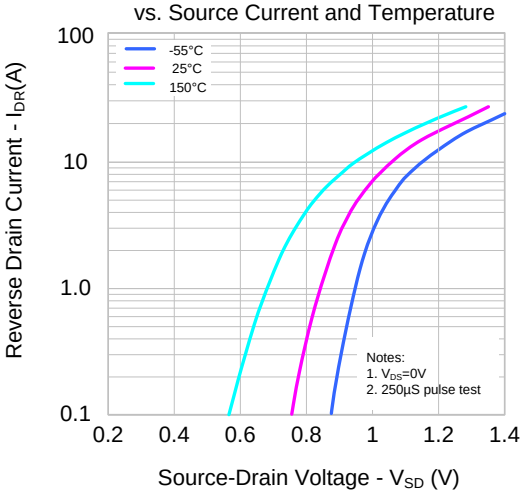


Figure 5. Capacitance Characteristics

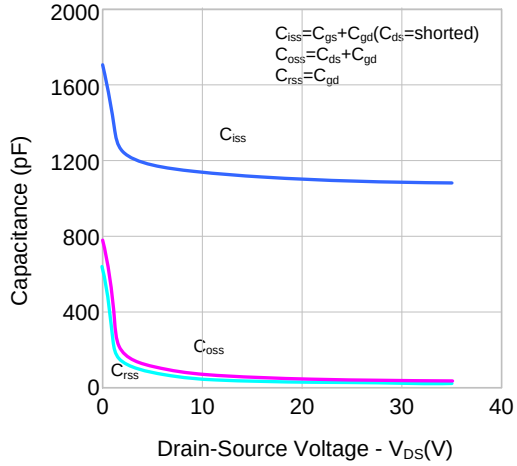
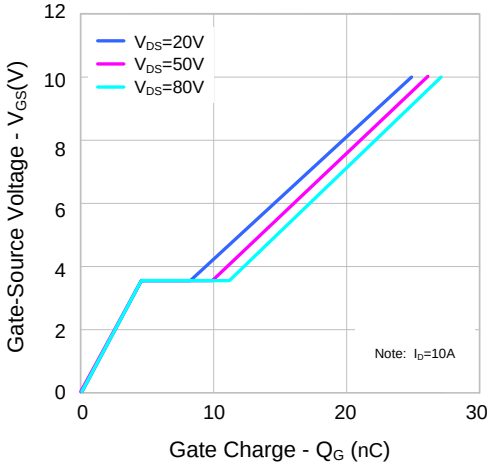


Figure 6. Gate Charge



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage vs. Temperature Characteristics

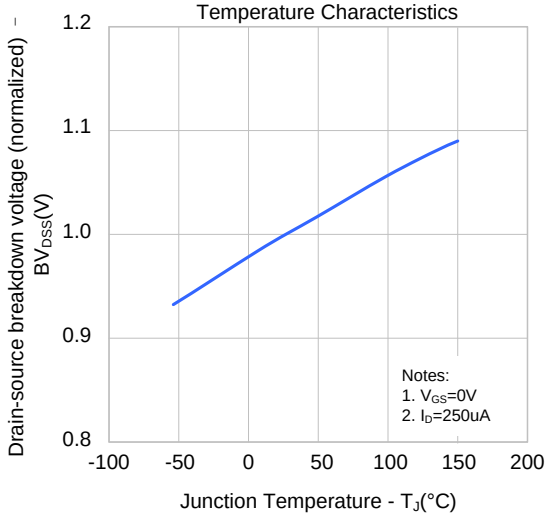


Figure 8. On-resistance vs. Temperature Characteristics

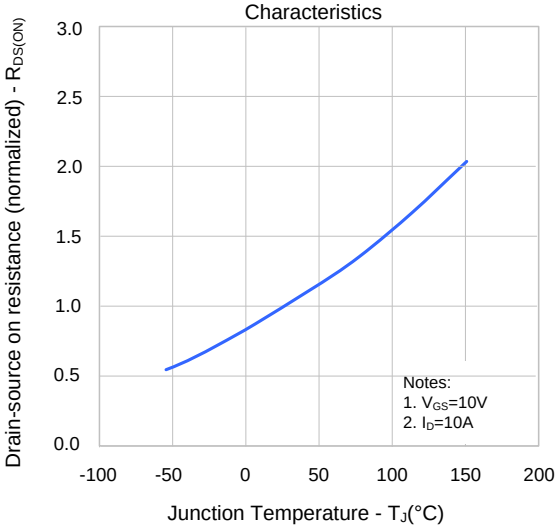


Figure 9. Max. Safe Operating Area

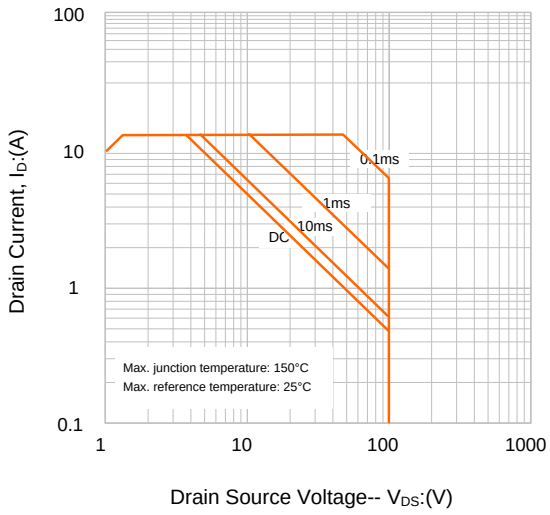
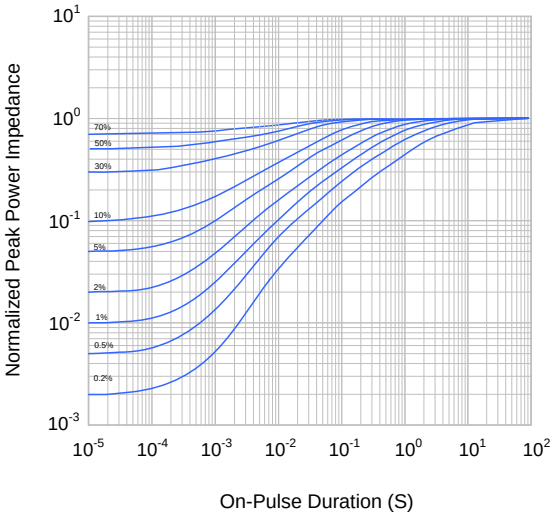
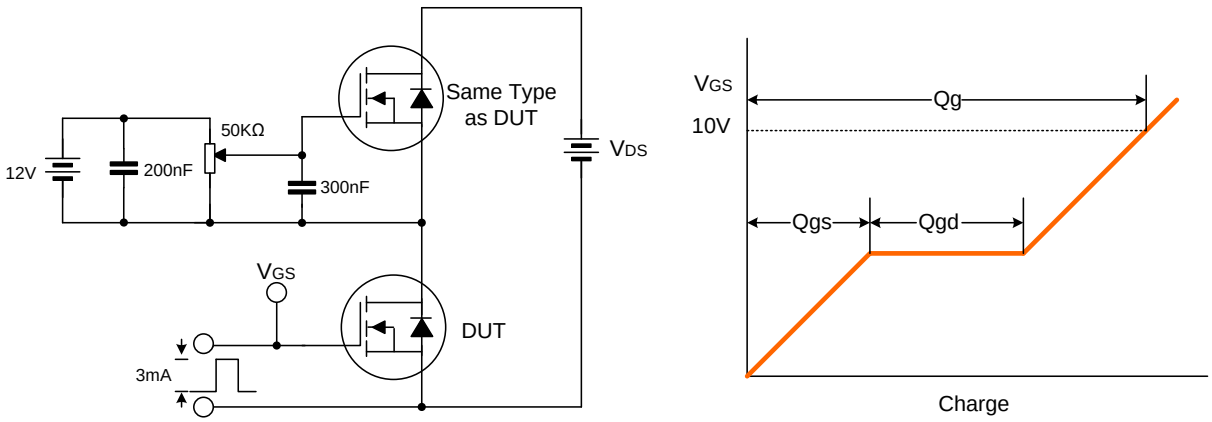


Figure 10. Square Wave Impedance Simulation

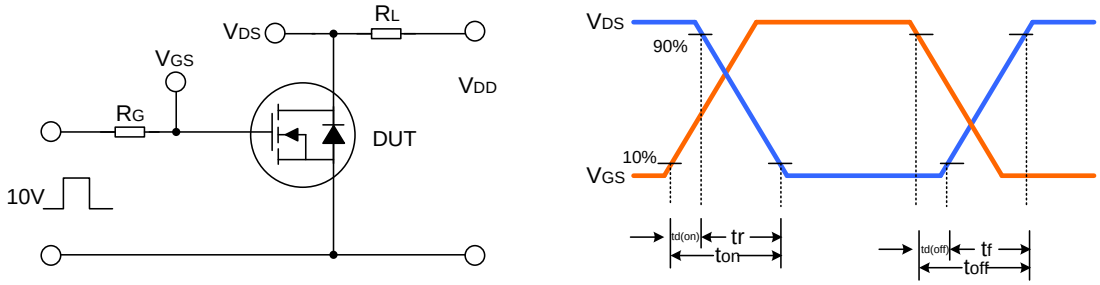


TYPICAL TEST CIRCUIT

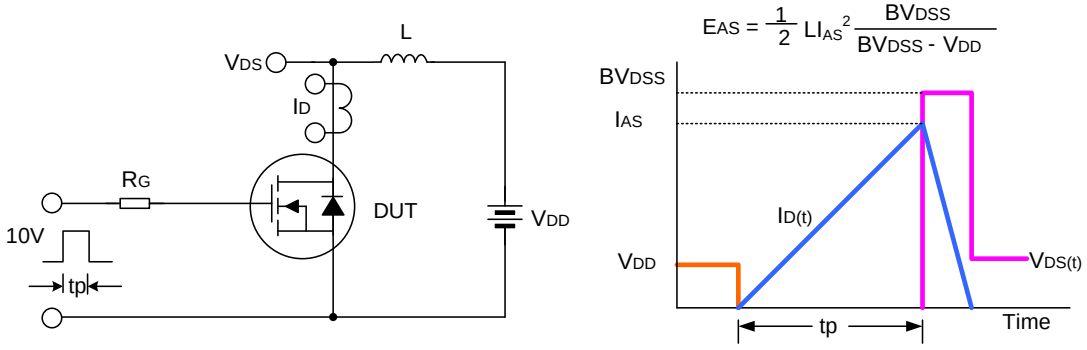
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

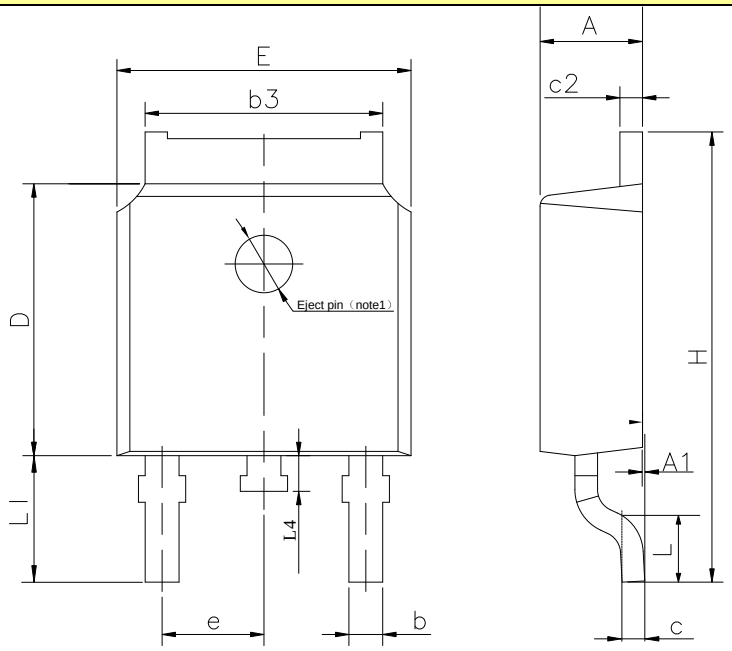


Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-252-2L **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e		2.30TYP	
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1		2.90REF	
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

Part No.:	SVT10111ND	Document Type:	Datasheet
Copyright:	HANGZHOU SILAN MICROELECTRONICS CO.,LTD	Website:	http: //www.silan.com.cn

Rev.: 1.3

Revision History:

1. Add EAS values under L= 0.5mh

Rev.: 1.2

Revision History:

1. Add Test conditions of $R_{DS(on)}$

Rev.: 1.1

Revision History:

1. Modify the packing and Hazardous Substance Control of TO-252-2L

Rev.: 1.0

Revision History:

1. First release