

13A, 60V N-CHANNEL MOSFET

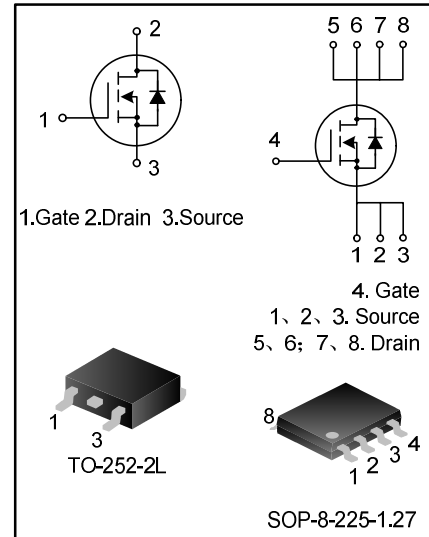
DESCRIPTION

The SVT13N06SA(D) is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance.

This device is widely used in UPS, DC-DC converters, synchronous rectifier and switch.

FEATURES

- ◆ 13A, 60V, $R_{DS(on)(typ.)}=9m\Omega@V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low C_{rss}
- ◆ Fast switching
- ◆ Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVT13N06SA	SOP-8-225-1.27	13N06SA	Halogen free	Tube
SVT13N06SATR	SOP-8-225-1.27	13N06SA	Halogen free	Tape & Reel
SVT13N06DTR	TO-252-2L	13N06D	Halogen free	Tape & Reel

ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, $T_C=25^{\circ}C$)

Characteristics	Symbol	Ratings		Unit
		SVT13N06SA	SVT13N06D	
Drain-Source Voltage	V_{DS}	60		V
Gate-Source Voltage	V_{GS}	± 20		V
Drain Current	$T_C=25^{\circ}C$	13	66	A
	$T_C=100^{\circ}C$	8.2	42	
Drain Current Pulsed(Note 1)	I_{DM}	52	264	A
Power Dissipation($T_C=25^{\circ}C$) -Derate above $25^{\circ}C$	P_D	4.6	97	W
		0.04	0.78	W/ $^{\circ}C$
Single Pulsed Avalanche Energy(Note 2)	E_{AS}	405		mJ
Operation Junction Temperature Range	T_J	$-55 \sim +150$		$^{\circ}C$
Storage Temperature Range	T_{stg}	$-55 \sim +150$		$^{\circ}C$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
Thermal Resistance, Junction-to-Case(Note 3)	$R_{\theta JC}$	27	1.29	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient(Note 3)	$R_{\theta JA}$	85	62	$^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $T_c=25^{\circ}\text{C}$)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.1	--	2.4	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=13A$	--	9	11	$m\Omega$
		$V_{GS}=4.5V, I_D=10A$	--	10.8	13.5	
Input Capacitance	C_{iss}	$f=1MHz, V_{GS}=0V,$ $V_{DS}=25V$	--	3071	--	pF
Output Capacitance	C_{oss}		--	221	--	
Reverse Transfer Capacitance	C_{rss}		--	177	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, V_{GS}=10V,$ $R_G=24\Omega, I_D=13A$ (Note 4,5)	--	18	--	ns
Turn-on Rise Time	t_r		--	80	--	
Turn-off Delay Time	$t_{d(off)}$		--	277	--	
Turn-off Fall Time	t_f		--	143	--	
Total Gate Charge	Q_g	$V_{DD}=48V, I_D=13A, V_{GS}=10V$ (Note 4,5)	--	69	--	nC
Gate-Source Charge	Q_{gs}		--	11	--	
Gate-Drain Charge	Q_{gd}		--	18	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	13	A
Pulsed Source Current	I_{SM}		--	--	52	
Diode Forward Voltage	V_{SD}	$I_S=13A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=13A, V_{GS}=0V,$ $dI/dt=100A/\mu s$	--	23	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.02	--	μC

Notes:

- 1.Drain current is limited by junction temperature;
- 2.L=10mH, $I_{AS}=9.0A$, $V_{DD}=50V$, $R_G=20\Omega$, starting $T_J=25^{\circ}\text{C}$;
- 3.The value of Thermal resistance is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper.
- 4.Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;
- 5.Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. Output Characteristics

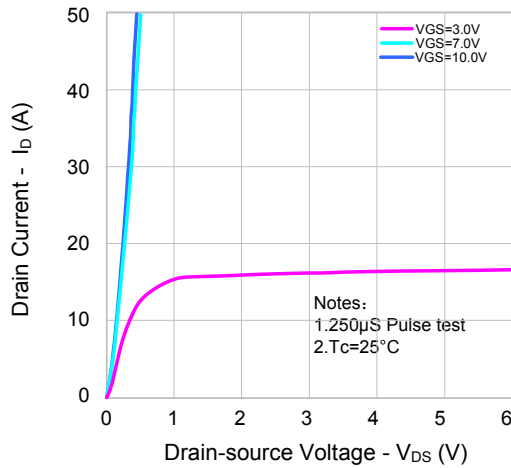


Figure 2. Transfer Characteristics

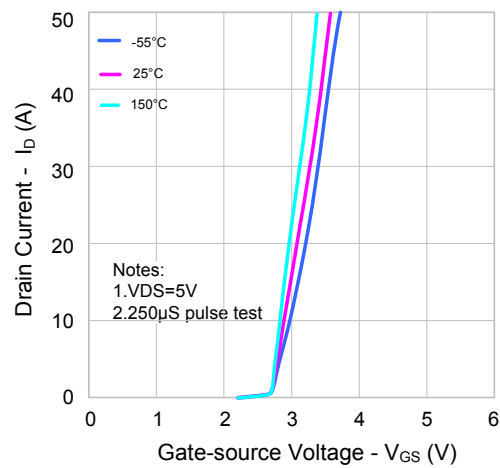


Figure 3. On-resistance vs. Drain Current

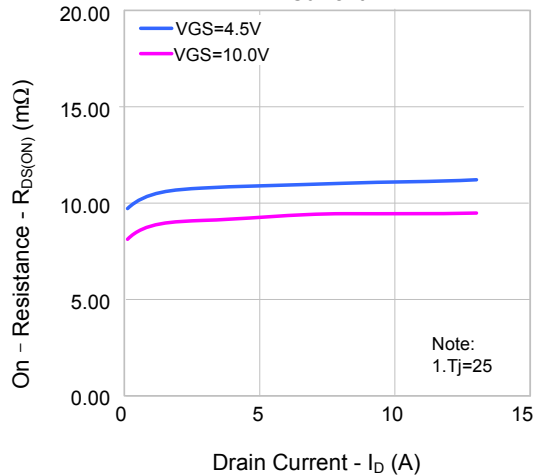


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

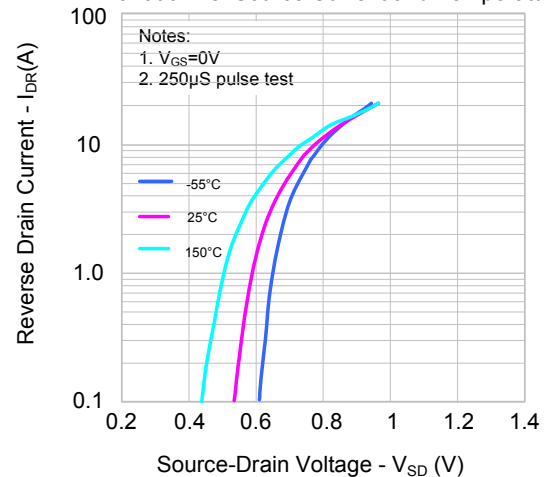


Figure 5. Capacitance Characteristics

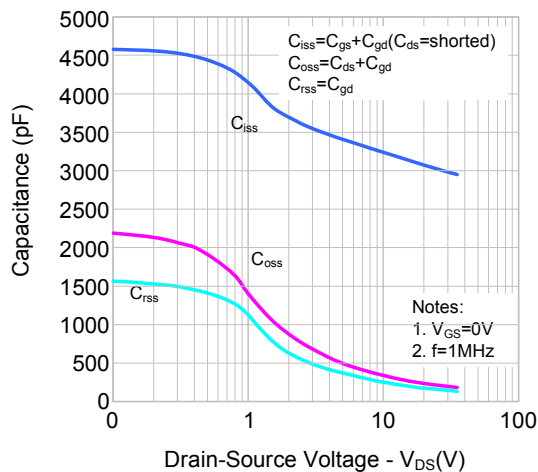
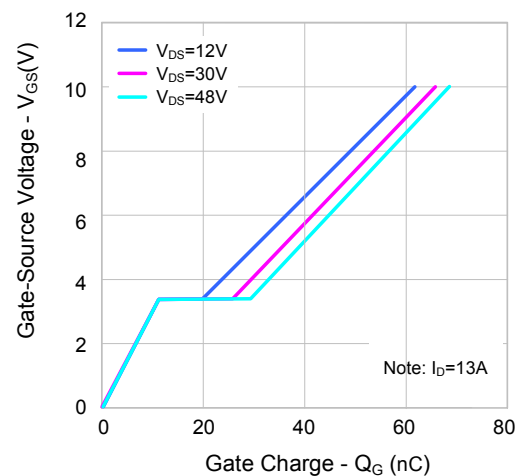
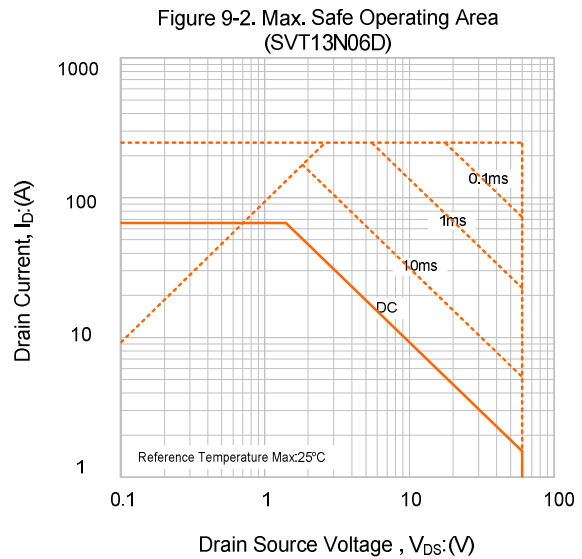
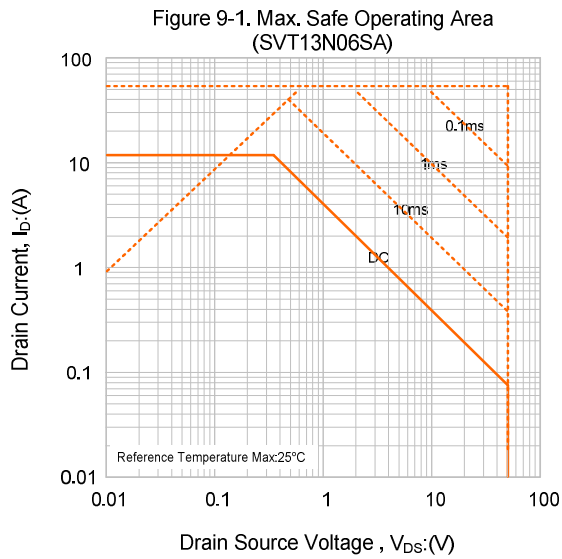
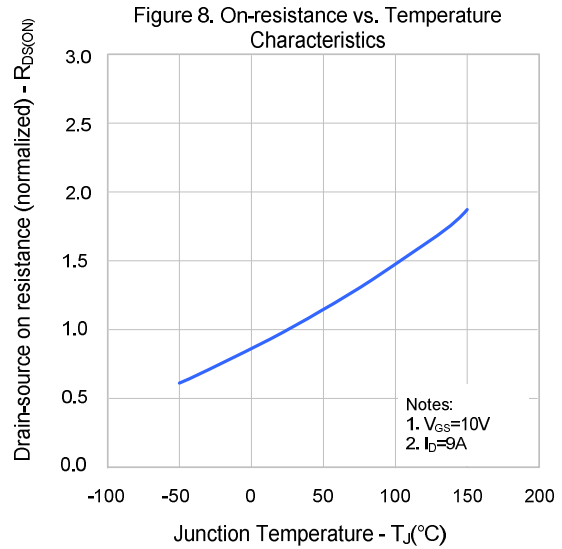
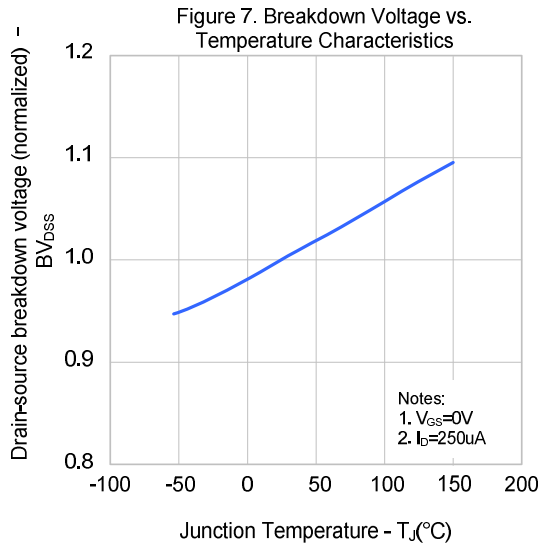


Figure 6. Gate Charge



TYPICAL CHARACTERISTICS(continued)



TYPICAL TEST CIRCUIT

Figure 1: Gate Charge Test Circuit & Waveform

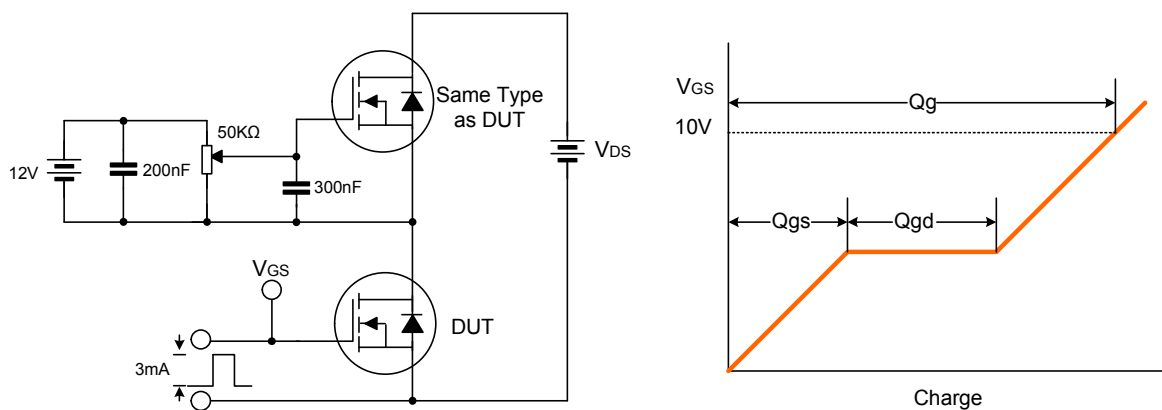


Figure 2: Resistive Switching Test Circuit & Waveform

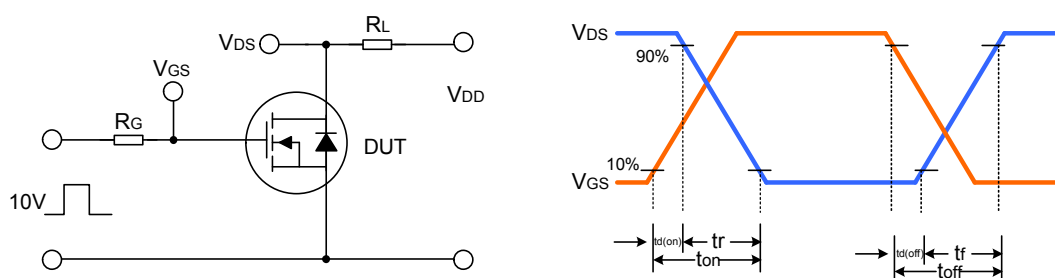
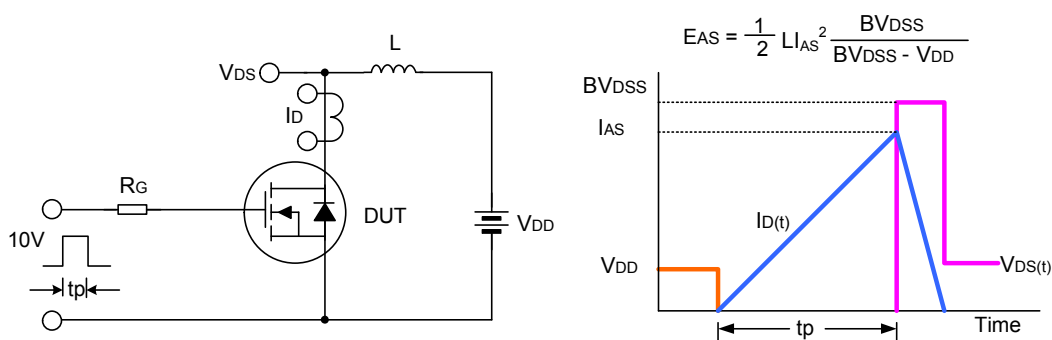


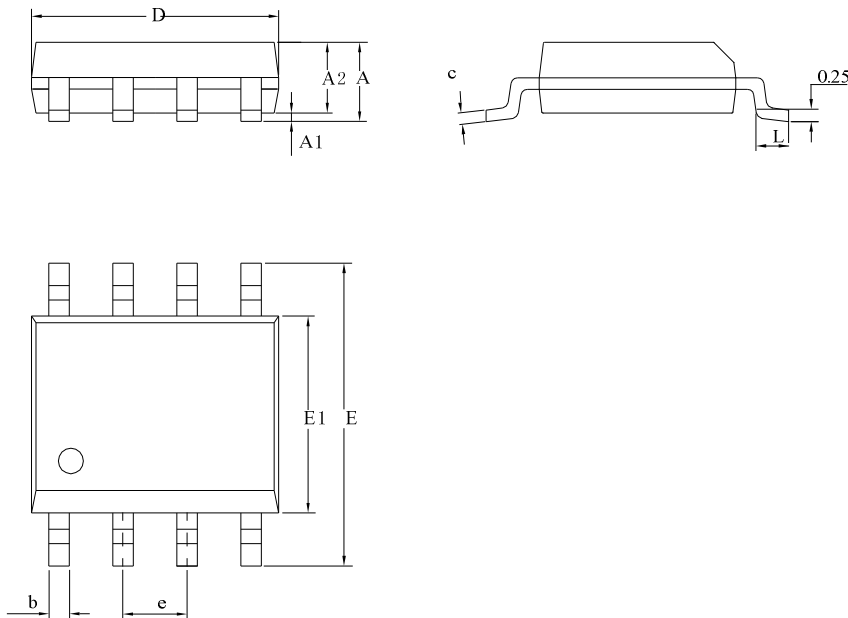
Figure 3: Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

SOP-8-225-1.27

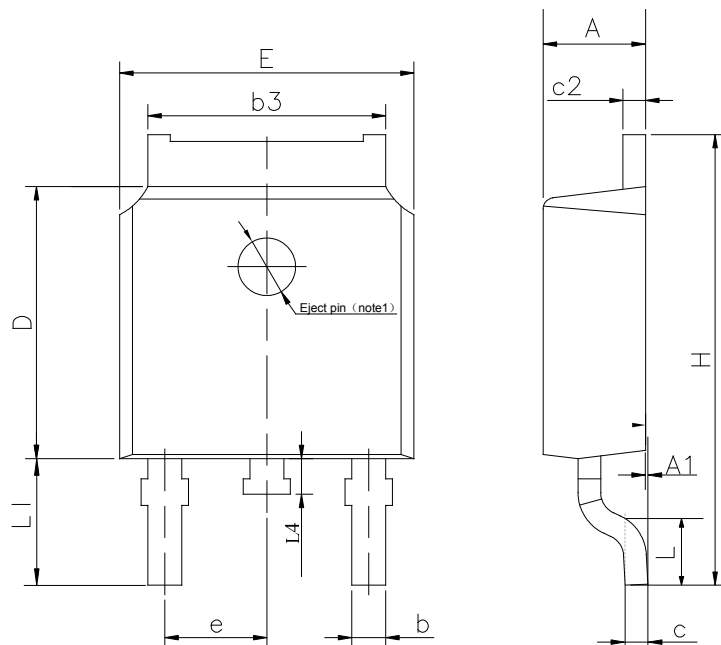
UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.05	0.15	0.25
A2	1.25	--	1.65
b	0.32	0.42	0.52
c	0.15	0.2	0.26
D	4.70	4.90	5.30
E	5.60	6.00	6.40
E1	3.60	3.90	4.20
e	1.27BSC		
L	0.30	—	1.27

TO-252-2L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

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Rev.: 1.5

Revision History:

1. Add TO-252-2L
 2. Update SOA of SVT13N06SA
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Rev.: 1.4

Revision History:

1. Modify the Tye.and Max. of Static Drain- Source On State Resistance
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Rev.: 1.3

Revision History:

1. Modify Electrical characteristics
 2. Update Fig 5 and 6
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Rev.: 1.2

Revision History:

1. Modify Electrical characteristics of VGS(th)
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Rev.: 1.1

Revision History:

1. Modify ordinate of Fig.3
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Rev.: 1.0

Revision History:

1. First Release
-
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