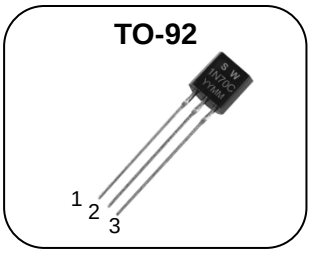
N-channel MOSFET

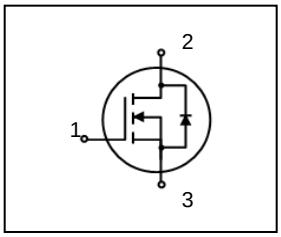
Features

- High ruggedness
- $R_{DS(ON)}$ (Max 16 **Ω**)@V_{GS}=10V
- Gate Charge (Max 6nC)
- Improved dv/dt Capability
- 100% Avalanche Tested



1. Gate 2. Drain 3. Source

BV_{DSS} : 700V
I_D : 0.8A
$R_{DS(ON)}$: 16ohm



General Description

This power MOSFET is produced with advanced VDMOS technology of SAMWIN. This technology enable power MOSFET to have better characteristics, such as fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics. This power MOSFET is usually used at AC adaptors and SMPS.

Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW C 1N70C	SW1N70C	TO-92	TAPE

Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		700	V
I_D	Continuous Drain Current (@T_C=25°C)		0.8	A
	Continuous Drain Current (@T_C=100°C)		0.4	A
I_{DM}	Drain current pulsed	(note 1)	2.4	A
V_{GS}	Gate to Source Voltage		±30	V
E_{AS}	Single pulsed Avalanche Energy	(note 2)	52	mJ
E_{AR}	Repetitive Avalanche Energy	(note 1)	0.3	mJ
dv/dt	Peak diode Recovery dv/dt	(note 3)	4.5	V/ns
P_D	Total power dissipation (@T_C=25°C)		3	W
	Derating Factor above 25°C		0.023	W/°C
T_{STG}, T_J	Operating Junction Temperature & Storage Temperature		-55 ~ + 150	°C
T_L	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.		300	°C

Thermal characteristics

Symbol	Parameter	Value	Unit
R_{thCS}	Thermal resistance, Junction to Lead Max	40	°C/W
R_{thjA}	Thermal resistance, Junction to ambient	120	°C/W

Electrical characteristic (T_C = 25ºC unless otherwise specified

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	700	-	-	V
I_{DSS}	Drain to source leakage current	V_{DS}=700V, V_{GS}=0V	-	-	1	uA
		V_{DS}=560V, T_C=125ºC	-	-	10	uA
I_{GSS}	Gate to source leakage current, forward	V_{GS}=30V, V_{DS}=0V	-	-	100	nA
	Gate to source leakage current, reverse	V_{GS}=-30V, V_{DS}=0V	-	-	-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=50uA	3.0	-	4.5	V
$R_{DS(ON)}$	Drain to source on state resistance	V_{GS}=10V, I_D = 0.4A		15	16	Ω
Dynamic characteristics						
C_{iss}	Input capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	70	100	pF
C_{oss}	Output capacitance		-	20	30	
C_{rss}	Reverse transfer capacitance		-	4	6	
$t_{d(on)}$	Turn on delay time	V_{DS}=350V, I_D=0.8A, R_G=25Ω	-	15	35	ns
tr	Rising time		-	75	140	
$t_{d(off)}$	Turn off delay time		-	30	60	
t_f	Fall time		-	35	60	
Q_g	Total gate charge	V_{DS}=560V, V_{GS}=10V, I_D=0.8A	-	7	10	nC
Q_{gs}	Gate-source charge		-	1.3	-	
Q_{gd}	Gate-drain charge		-	2.4	-	

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET	-	-	0.8	A
I_{SM}	Pulsed source current		-	-	2.4	A
V_{SD}	Diode forward voltage drop.	I_S=0.8A, V_{GS}=0V	-	-	1.5	V
T_{rr}	Reverse recovery time	I_S=0.8A, V_{GS}=0V, dI_F/dt=100A/us	-	150	-	ns
Q_{rr}	Breakdown voltage temperature		-	0.44	-	uC

※. Notes

1. Repeatitive rating : pulse width limited by junction temperature.
2. L = 95mH, I_{AS} = 0.8A, V_{DD} = 50V, R_G=25Ω, Starting T_J = 25ºC
3. I_{SD} ≤ 0.8A, di/dt = 300A/us, V_{DD} ≤ BV_{DSS}, Staring T_J =25ºC
4. Pulse Test : Pulse Width ≤ 300us, duty cycle ≤ 2%
5. Essentially independent of operating temperature.

Fig. 1. On-state characteristics

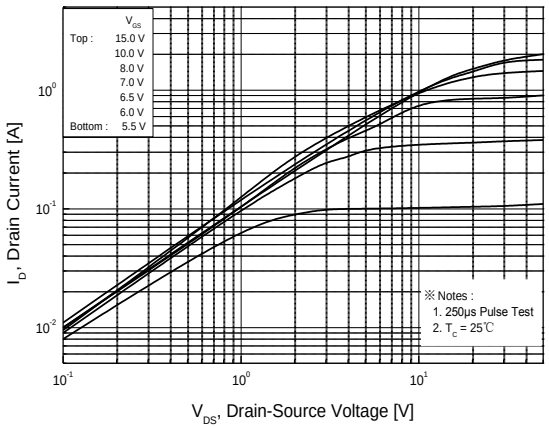


Fig. 2. Transfer characteristics

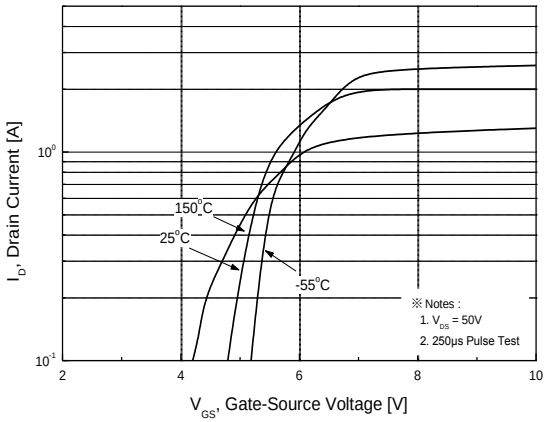


Fig. 3. On-resistance variation vs. drain current and gate voltage

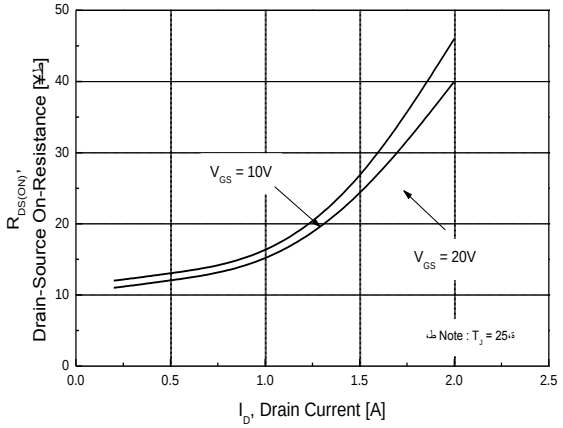


Fig. 4. On state current vs. diode forward voltage

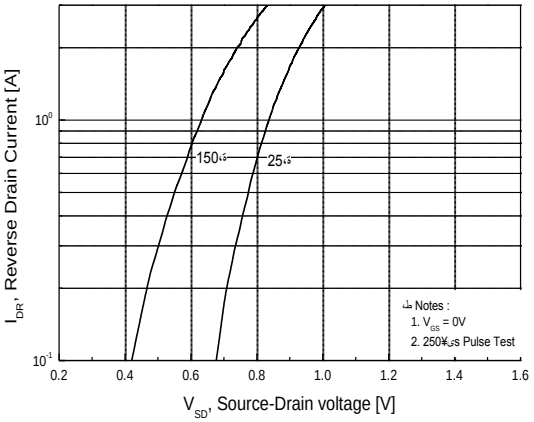


Fig. 5. Capacitance characteristics (Non-Repetitive)

Fig. 6. Gate charge characteristics

Fig 7. Breakdown Voltage Variation vs. Junction Temperature

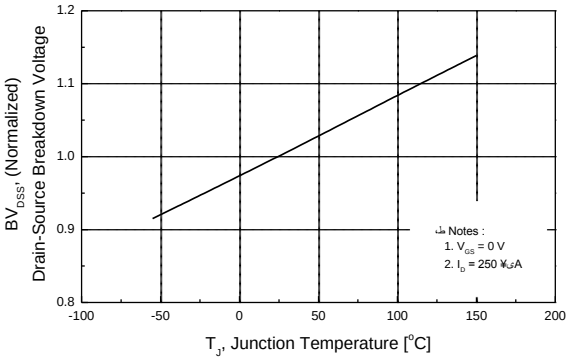


Fig. 8. On resistance variation vs. junction temperature

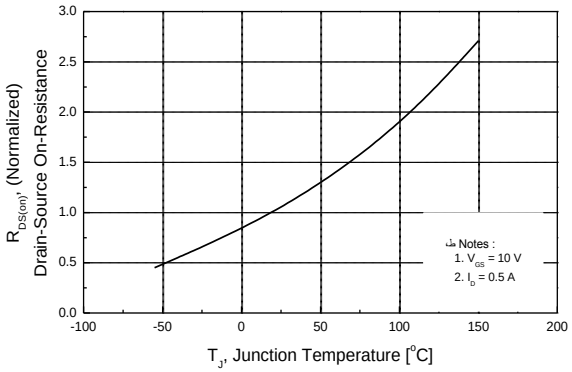


Fig. 9. Maximum drain current vs. case temperature.

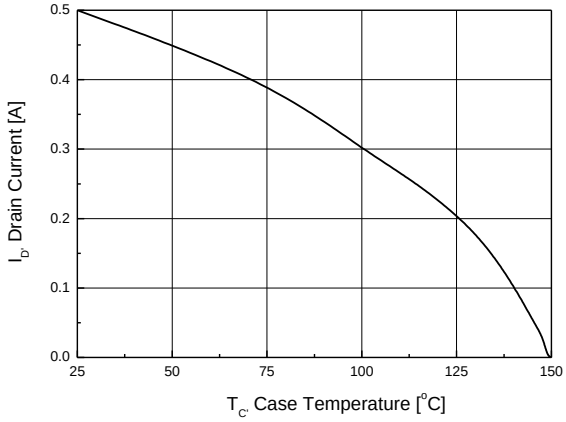


Fig. 10. Maximum safe operating area

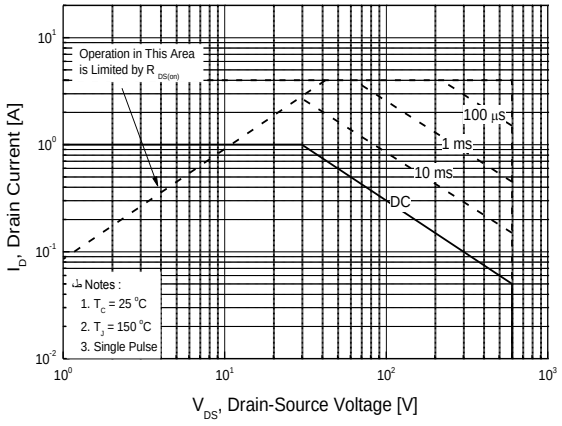


Fig. 11. Transient thermal response curve

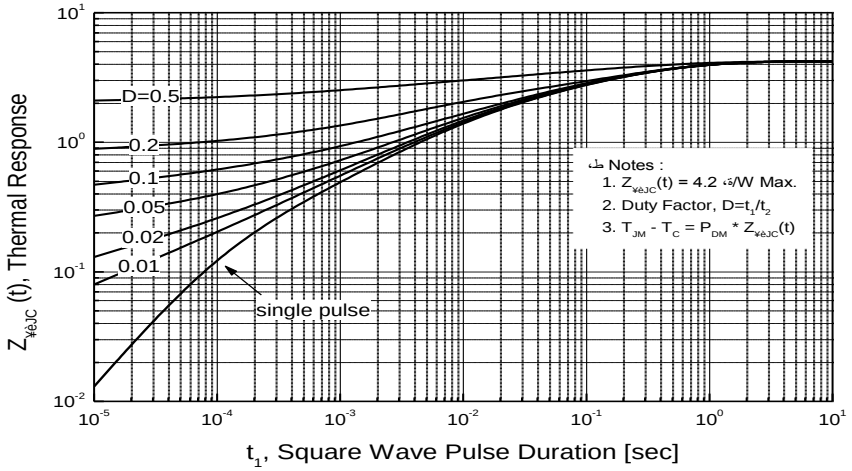


Fig. 12. Gate charge test circuit & waveform

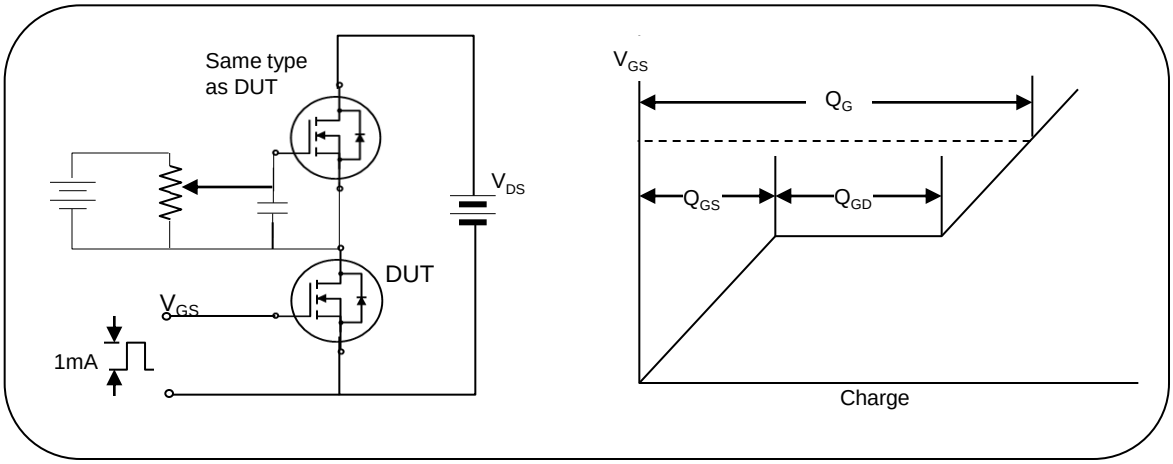


Fig. 13. Switching time test circuit & waveform

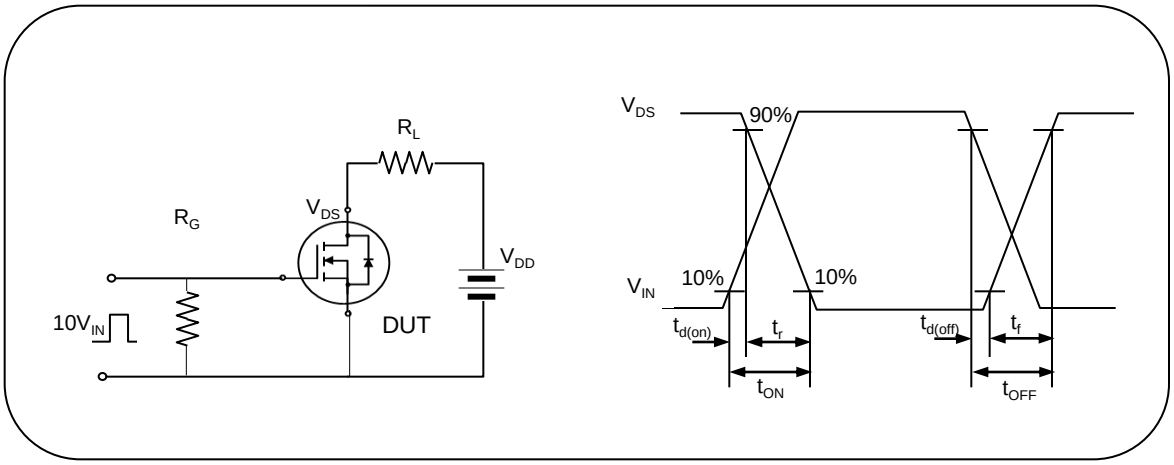


Fig. 14. Unclamped Inductive switching test circuit & waveform

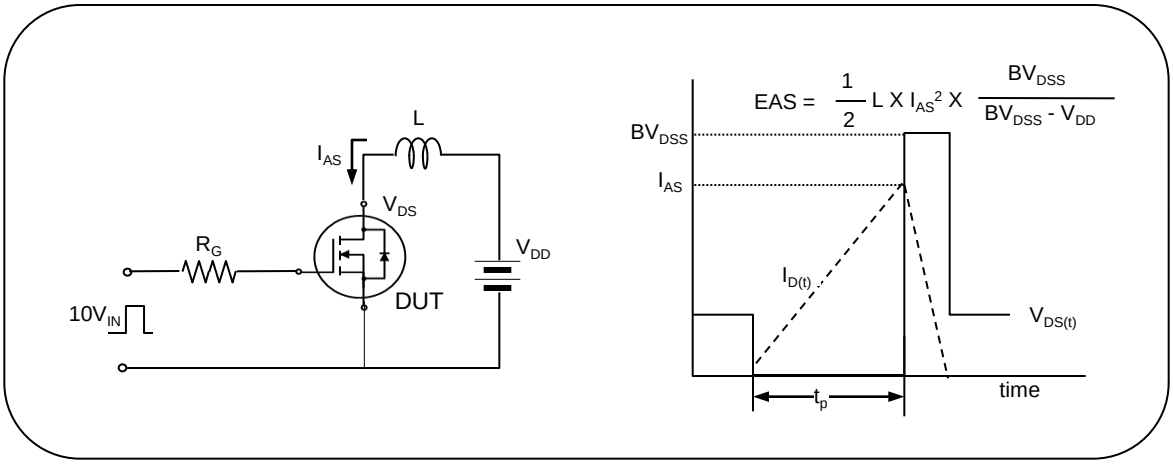
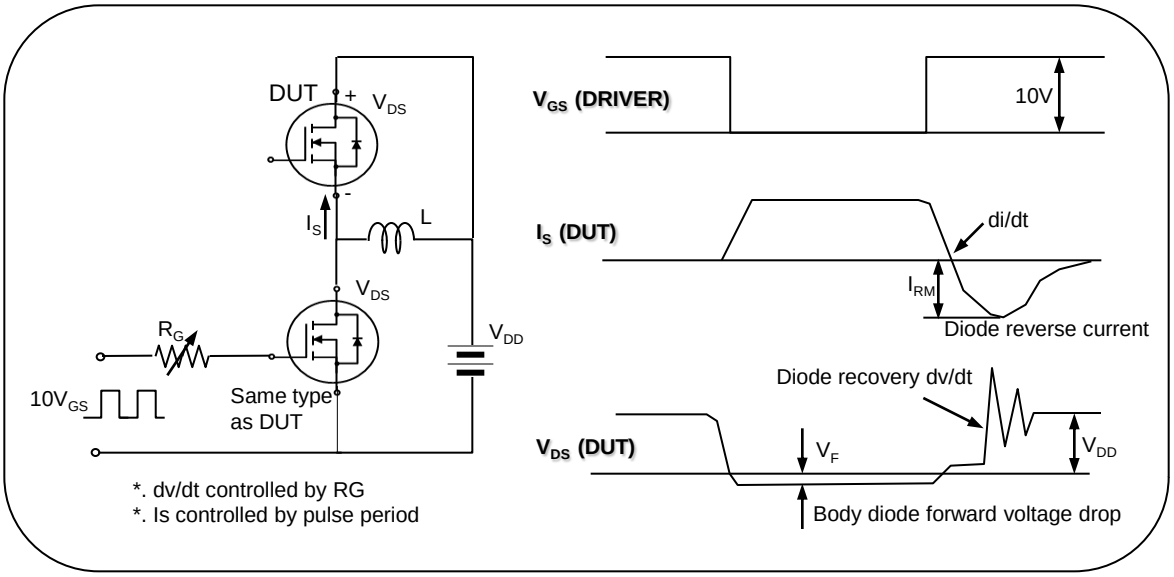


Fig. 15. Peak diode recovery dv/dt test circuit & waveform



REVISION HISTORY

Revision No.	Changed Characteristics	Responsible	Date	Issuer
REV 1.0	Origination, First Release	Alice Nie	2007.12.05	XZQ
REV 2.0	Updated the format of datasheet and added Order Codes.	Alice Nie	2011.03.24	XZQ

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