SW2303 USB PD And QC Protocols Controller

1. General Description

The SW2303 is a highly integrated Type-C/Type-A port fast charging protocol controller. It supports BC1.2/PD3.0+PPS/QC4+/AFC/FCP/SCP/SFCP/PE charging protocols. It integrates an optocoupler driver and a FB feedback output for CC and CV loop control. With ACDC or DCDC and a few external components, the SW2303 provides a complete high-performance Type-C port/Type-A port fast charging solution.

2. Applications

- Car charger
- Adapter
- Power strip

3. Features

- **Power Management**
  - Wide input voltage range 3.0~25V
  - Optocoupler drive and FB output
  - CC/CV Mode
  - VIN and VBUS fast discharge
  - Cable voltage drop compensation

- **Fast Charge Protocol**
  - Support QC5/QC4.0+/QC3.0/QC2.0
    QC5
    Report Number:QC20210413228
    QC4+
    Report Number:QC20201216209
  - Support PD3.0 with PPS
    PD TID:4847
  - Support AFC
  - Support FCP and SCP
  - Support SFCP
  - Support PE1.1 and PE2.0

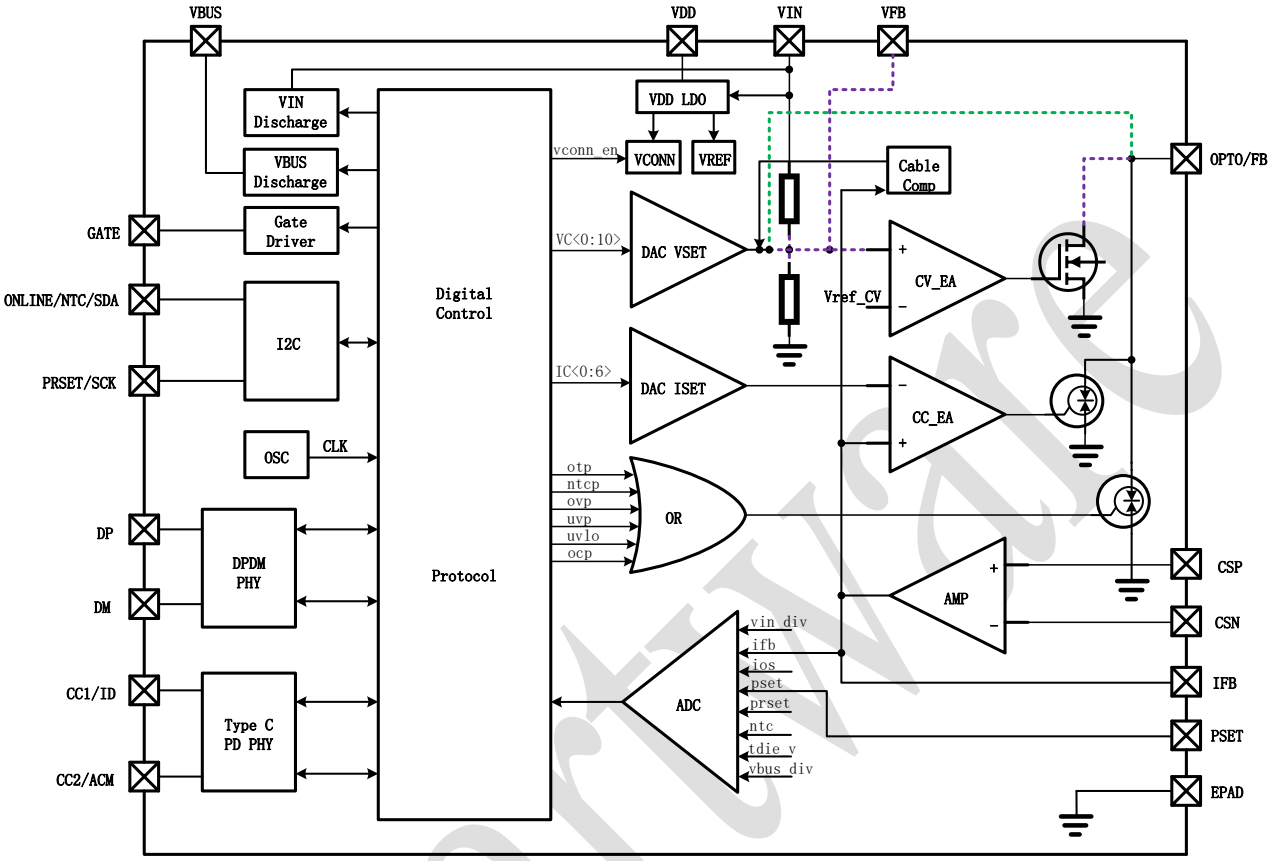
- **Type-C Interface**
  - Support USB Type-C Specification
  - Support DFP Role
  - Support VCONN
  - CC/CC2/DP/DM Pin BV > 25V

- **BC1.2 Module**
  - Support BC1.2 DCP
  - Support Apple & Samsung Device
- **System Control**
  - External blocking PMOS/NMOS
  - I2C interface
  - Flexible configuration of power and voltage profile
  - Dynamic power allocation

- **Protection**
  - Softstart
  - Output over voltage protection
  - Output under voltage protection
  - Output over current protection
  - Input under voltage protection
  - NTC over temperature protection
  - Over temperature protection
  - DPDM and CC/CC2 over voltage protection

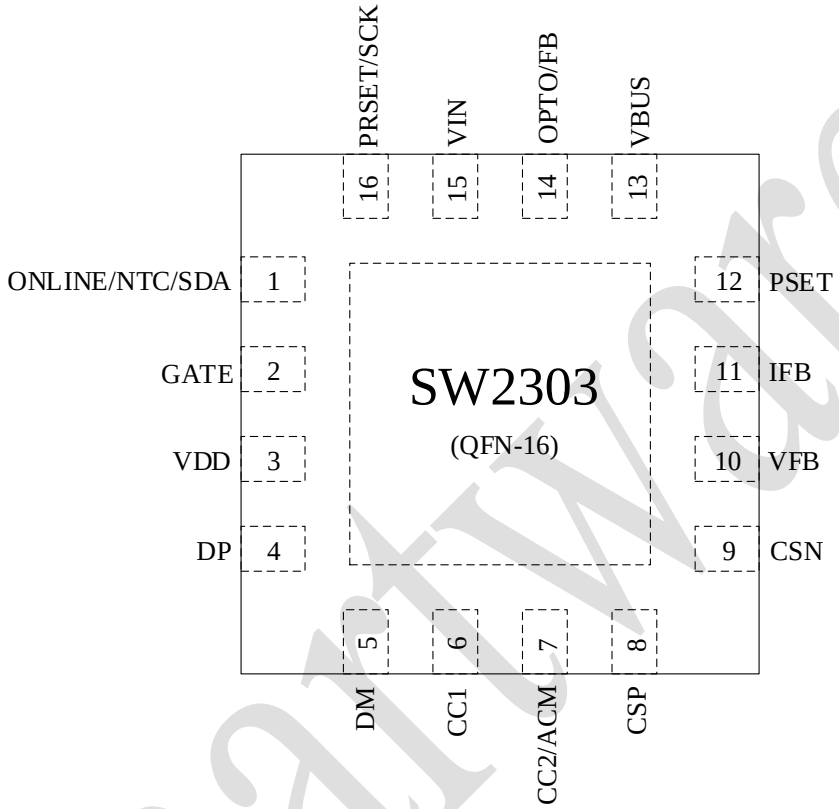
- **QFN-16(4x4mm)Package**
- **>±4KV ESD HBM**

4. Block Diagram



5. Pin Configuration and Function

5.1. Pin Configuration



5.2. Pin Descriptions

Pin	Name	Function Description
1	ONLINE/NTC/SDA	Online detect, NTC detect, I2C SDA pin.
2	GATE	Power path control pin, supporting NMOS and PMOS.
3	VDD	Internal power.
4	DP	USB port DP pin.
5	DM	USB port DM pin.
6	CC1	Type-C port CC1 pin.
7	CC2/ACM	Type-C port CC2, or Port A and port C mode detect pin.
8	CSP	Current sense positive pin.
9	CSN	Current sense negative pin.
10	VFB	Voltage loop feedback pin.
11	IFB	Current loop feedback pin.
12	PSET	Power set pin.

13	VBUS	VBUS detect and discharge pin.
14	OPTO/FB	OPTP driver, or FB output pin
15	VIN	Input power
16	PRSET/SCK	Power reduction set, or I2C SCK pin.
EPAD	GND	Power ground

6. Absolute Maximum Ratings

Parameters	Symbol	MIN	MAX	UNIT
Input Voltage	VIN	-0.3	44	V
Output Voltage	VBUS	-0.3	44	V
Power Path Control	GATE	-0.3	44	V
OPTO Driver	OPTO	-0.3	40	V
Internal Power	VDD	-0.3	5.5	V
Communication Pins	CC1/CC2/DP/DM	-0.3	40	V
Other Pins	/	-0.3	6	V
Junction Temperature		-40	+150	°C
Storage Temperature Range		-60	+150	°C
ESD（HBM）		-4	+4	KV

【Notice】Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7. Recommended Operating Conditions

Parameters	Symbol	MIN	Typical	MAX	UNIT
Input Voltage	VIN	3.0		25	V

8. Electrical Characteristics

(T_A = 25°C, unless otherwise specified.)

Parameters	Symbol	Test Conditions	MIN	TYP	MAX	UNIT
Power Supply						
VIN Input Voltage	V_{IN}		3.0		30	V
VIN Input UVLO Threshold	V_{IN_UVLO}	VIN Voltage Falling	2.70	2.75	2.80	V
VIN Input UVLO Hysteresis	$V_{IN\_UVLO\_HYS}$	VIN Voltage Rising	0.20	0.25	0.30	V

VDD Output Voltage	V_{DD}	V_{IN}=5V	4.90	4.95	5.0	V
VDD Output Current	I_{DD}	V_{IN}=5V	70	80	90	mA
Quiescent Current	I_Q	V_{IN}=5V, I_{OUT}=0mA	0.5	0.6	0.8	mA
Type-C Interface						
CC Pins Output Current	I_{CC_SOURCE}	Power Level=1.5A	170	180	190	uA
	I_{CC_SOURCE}	Power Level=3.0A	315	330	345	uA
BMC Bit Rate	$f_{BitRate}$		270	300	330	Kbps
BMC Level	V_{Swing}		1.050	1.125	1.200	V
TX Output impedance	Z_{Driver}		30	54	70	Ω
BC1.2 DCP						
Apple 2.4A mode	V_{DP}/V_{DM}	Apple 2.4A Voltage	2.65	2.7	2.75	V
	R_{DP}/R_{DM}	Apple 2.4A impedance	27	30	33	kΩ
Samsung 2A mode	V_{DP}/V_{DM}	Samsung 2A Voltage	1.15	1.2	1.25	V
	R_{DP}/R_{DM}	Samsung 2A impedance	90	100	110	kΩ
HVDCP						
DATA Detect Voltage Reference	V_{DATA_REF}		0.3	0.325	0.35	V
DP High Glitch Filter Time	$T_{GLITCH\_DP\_H}$		1000	1250	1500	ms
DM Low Glitch Filter Time	$T_{GLITCH\_DM\_L}$		1.5	2	2.5	ms
Output Voltage Glitch Filter Time	T_{GLITCH_CHANGE}		20	40	60	ms
Glitch Filter Time For Continuous Change	$T_{GLITCH\_CONT\_CHANGE}$		100	150	200	us
DP Pulldown Resistance	R_{DAT_LKG}	VDP=0.6V	300	900	1500	kΩ
DM Pulldown Resistance	R_{DM_DOWN}	VDM=0.6V	18	20	22	kΩ
OVP Protections						
VBUS OVP Threshold	$Vbus_{OVP}$	Respect to Target	+1.8	+2	+2.2	V
VBUS UVP Threshold	$Vbus_{UVP}$	Respect to Target	-1.8	-2	-2.2	V
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SHDT}	Temperature Rising	120	130	140	℃
Thermal Shutdown Hysteresis	T_{SHDT_HYS}	Temperature Falling	45	50	55	℃

9. Functional Description

9.1. Power System

VIN is the power supply input pin of SW2303. It is connected to the output of AC-DC or DC-DC to supply power to SW2303 and the sink device, and its integrated a discharge path is used for quick discharge under specific conditions.

VDD is the 5.0V output voltage by the internal LDO, which is mainly used for the power supply of the circuit inside the SW2303.

9.2. Feedback Mode

When the VFB pin is connected to the compensation network to the OPTO/FB pin, it configures to optocoupler feedback mode, and the OPTO/FB pin is used to drive the optocoupler diode.

When the VFB pin is connected to ground , it configures to FB feedback mode. The OPTO/FB pin is connected to the AC-DC or DC-DC resistor feedback node.

9.3. Loop Control

In optocoupler feedback mode, SW2303 internally integrates a constant voltage control loop (CV) and a constant current control loop (CC). The output of the two loops is connected to the OPTO/FB pin and used to drive the optocoupler, similar to the function of TL431.

The CV loop compensation is achieved through the compensation circuit between the VFB pin and the OPTO/FB pin, and the CC loop compensation is achieved through the compensation circuit between the IFB pin and the OPTO/FB pin. In actual applications, device parameters can be adjusted to improve loop stability and response speed.

9.4. Interface Mode

The SW2303 supports Type-C and Type-A interfaces. If the CC2/ACM pin is connected to VDD, it is configured as Type-A port; otherwise, it is configured as Type-C port.

9.5. Type C Interface

The SW2303 integrates a Type-C logic controller and supports DFP/Source role. When UFP is attached,

the Type-C port will automatically turn on to supply device. When UFP is detached, the Type-C port will automatically turn off.

When Sink is attached ,the Type-C port will turn on and the SW2303 will broadcast power level of 3A.

9.6. Power Path Control

The SW2303 internal integrates a power path control circuit, supporting NMOS and PMOS. The SW2303 will automatically detect the type of external MOS and then switch to the corresponding drive mode.

9.7. BC1.2 Module

The SW2303 integrates a BC1.2 controller, and automatically detects apple and samsung devices:

Apple 2.4A mode: DP=2.7V, DM=2.7V;

Samsung 2A mode: DP=1.2V, DM=1.2V;

9.8. PD Fast Charge

The SW2303 integrates PPS/PD3.0/PD2.0 fast charging protocols, and supports up to 5 FPDOs and 4 APDOs, with 5V/9V/12V/15V/20V, 3.3~5.9V/3.3~11V/3.3 ~16V/3.3~21V respectively. The maximum output current is 5A.

9.9. QC Fast Charge

The SW2303 integrates QC4.0/QC3.0/QC2.0 fast charge protocols. It supports Class A/Class B, while QC2.0 supports 5V/9V/12V/20V output voltage and QC3.0 supports 3.6V~20V output voltage, 200mV/Step.

QC2.0/QC3.0 will output voltage base on DP/DM voltage:

Device		SW2303	
DP	DM	VOUT	Note
3.3V	3.3V	20V	
0.6V	0.6V	12V	

3.3V	0.6V	9V	
0.6V	3.3V	continuous mode	200mV/Step
0.6V	GND	5V	

9.10. AFC Fast Charge

The SW2303 integrates AFC fast charge protocol, and supports 5V/9V/12V output voltage.

9.11. FCP Fast Charge

The SW2303 integrates FCP fast charge protocol, and supports 5V/9V/12V output voltage.

9.12. SCP Fast Charge

The SW2303 integrates SCP fast charge protocol, and supports 5V@4.5A/4.5V@5A or 10V@2A.

9.13. PE Fast Charge

The SW2303 integrates PE 1.1 and PE2.0 fast charge protocols. PE1.1 supports 5V/7V/9V/12V output voltage, PE2.0 supports 5V~20V output voltage with 500mV/Step

9.14. SFCP Fast Charge

The SW2303 integrates SFCP fast charge protocol, and supports 5V/9V/12V output voltage.

9.15. ADC

The SW2303 integrates a 12-bit ADC, which can sample VIN, VBUS, output current and NTC. The resistance of the current-sense resistor can be configured as 5mΩ/10mΩ. It is recommended to use an alloy resistor with 1% accuracy and 1206 package. In order to filter out ripple interference, it is recommended to use an RC filter network composed of 510Ω and 1μF. The filtered signal is connected to the CSP and CSN pins in a differential form. The sampling range and accuracy of each

ADC channel are as follows:

ADC Channel	Range	Step
VIN	0~30.72V	7.5mV
VBUS	0~30.72V	7.5mV
Iout	0~8.533A@10 mΩ 0~12.8A@5 mΩ	25/12mA@10 mΩ 25/8mA@5 mΩ
NTC Voltage	0~2.048V	0.5mV

9.16. Power configuration and dynamic allocation

The SW2303 supports output power configuration for all applications and dynamic power allocation for two chip application, through three pins: PRSET/SCK, PSET, ONLINE/NTC/SDA, as shown in the following table:

PRSET/SCK	PSET	ONLINE/NTC/SDA	dynamic power allocation
SCK pull-up resistor	X	SDA	I2C
GND	Resistor set total power	NTC	Not Support
Resistor set total power	GND	ONLINE	No power reduction
Resistor set reduced power	Resistor set total power	ONLINE	Support

The corresponding relationship between resistance and power is shown in the following table:

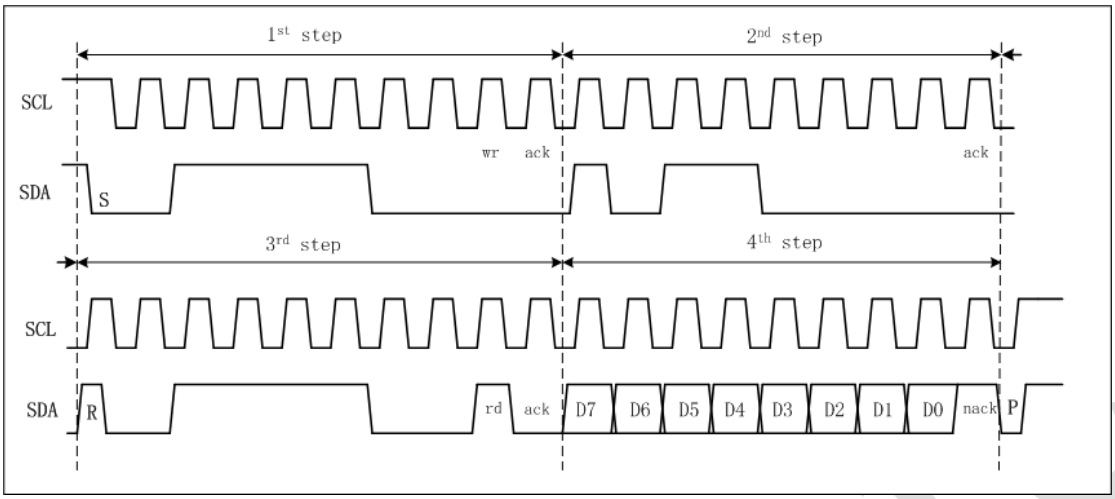
Configure power	Resistance（1%）
100W	Floating
65W	36.5k Ω
60W	27k Ω
45W	19.6k Ω
30W	13k Ω
25W	7.5k Ω
18W	3k Ω

9.17. I2C Interface

The SW2303 integrates a I2C interface, and supports 100K/400K rate.

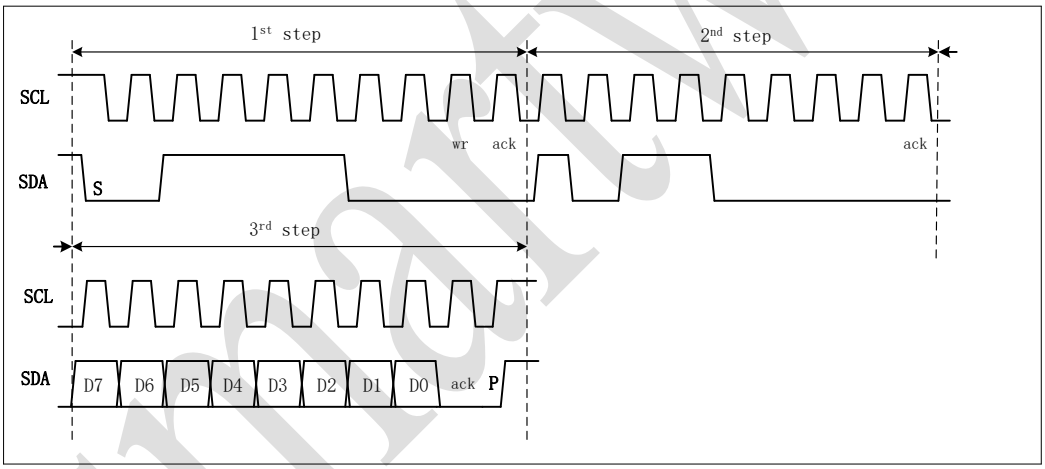
Read Timing:

Slave address ： 0x3C
Register address： 0xB0

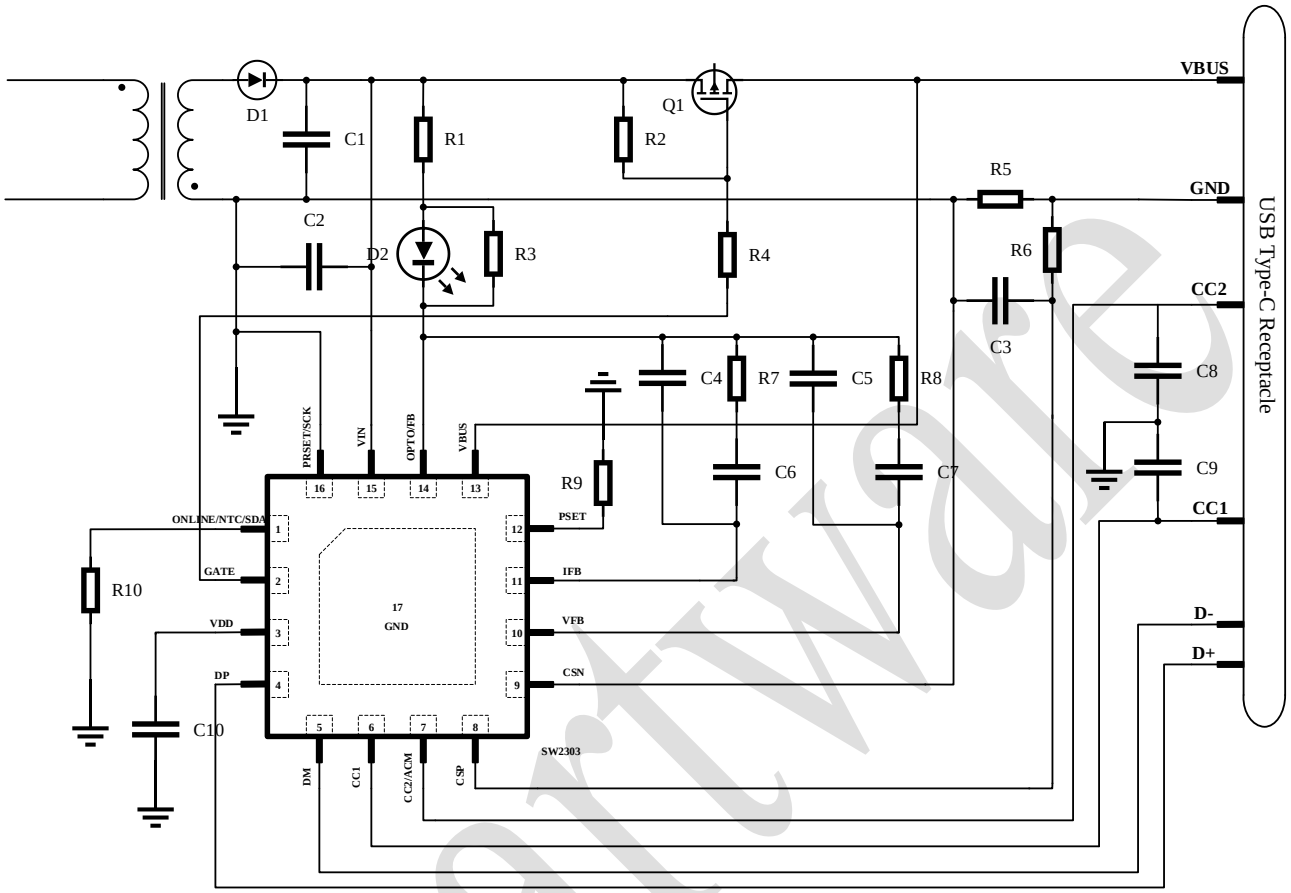


Write Timing:

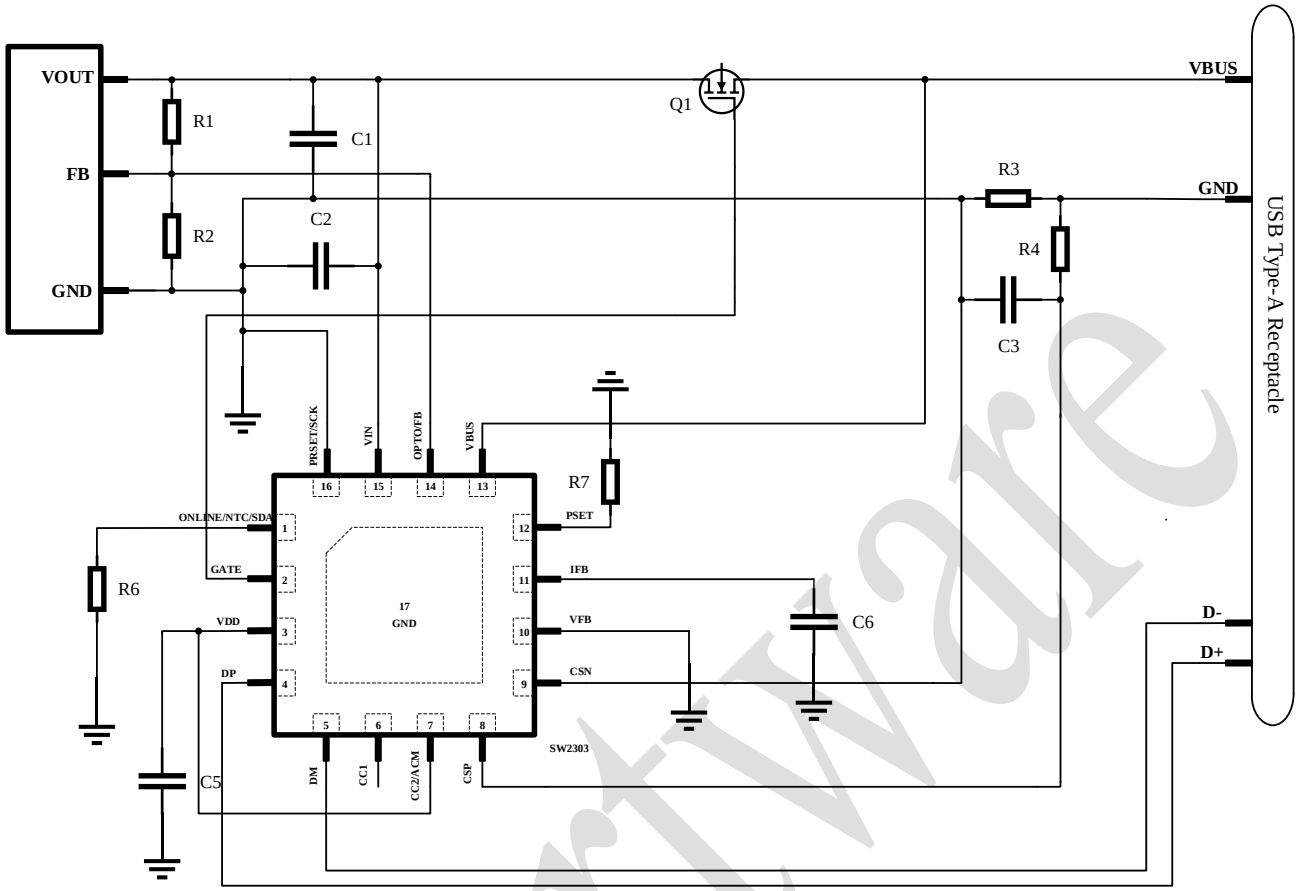
Slave address ： 0x3C
Register address： 0xB0



10. Typical Application Circuit



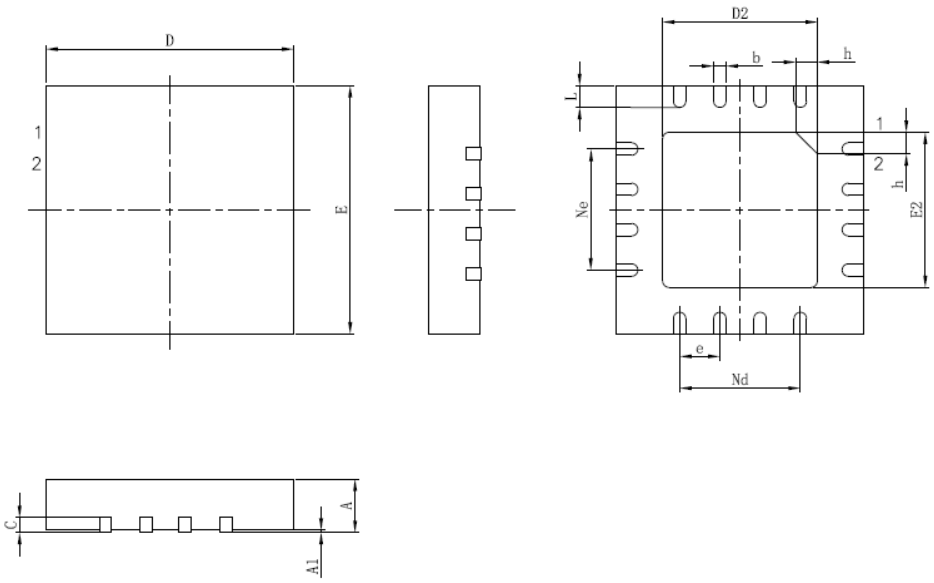
Reference 1 (port C, optocoupler feedback, PMOS)



Reference 2 (port A, FB feedback, NMOS)

11. Mechanical and Packaging

11.1. Package Summary



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.25	0.30	0.35
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.10	2.20	2.30
e	0.650BSC		
Ne	1.95BSC		
Nd	1.95BSC		
E	3.90	4.00	4.10
E2	2.10	2.20	2.30
L	0.45	0.55	0.65
h	0.30	0.35	0.40
L/F载体尺寸	98*98		

12. Revision History

V0.1 Initial version.
V1.1 Update Electrical Characteristics
V1.2 Update The Logo
V1.3 Add QC5 Report Number
V1.4 Modify RSET 24W to 25W
V1.5 Update Electrical Characteristics
V1.6 Modify Document Templates

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