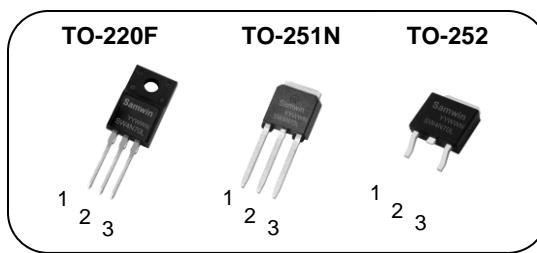


### N-channel Enhanced mode TO-220F/TO-251N/TO-252 MOSFET

#### Features

- High ruggedness
- Low  $R_{DS(ON)}$  (Typ 0.8Ω)@ $V_{GS}=10V$
- Low Gate Charge (Typ 18nC)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Application: LED, Charge, Adaptor

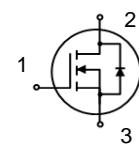


1. Gate 2. Drain 3. Source

$BV_{DSS}$  : 700V

$I_D$  : 4A

$R_{DS(ON)}$  : 0.8Ω



#### General Description

This power MOSFET is produced with advanced super junction technology of SAMWIN. This technology enable the power MOSFET to have better characteristics, including fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics.

#### Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW F 4N70L	SW4N70L	TO-220F	TUBE
2	SW N 4N70L	SW4N70L	TO-251N	TUBE
3	SW D 4N70L	SW4N70L	TO-252	REEL

#### Absolute maximum ratings

Symbol	Parameter	Value			Unit
		TO-220F	TO-251N	TO-252	
$V_{DSS}$	Drain to source voltage	700			V
$I_D$	Continuous drain current (@ $T_C=25^\circ C$ )		4*		A
	Continuous drain current (@ $T_C=100^\circ C$ )		2.5*		A
$I_{DM}$	Drain current pulsed	(note 1)	16		A
$V_{GS}$	Gate to source voltage		$\pm 30$		V
$E_{AS}$	Single pulsed avalanche energy	(note 2)	202		mJ
$E_{AR}$	Repetitive avalanche energy	(note 1)	20		mJ
dv/dt	MOSFET dv/dt ruggedness (@ $V_{DS}=0\sim 400V$ )		30		V/ns
dv/dt	Peak diode recovery dv/dt	(note 3)	20		V/ns
$P_D$	Total power dissipation (@ $T_C=25^\circ C$ )	20	125	114	W
	Derating factor above 25°C	0.16	1.0	0.9	W/°C
$T_{STG}, T_J$	Operating junction temperature & storage temperature		-55 ~ + 150		°C
$T_L$	Maximum lead temperature for soldering purpose, 1/8 from case for 5 seconds.		300		°C

\*. Drain current is limited by junction temperature.

#### Thermal characteristics

Symbol	Parameter	Value			Unit
		TO-220F	TO-251N	TO-252	
$R_{thjc}$	Thermal resistance, Junction to case	6.2	1.0	1.1	°C/W
$R_{thja}$	Thermal resistance, Junction to ambient	54	86		°C/W

### Electrical characteristic ( $T_C = 25^\circ\text{C}$ unless otherwise specified )

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>Off characteristics</b>						
$\text{BV}_{\text{DSS}}$	Drain to source breakdown voltage	$V_{\text{GS}}=0\text{V}$ , $I_D=250\mu\text{A}$	700			V
$\Delta \text{BV}_{\text{DSS}} / \Delta T_J$	Breakdown voltage temperature coefficient	$I_D=250\mu\text{A}$ , referenced to $25^\circ\text{C}$		0.89		$\text{V}/^\circ\text{C}$
$I_{\text{DSS}}$	Drain to source leakage current	$V_{\text{DS}}=700\text{V}$ , $V_{\text{GS}}=0\text{V}$			1	$\mu\text{A}$
		$V_{\text{DS}}=560\text{V}$ , $T_C=125^\circ\text{C}$			50	$\mu\text{A}$
$I_{\text{GSS}}$	Gate to source leakage current, forward	$V_{\text{GS}}=30\text{V}$ , $V_{\text{DS}}=0\text{V}$			100	nA
	Gate to source leakage current, reverse	$V_{\text{GS}}=-30\text{V}$ , $V_{\text{DS}}=0\text{V}$			-100	nA
<b>On characteristics</b>						
$V_{\text{GS(TH)}}$	Gate threshold voltage	$V_{\text{DS}}=V_{\text{GS}}$ , $I_D=250\mu\text{A}$	2.5		4.5	V
$R_{\text{DS(ON)}}$	Drain to source on state resistance	$V_{\text{GS}}=10\text{V}$ , $I_D=2\text{A}$		0.8	1.0	$\Omega$
$G_{\text{fs}}$	Forward transconductance	$V_{\text{DS}}=30\text{V}$ , $I_D=2\text{A}$		3		S
<b>Dynamic characteristics</b>						
$C_{\text{iss}}$	Input capacitance	$V_{\text{GS}}=0\text{V}$ , $V_{\text{DS}}=200\text{V}$ , $f=1\text{MHz}$		433		pF
$C_{\text{oss}}$	Output capacitance			28		
$C_{\text{rss}}$	Reverse transfer capacitance			3		
$t_{\text{d(on)}}$	Turn on delay time	$V_{\text{DS}}=350\text{V}$ , $I_D=4\text{A}$ , $R_G=25\Omega$ , $V_{\text{GS}}=10\text{V}$ (note 4,5)		10		ns
$t_r$	Rising time			25		
$t_{\text{d(off)}}$	Turn off delay time			34		
$t_f$	Fall time			24		
$Q_g$	Total gate charge	$V_{\text{DS}}=560\text{V}$ , $V_{\text{GS}}=10\text{V}$ , $I_D=4\text{A}$ , $I_g=3\text{mA}$ (note 4,5)		18		nC
$Q_{\text{gs}}$	Gate-source charge			3		
$Q_{\text{gd}}$	Gate-drain charge			10		
$R_g$	Gate resistance	$V_{\text{DS}}=0\text{V}$ , Scan F mode		2.6		$\Omega$

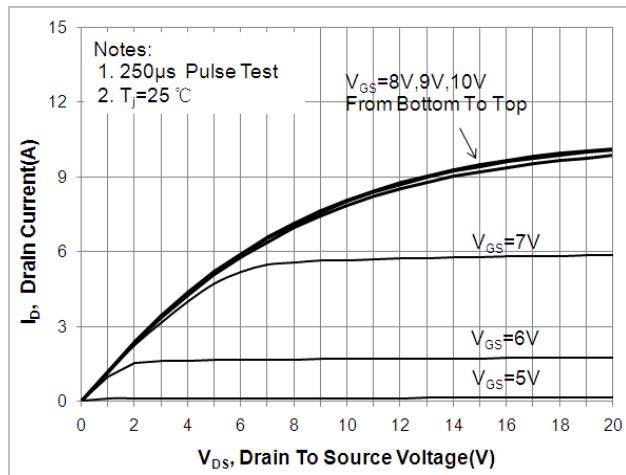
### Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			4	A
$I_{\text{SM}}$	Pulsed source current				16	A
$V_{\text{SD}}$	Diode forward voltage drop.	$I_S=4\text{A}$ , $V_{\text{GS}}=0\text{V}$			1.4	V
$t_{\text{rr}}$	Reverse recovery time	$I_S=4\text{A}$ , $V_{\text{GS}}=0\text{V}$ , $dI_F/dt=100\text{A/us}$		280		ns
$Q_{\text{rr}}$	Reverse recovery charge			2.3		$\mu\text{C}$

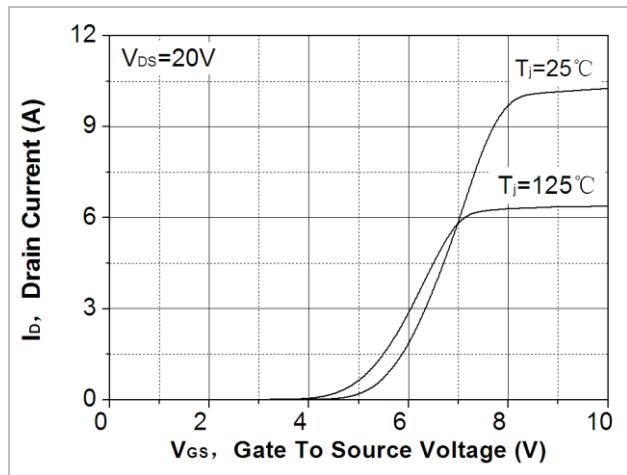
※. Notes

- Repetitive rating : pulse width limited by junction temperature.
- $L = 70\text{mH}$ ,  $I_{AS} = 2.4\text{A}$ ,  $V_{DD} = 50\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
- $I_{SP} \leq 4\text{A}$ ,  $di/dt = 100\text{A/us}$ ,  $V_{DD} \leq \text{BV}_{\text{DSS}}$ , Starting  $T_J = 25^\circ\text{C}$
- Pulse Test : Pulse Width  $\leq 300\text{us}$ , duty cycle  $\leq 2\%$ .
- Essentially independent of operating temperature.

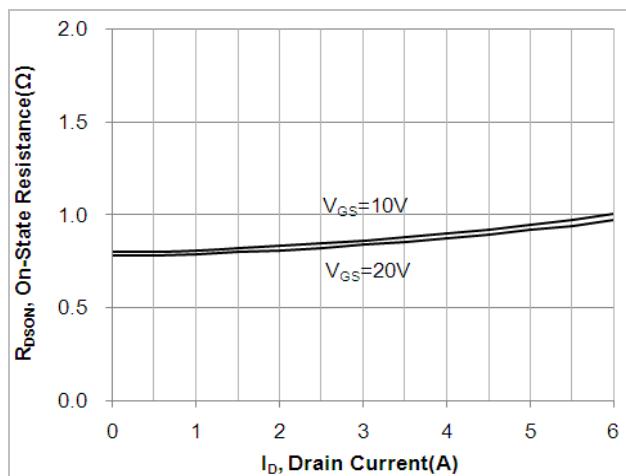
**Fig. 1. On-state characteristics**



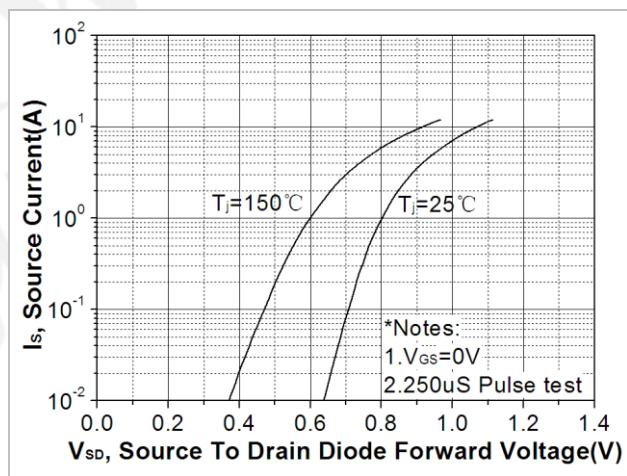
**Fig. 2. Transfer Characteristics**



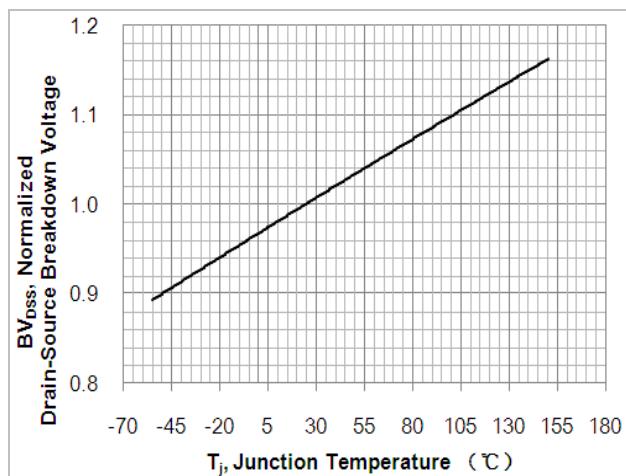
**Fig. 3. On-resistance variation vs. drain current and gate voltage**



**Fig. 4. On-state current vs. diode forward voltage**



**Fig 5. Breakdown voltage variation vs. junction temperature**



**Fig. 6. On-resistance variation vs. junction temperature**

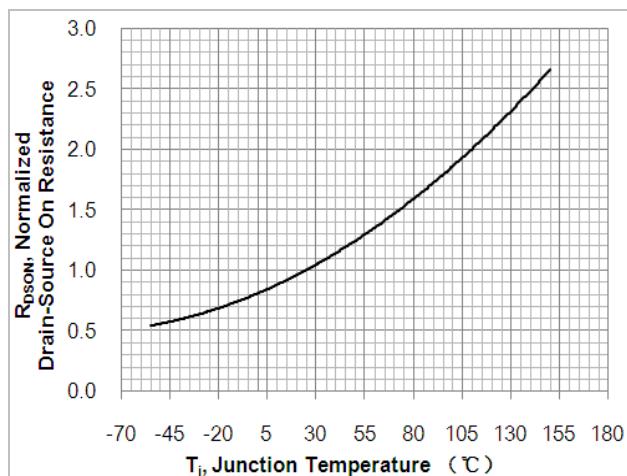


Fig. 7. Gate charge characteristics

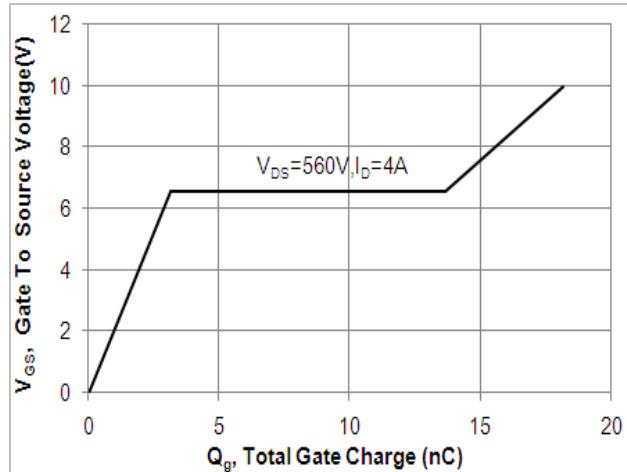


Fig. 8. Capacitance Characteristics

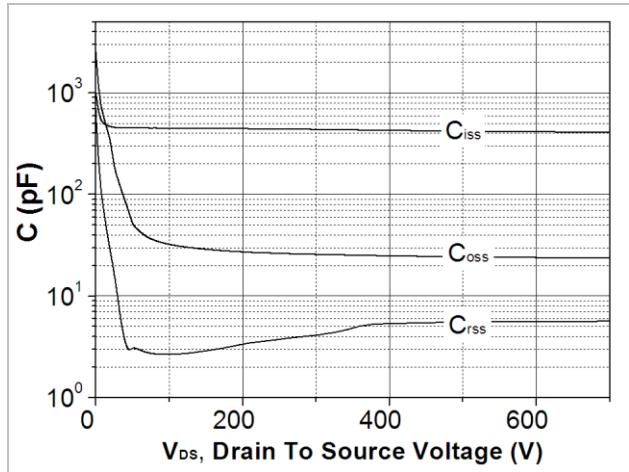


Fig. 9. Maximum safe operating area (TO-220F)

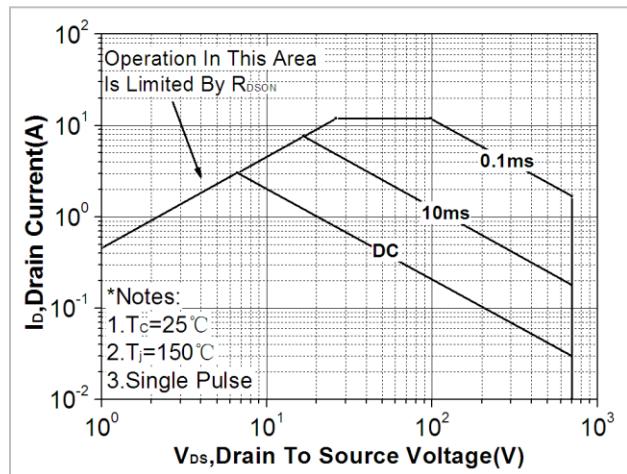


Fig. 10. Maximum safe operating area (TO-251N)

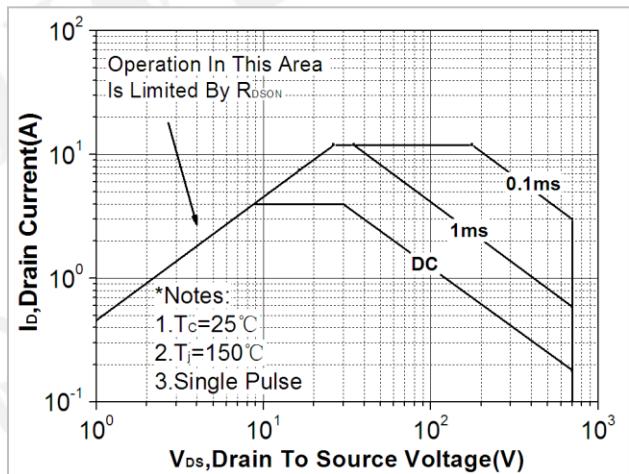


Fig.11. Maximum safe operating area (TO-252)

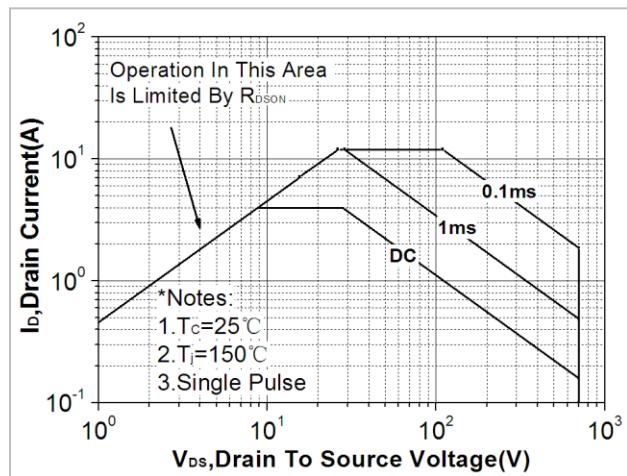


Fig. 12. Transient thermal response curve (TO-220F)

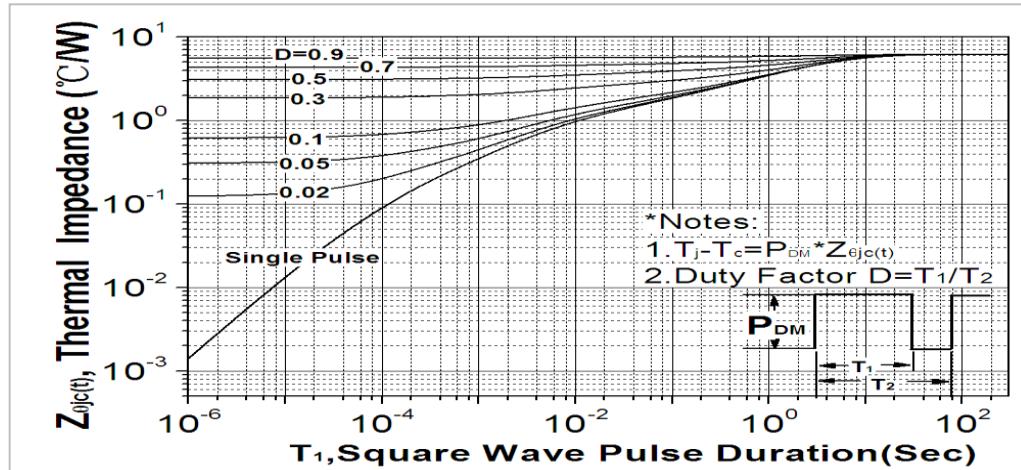


Fig. 13. Transient thermal response curve (TO-251N)

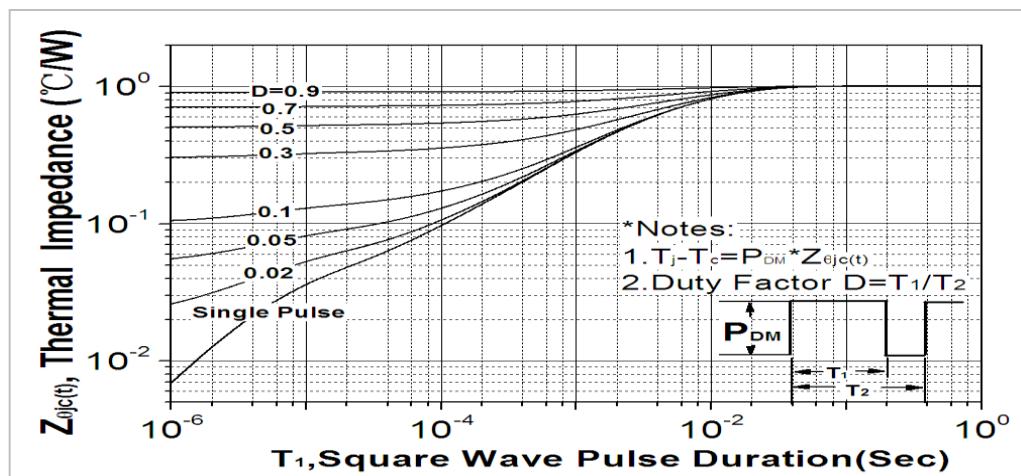


Fig. 14. Transient thermal response curve (TO-252)

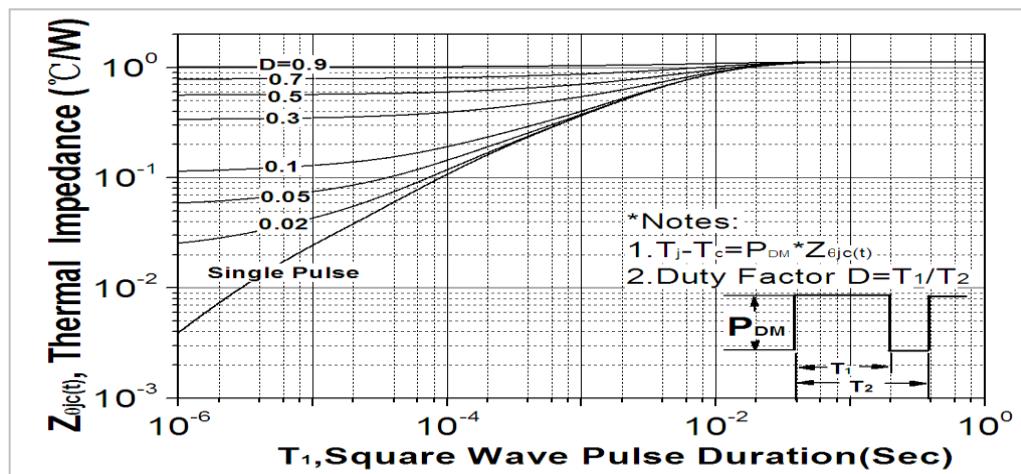


Fig. 15. Gate charge test circuit & waveform

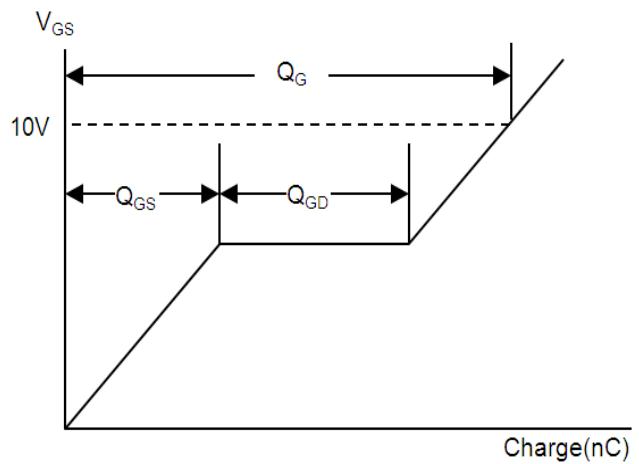
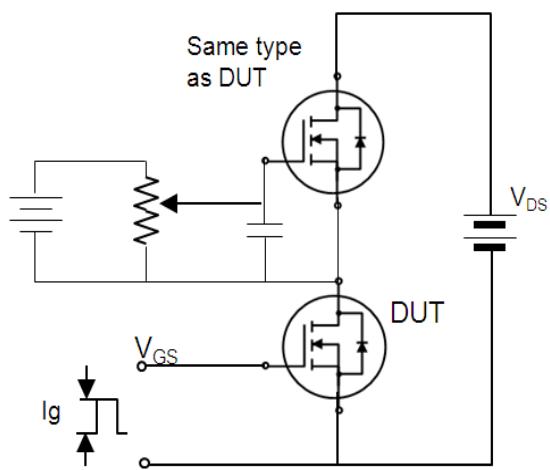


Fig. 16. Switching time test circuit & waveform

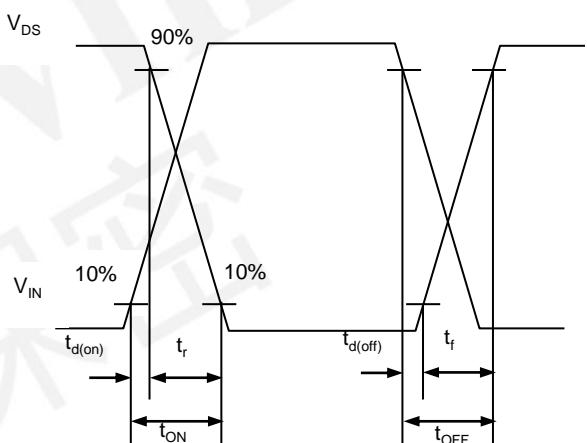
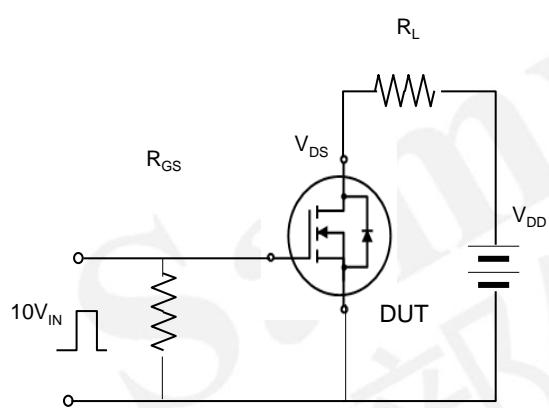


Fig. 17. Unclamped Inductive switching test circuit & waveform

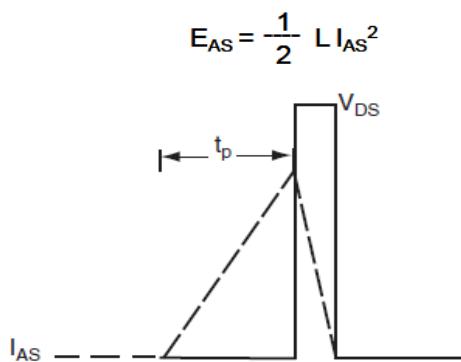
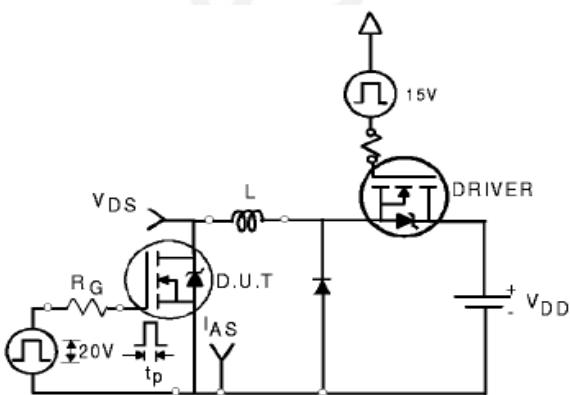
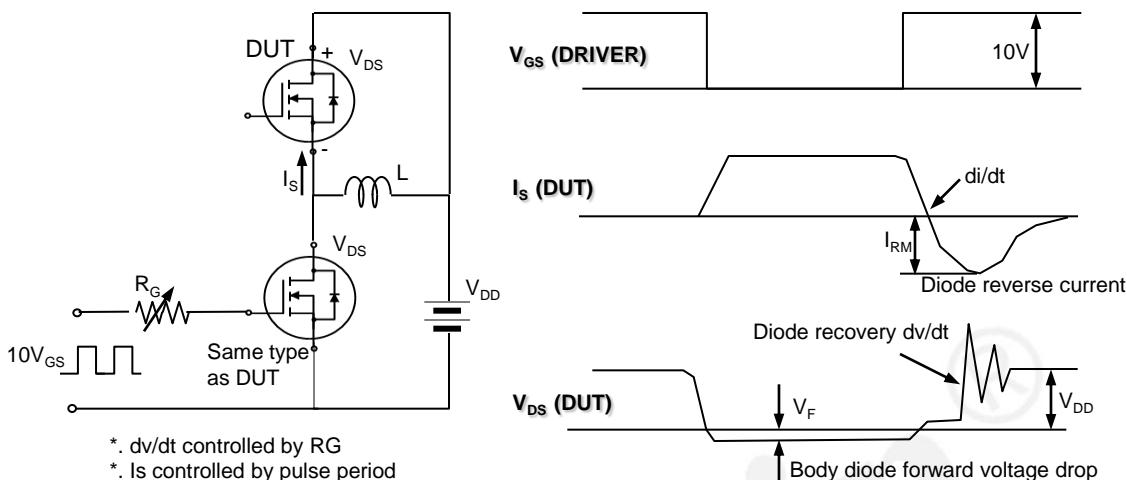


Fig. 18. Peak diode recovery dv/dt test circuit & waveform



## DISCLAIMER

- \* All the data & curve in this document was tested in XI' AN SEMIPOWER TESTING & APPLICATION CENTE R.
- \* This product has passed the PCT, TC, HTRB, HTGB, HAST, PC and Solderdunk reliability testing.
- \* Qualification standards can also be found on the Web site (<http://www.semipower.com>).
- \* Suggestions for improvement are appreciated, Please send your suggestions to [samwin@samwinsemi.com](mailto:samwin@samwinsemi.com)