SWL-A20S Datasheet

Atheros AR6002 WLAN Solution

REV 6

Samsung Electro-Mechanics

2009-09-10

Summary

This datasheet presents the general performance and specifications of SWL-A20S IEEE 802.11b/g Wireless LAN module.

Table of Contents

1 General Description

1.1 Functional Description

SWL-A20S is the compact size and low power System-in-Package (SiP) for IEEE 802.11b/g wireless LAN (WLAN) aimed at embedded and mobile applications.

SWL-A20S is based on Atheros AR6002 solution.

SWL-A20S supports both SDIO1.1 and GSPI host interface.

1.2 Features

- IEEE Std 802.11b/g Standard Compliant
- Includes all the base-band and radio functionality, from host interface up to antenna, needs only external antenna
- Small dimensions (9.5 x 9.5 x 1.6 mm) with an LGA - 52pin peripheral footprint
- Low Power Consumption
- Cellular Coexistence Supported
- Standard 2,3 and 4 wire Bluetooth coexistence handshake supported
- Host Interface: SDIO and GSPI
- RoHS Compliant

1.2.1 Power Management

- Supply voltage range

1.2V	1.2V +/-5% (ripple Vpp<15mV)
1.8V	1.8V +/-5% (ripple Vpp<45mV)
VBATT	3.2~4.2V (Recommend 3.3V, ripple Vpp<15mV)
SDIO Interface Voltage	Need to meet SDIO High signal level

- Power Consumption

WLAN	600 mW (@11b Continuous Tx) 130 mW (@ Continuous Rx)

1.2.2 Radio Transceiver

- Fully compliant with IEEE 802.11/b/g
- Receiver sensitivity (< 8% PER) at 11 Mbit/sec data rate: -87 dBm
- Receiver sensitivity (< 10% PER) at 54 Mbit/sec data rate: -74 dBm
- Blocking filter for suppression of CDMA, GSM, PCS and WCDMA interfering signals
- Transmitter output power in 802.11b mode: +15 dBm
- Transmitter output power in 802.11g mode at 6~24Mbps: +15 dBm

1.2.3 Applications

- Smart phone/feature phones with embedded WLAN connectivity
- Personal digital assistants (PDA)
- SDIO WLAN Network Interface Cards (NIC)
- Voice over IP (VoIP) cordless phones
- Mobile gaming devices
- Portable media players (PMP) including networked MP3 player
- Networked digital camera and photo frames
- Digital media adapter and receiver
- Networked TV, set-top box, DVD recorder, personal video recorder (PVR), media drive, and other consumer electronics appliances

1.3 Block Diagram

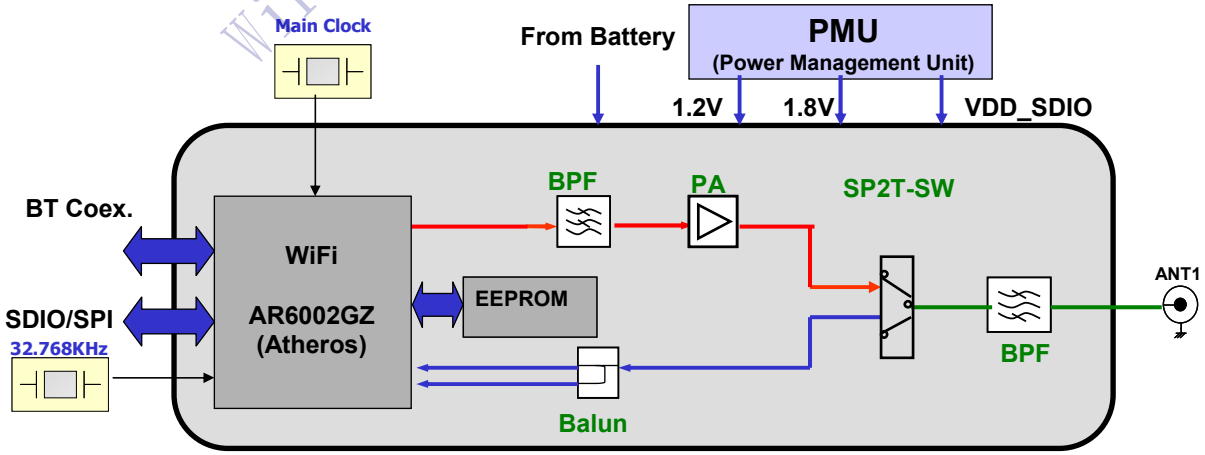


Figure 1-1 SWL-A20S Hardware block diagram

2 Dimension and Pin Assignments

2.1 Mechanical Dimension

<Top View>

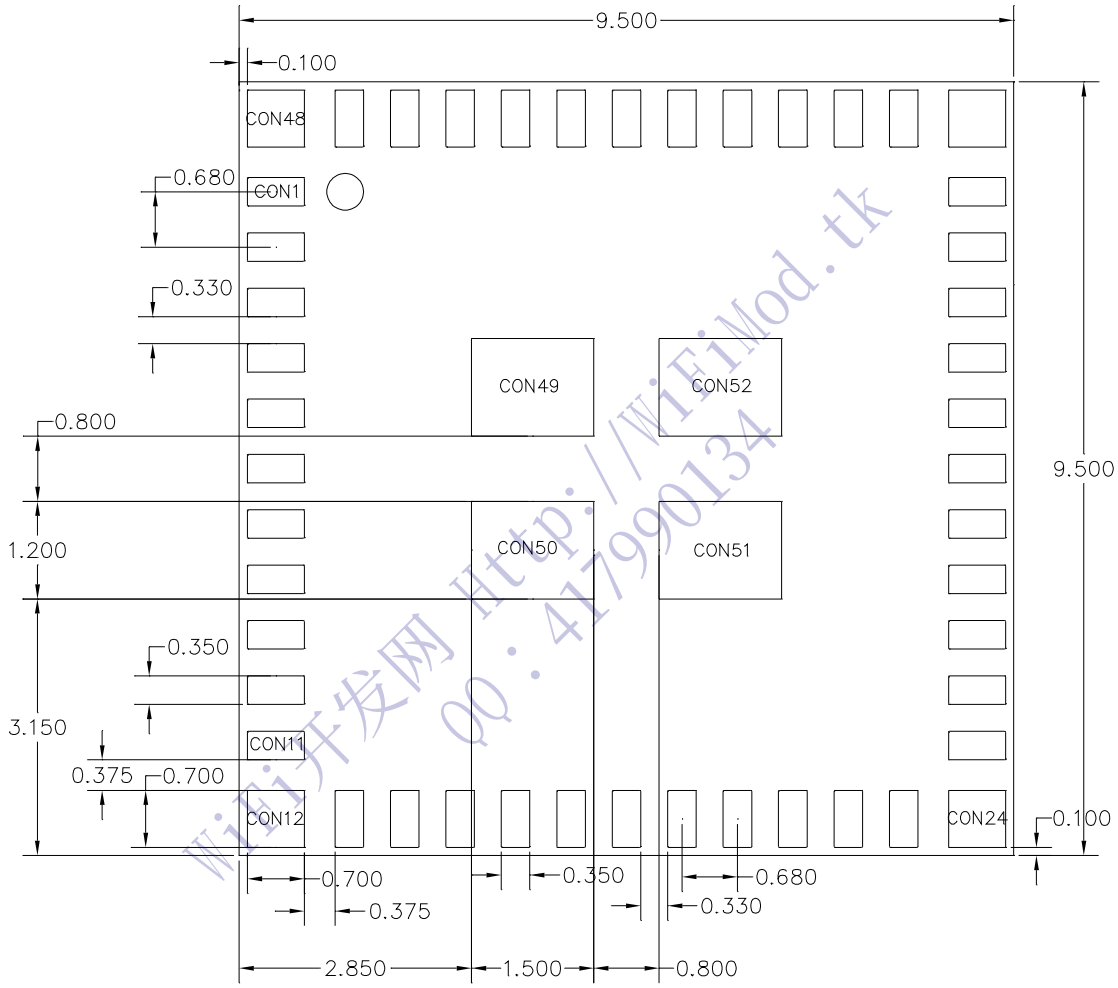


Figure 2-1 SWL-A20S Mechanical Dimension

Parameter	Min.	Nom.	Max.	Unit
X	9.4	9.5	9.6	mm
Y	9.4	9.5	9.6	mm
Height			1.60	mm

2.2 Pin Assignments

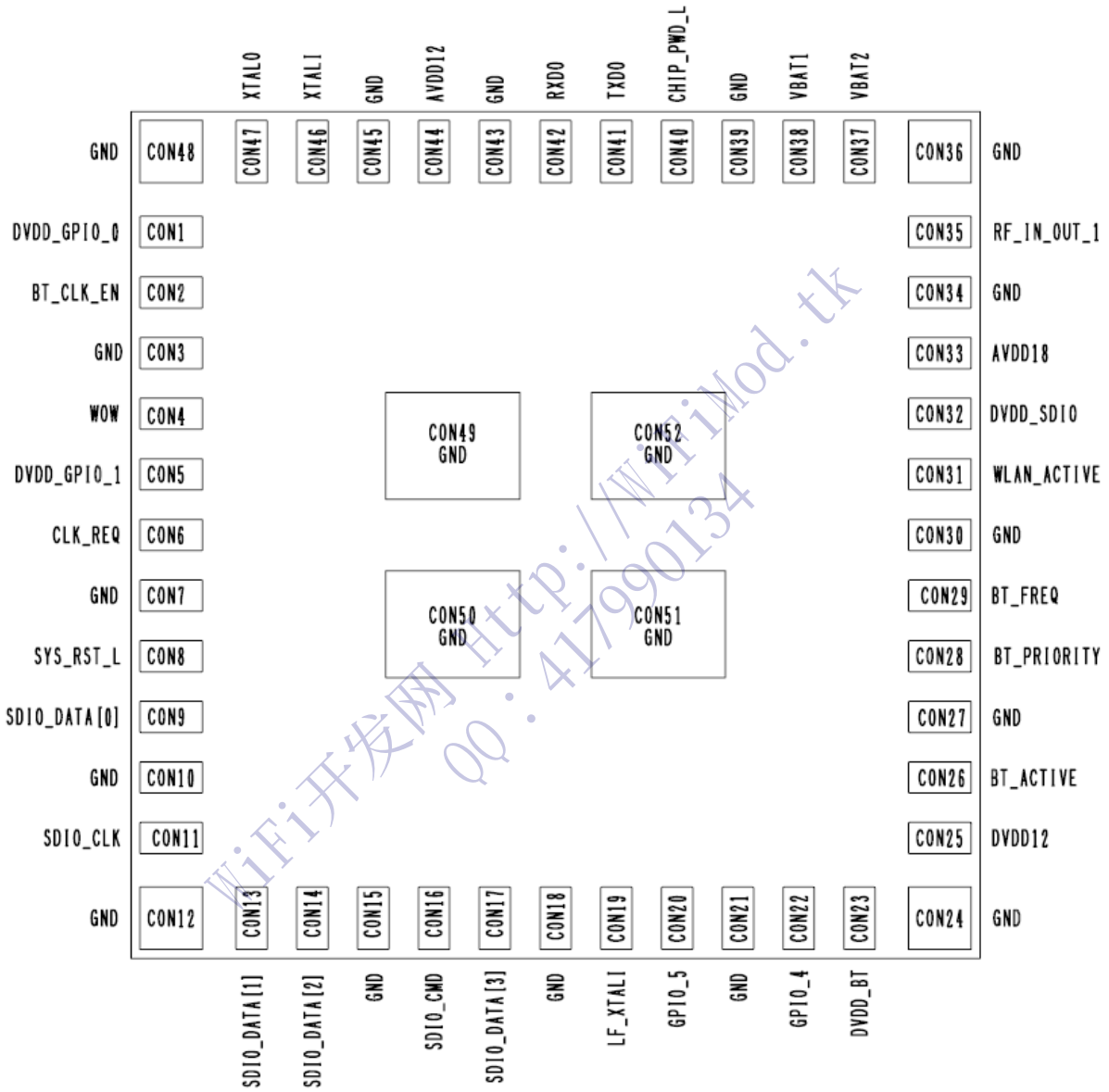


Figure 2-2 SWL-A20S Pin Assignments (Top View)

No.	Name	No.	Name	No.	Name	No.	Name
1	DVDD_GPIO_0	14	SDIO_DATA[2]	27	GND	40	CHIP_PWD_L
2	BT_CLK_EN	15	GND	28	BT_PRIORITY	41	TXDO
3	GND	16	SDIO_CMD	29	BT_FREQ	42	RXDO
4	WOW	17	SDIO_DATA[3]	30	GND	43	GND
5	DVDD_GPIO_1	18	GND	31	WLAN_ACTIVE	44	AVDD12
6	CLK_REQ	19	LF_XTALI	32	DVDD_SDIO	45	GND
7	GND	20	GPIO_5	33	AVDD18	46	XTALI
8	SYS_RST_L	21	GND	34	GND	47	XTALO
9	SDIO_DATA[0]	22	GPIO_4	35	RF_IN_OUT_1	48	GND
10	GND	23	DVDD_BT	36	GND	49	GND
11	SDIO_CLK	24	GND	37	VBAT2	50	GND
12	GND	25	DVDD12	38	VBAT1	51	GND
13	SDIO_DATA[1]	26	BT_ACTIVE	39	GND	52	GND

3 Pin Descriptions

3.1 Interface, I/O, Control and Clock Pins

Pin #	Pin Name	Description	Type	Circuit	Reset	Supply
SDIO Interface						
11	SDIO_CLK	SDIO input clock from Host (up to 25MHz)	I	DI	-	DVDD_SDIO
16	SDIO_CMD	SDIO command	IO	DIO	PU	DVDD_SDIO
9	SDIO_DATA[0]	SDIO data bit [0]	IO	DIO	PU	DVDD_SDIO
13	SDIO_DATA[1]	SDIO data bit [1]	IO	DIO	PU	DVDD_SDIO
14	SDIO_DATA[2]	SDIO data bit [2]	IO	DIO	PU	DVDD_SDIO
17	SDIO_DATA[3]	SDIO data bit [3]	IO	DIO	PU	DVDD_SDIO
Antenna RF Port						
35	RF_IN_OUT_1	RF antenna port for 2.4G; 50Ohm	IO	RF IO	-	-
Clock Interface						
47	XTALO	Reference crystal output External clock source input	Crystal Output	-	-	-
46	XTALI	Reference crystal input	Crystal Input	-	-	-
6	CLK_REQ	External clock request	O	DO	PD	DVDD_SDIO
19	LF_XTALI	32KHz crystal input	I	DI	-	DVDD_BT
Bluetooth Coexistence Interface						
26	BT_ACTIVE		I	DI		DVDD_BT
28	BT_PRIORITY		I	DI		DVDD_BT
29	BT_FREQ		I	DI		DVDD_BT
31	WLAN_ACTIVE		O	DO		DVDD_BT
Miscellaneous Pins						
40	CHIP_PWD_L		I	DI	PD	DVDD_SDIO
8	SYS_RST_L	AR6002 Reset	I	DI	PU	DVDD_SDIO
4	WOW	wake-on-wireless(WOW)	O	DO	PD	DVDD_GPIO1
41	TXD0	Tx Data from module	O	DO	PU	DVDD_GPIO0
42	RXD0	Rx data from serial transceiver board	IO	DIO	PU	DVDD_GPIO0
22	GPIO_4	Mode configuration(For SDIO "H")	IO	DIO	-	DVDD_SDIO
20	GPIO_5	Mode configuration(For SDIO "H")	IO	DIO	-	DVDD_SDIO
2	BT_CLK_EN	Indicate BT is working	I	DI	-	-

"Type" Column: I=Input, O=Output, IO=Bi-directional
"Circuit" Column: DI=Digital Input, DO=Digital Output, DIO=Digital Bi-directional
"Reset" Column: PL=Plain, PD=Pull-down, PU=Pull-up

3.2 Power Supply Pins

Pin #	Pin Name	Description	Min.	Nom.	Max.	Unit
32	DVDD_SDIO	SDIO interface voltage (Meet SDIO signal level)	1.71	2.6	3.46	V
37	VBAT2	PA supply voltage	3.2	3.3	4.2	V
38	VBAT1	Internal LDO supply voltage	3.2	3.3	4.2	V
23	DVDD_BT	BT-Coexistence IO Supply (Meet BT IO level)	1.71	2.6	3.46	V
1	DVDD_GPIO_0	GPIO supply voltage for TXDO, RXDO, Internal EEPROM	1.71	1.8	3.46	V
5	DVDD_GPIO_1	GPIO supply voltage for WOW Meet host WOW level	1.71	2.6	3.46	V
25	DVDD12	1.2V Digital core	1.14	1.2	1.26	V
44	AVDD12	Analog 1.2V	1.14	1.2	1.26	V
33	AVDD18	Analog 1.8V	1.71	1.8	1.89	V
3	GND					-
7	GND					-
10	GND					-
12	GND					-
15	GND					-
18	GND					-
21	GND					-
24	GND					-
27	GND					-
30	GND					-
34	GND					-
36	GND					-
39	GND					-
43	GND					-
45	GND					-
48	GND					-
49	GND					-
50	GND					-
51	GND					-
52	GND					-

4 Electrical Characteristics

4.1 DC Characteristics

4.1.1 Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Max.	Unit
VBAT1	Internal LDO supply voltage		-0.3	4.35	V
VBAT2	PA supply voltage		-0.3	4.35	V
DVDD_BT	BT-Coexistence IO level		-0.3	4.0	V
DVDD_GPIO_0	Some GPIO supply voltage		-0.3	4.0	V
DVDD_GPIO_1	Some GPIO supply voltage		-0.3	4.0	V
DVDD12	1.2V Digital core		-0.3	1.35	V
AVDD12	Analog 1.2V		-0.3	1.35	V
AVDD18	Analog 1.8V		-0.3	2.5	V

4.2 Environmental Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
ESD	Electro-static discharge voltage	HBM	-2000	2000	V
Top	Operating temperature		-20	70	°C
Tstg	Storage temperature		-30	85	°C

*HBM : Human Body Model
ESD Class 1C

4.3 Power Consumption

Parameter	Conditions	Min.	Nom.	Max.	Unit
Tx mode (11b Max current)					
1.2V	Tx 99% @11b Tx 15dBm		39		mA
1.8V			62		mA
IO Part (General 2.6V)			5.5		uA
VBAT1 + VBAT2			116		mA
Tx mode (11g Max current)					
1.2V	Tx 99% @11g Tx 15dBm		46		mA
1.8V			62		mA
IO Part (General 2.6V)			5.5		uA
VBAT1 + VBAT2			110		mA
Rx mode					
1.2V	Rx @Max gain		62		mA
1.8V			27		mA
IO Part (General 2.6V)			5.5		uA
VBAT1 + VBAT2			0.1		mA
Sleep mode					
1.2V			0.488		mA
1.8V			0.013		mA
IO Part (General 2.6V)			5.5		uA
VBAT1 + VBAT2			0.003		mA

5 RF Specifications

All measurements are made under nominal supply voltage and room temperature conditions.

5.1 Receiver RF Specifications

Parameter	Conditions	Min.	Nom.	Max.	Unit
Minimum receiver sensitivity in 802.11 mode					
1Mbps	PER<8%, Packet size= 1024bytes		-96	-80*	dBm
2Mbps			-92	-80*	dBm
Minimum receiver sensitivity in 802.11b mode					
5.5Mbps	PER<8%, Packet size= 1024bytes		-90	-76*	dBm
11Mbps			-87	-76*	dBm
Minimum receiver sensitivity in 802.11g mode					
6Mbps	PER<10%, Packet size= 1024bytes		-92	-82*	dBm
9Mbps			-91	-81*	dBm
12Mbps			-90	-79*	dBm
18Mbps			-88	-77*	dBm
24Mbps			-84	-74*	dBm
36Mbps			-80	-70*	dBm
48Mbps			-76	-66*	dBm
54Mbps			-74	-65*	dBm
Maximum input level					
Maximum input signal level in 802.11b	PER<8%	-10*			dBm
Maximum input signal level in 802.11g	PER<10%	-20*			dBm
Adjacent channel rejection (ACR) in 802.11 mode					
1Mbps	PER<8%, Packet size= 1024bytes	35*			dB
2Mbps		35*			dB
Adjacent channel rejection (ACR) in 802.11b mode					
5.5Mbps	PER<8%, Packet size= 1024bytes	35*			dB
11Mbps		35*			dB
Adjacent channel rejection (ACR) in 802.11g mode					
6Mbps	PER<10%, Packet size= 1024bytes	16*			dB
9Mbps		16*			dB
12Mbps		13*			dB
18Mbps		11*			dB
24Mbps		8*			dB
36Mbps		4*			dB
48Mbps		0*			dB
54Mbps		-1*			dB

"*" Indicate IEEE 802.11 specifications

5.2 Transmitter RF Specifications

Parameter	Conditions	Min	Nom	Max	Unit
Linear average output power in 802.11b mode					
Average output power@1~11Mbps	As specified in IEEE802.11 Chap.17~19	13	15	17	dBm
Linear average output power in 802.11g mode					
Average output power@6~24Mbps	As specified in IEEE802.11 Chap.17~19	13	15	17	dBm
Average output power@36Mbps		13	15	17	dBm
Average output power@48Mbps		12	14	16	dBm
Average output power@54Mbps		11	13	15	dBm
Transmit spectrum mask					
Margin to 802.11b spectrum mask	Maximum output power	0			dB
Margin to 802.11g spectrum mask		0			dB
Transmit modulation accuracy in 802.11b mode					
1Mbps	As specified in IEEE802.11b			35	%
2Mbps				35	%
5.5Mbps				35	%
11Mbps				35	%
Transmit modulation accuracy in 802.11g mode					
6Mbps	**Mandatory**			**-5**	**dB**
9Mbps	Option			-8	dB
12Mbps	**Mandatory**			**-10**	**dB**
18Mbps	Option			-13	dB
24Mbps	**Mandatory**			**-16**	**dB**
36Mbps	Option			-19	dB
48Mbps	Option			-22	dB
54Mbps	Option			-25	dB
Transmit power-on and power-down ramp time in 802.11b mode					
Transmit power-on ramp time from 10% to 90% output power				2	usec
Transmit power-down ramp time from 90% to 10% output power				2	usec

Frame-to-Frame output power has +/-1.5dB fluctuation from the average output power

6 Assembly Recommendations

6.1 Printed Circuit Board and Stencil Design

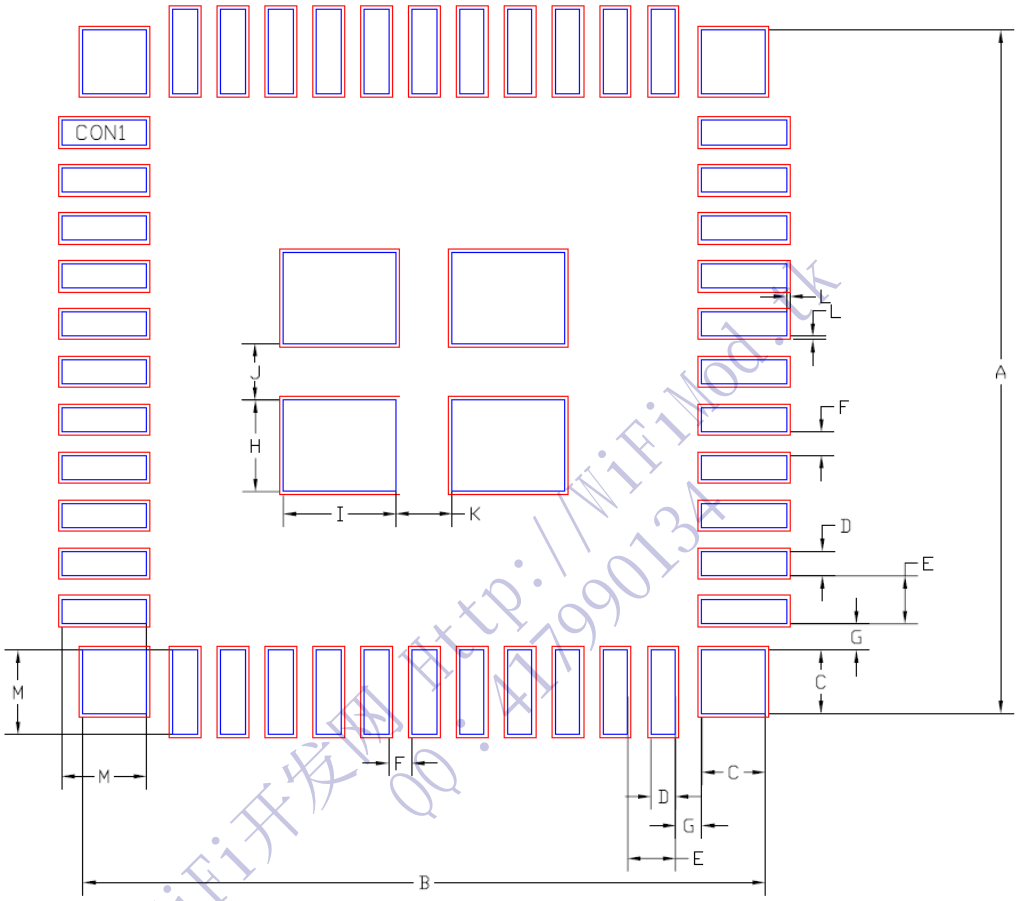


Figure 6-1 PCB and Stencil Design (Top View)

Dimension Label	Nom.	Unit	Dimension	Nom.	Unit
A	9.700	mm	H	1.300	mm
B	9.700	mm	I	1.600	mm
C	0.900	mm	J	0.700	mm
D	0.350	mm	K	0.700	mm
E	0.680	mm	L	0.050	mm
F	0.330	mm	M	1.200	mm
G	0.375	mm			

* Note
Land: Blue Color
SR Open: Red Color
Metal Mask Open Size = Land Size (Customer needs to modify based on their production line)

6.1.1 PCB Finish

The SWL-A20S can be mounted on a variety of PCB finishes such as immersion gold (Ni/Au) or Hot air solder level (HASL) or Organic Surface Protection (OSP).

Ni/Au finish is recommended. OSP is not recommended in cases that OSP does not withstand a Pb-free or a double-sided reflow application.

6.2 Reflow and Soldering

6.2.1 Solder Paste

Standard (No-clean) Sn/Pb (63%/37%) or Pb-free solder pastes should be used for soldering the package. Solder pastes should be selected based on their printing and reflow behavior. For Pb-free solder paste it is recommended to use "SAC" type solder paste (e.g. SnAg3.8Cu0.7) with melting point of 217°C.

6.2.2 Reflow Profile

Industrial convection reflow oven should be used to mount the packages. The profile depends on the printed circuit board and other components that are used in the customer application. For maximum peak temperature JEDEC specification should be followed. Following reflow profile and constraints are recommended for eutectic Sn/Pb and Pb-free reflow solders

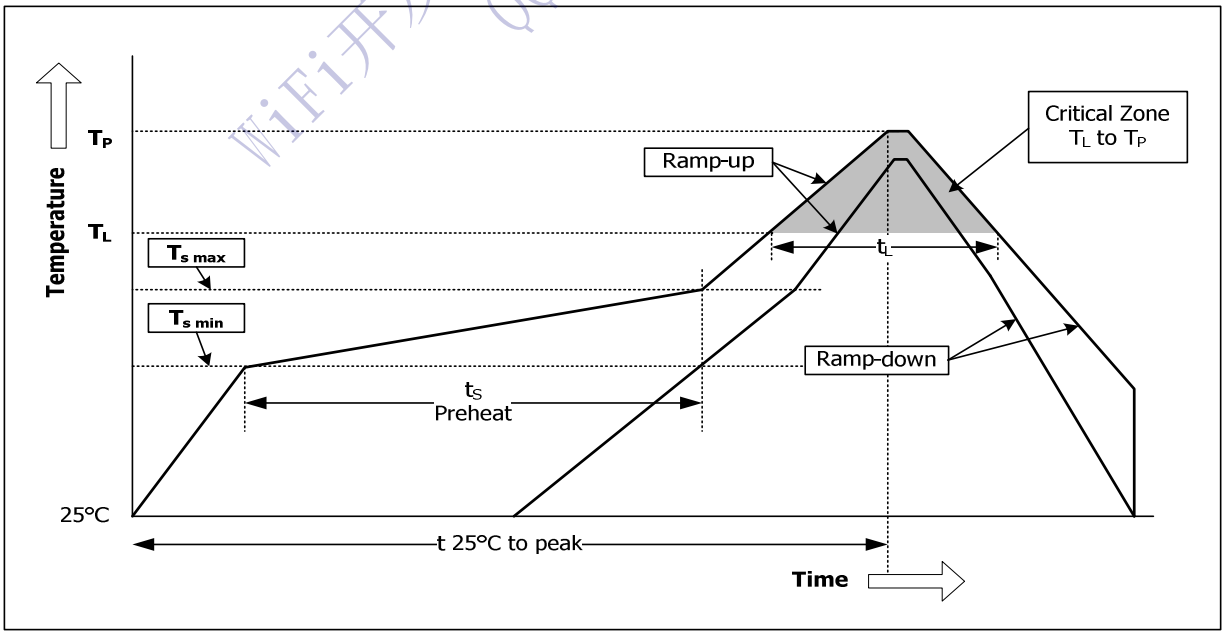


Figure 6-1 Recommended Reflow Temperature Profile

	Eutectic Sn/Pb	Pb-free
Average ramp-up rate (T_{Smax} to T_p)	2°C /second max	2°C /second max
Preheat		
-Temperature Min(T_{Smin})	100 °C	150 °C
-Temperature Max(T_{Smax})	150 °C	200 °C
-Time(T_{Smin} to T_{Smax})	60-120 seconds	75-90 seconds(≤0.75℃/second)
Time maintained above:		
-Temperature(T_L)	183 °C	217 °C
-Time(t_L)	60-90 seconds	70-90 seconds
Max. Peak Temperature(T_p)	240 +/-5 °C	255 ± 5 °C (max 260°C)
Time within 5℃ of actual Peak Temperature(t_P)	10-30 seconds	20-30 seconds
Ramp-Down Rate	>180°C: 2 °C /second max. <180°C: 6 °C /second max.	>180°C: 2 °C /second max. <180°C: 6 °C /second max.
Minimum Peak Temperature(Tp_{min})	205 °C	230 °C
Time 25 °C to Tp	4-5 minutes	4-5 minutes

7 Additional Information

7.1 Host Interface Configuration

GPIO4	GPIO5	Configuration
0	0	GSPI Mode
1	1	SDIO Mode

7.2 Power On/Off Sequences

The CHIP_PWD_L or SYS_RST_L ports can be used to reset the chip. If CHIP_PWD_L is used to reset the chip, a ~20ms delay occurs before the AR6002 is ready. In addition, unlike SYS_RST_L, CHIP_PWD_L can be used to put the AR6002 into CHIP_PWD power state. Figure 7-1, Figure 7-2 and Figure 7-3 show the CHIP_PWD_L, SYS_RST_L, and power supply domain timing diagrams. Table 7-1 describes the symbols used in these figures.

It is recommended that for power savings, CHIP_PWD_L be driven low and all I/O supplies remain in place when A20S is not in use. The core 1.2V supply can be left on or off. For proper reset, if any supplies have been turned off, CHIP_PWD_L (or SYS_RST_L) must remain low, or toggled after, until all supplies have stabilized.

The AR6002 has an internal pull-down on CHIP_PWD_L, so when the host pulls it high, the pad sinks current. The amount of current ranges from ~10uA to ~40uA. As a result, the solution power consumption is at least 18~132uW higher than the chip power consumption in non-CHIP_PWD states. The AR6002 has an internal pull-up on SYS_RST_L, thus to minimize CHIP_PWD power consumption, customer designs should not tie CHIP_PWD_L and SYS_RST_L together.

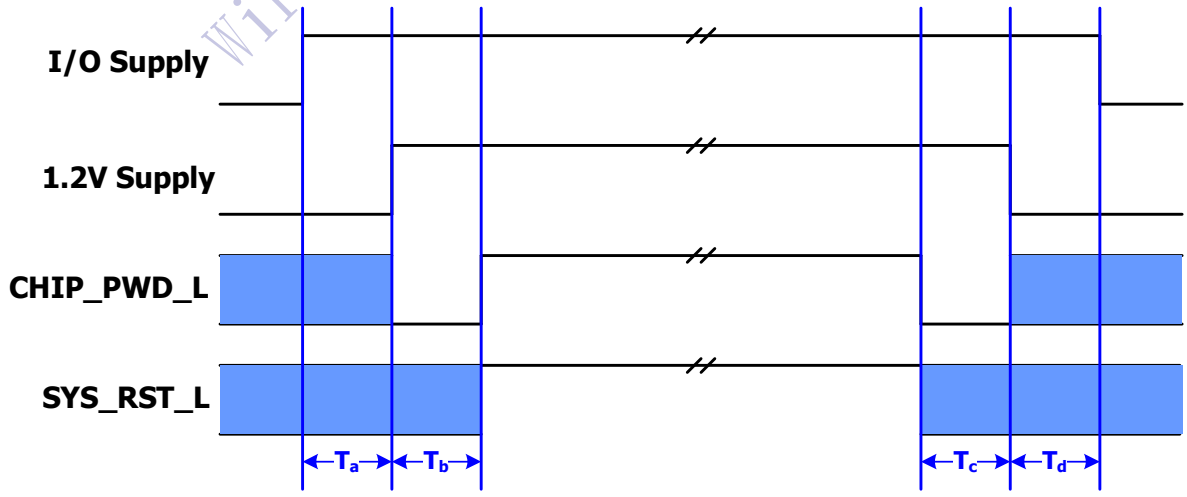


Figure 7-1 Power-Up/Power-Down Timing While Asserting CHIP_PWD_L

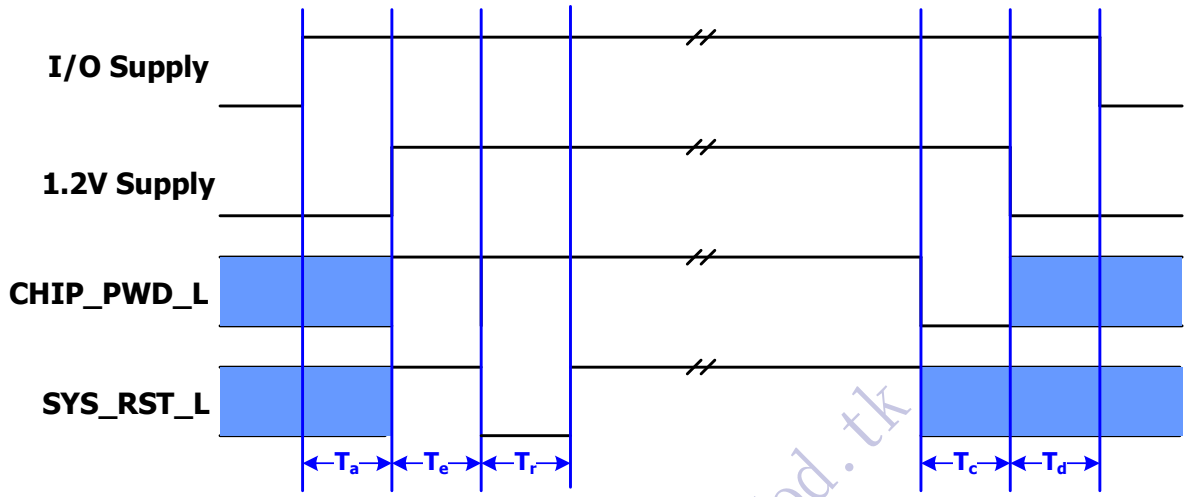


Figure 7-2 Power-Up/Power-Down Timing While Asserting SYS_RST_L

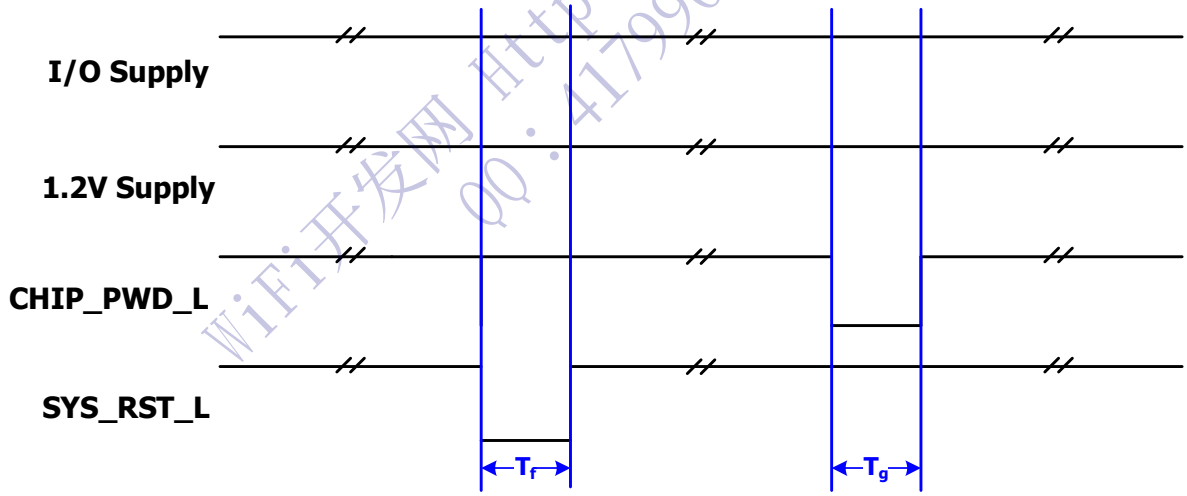


Figure 7-3 Reset and Power Cycle Timing

I/O Supply = AVDD18, DVDD_SDIO, DVDD_BT, DVDD_GPIO_0, DVDD_GPIO_1, VBAT1

1.2V Supply = DVDD12, AVDD12

Symbol	Description	Min
Ta	Time between I/O supply valid* and 1.2V supply valid	0 us
Tb	Time between 1.2V supply valid and CHIP_PWD_L deassertion	5 us
Tc	Time between CHIP_PWD_L or SYS_RST_L assertion and 1.2V supply invalid	0 us
Td	Time between 1.2V supply invalid and I/O supply invalid	0 us
Te	Time between 1.2V supply valid and SYS_RST_L assertion	0 us
Tf	Length of SYS_RST_L pulse	1 us
Tg	Length of CHIP_PWD_L pulse	5 us

Table 7-1 Timing Diagram Definitions

"*" Supply valid represents the voltage level has reached 90% level.

7.3 Reference and Sleep Clock requirements

7.3.1 Low-Frequency/Sleep/32KHz clock

LF-XTALI is pin used for the 32KHz sleep clock of SWL-A20S WLAN section. The 32KHz sleep clock line is DC-coupled into LF-XTALI pin. The LF-XTALI input clock timing and voltage requirements are shown below.

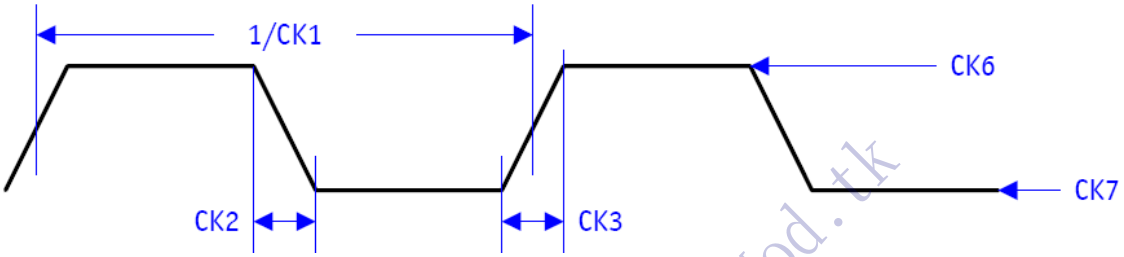


Figure 7-4 LF-XTALI Input clock timing

Symbol	Description	Min.	Nom.	Max.	Unit
CK1	Frequency	-	32.768	-	KHz
CK2	Fall Time	-	-	100	ns
CK3	Rise Time	-	-	100	ns
CK4	Duty Cycle (High-to-Low Ratio)	15	-	85	%
CK5	Frequency Stability	-50	-	50	ppm
CK6	Input High Voltage	0.8*DVDD_BT	-	DVDD_BT+0.2	V
CK7	Input Low Voltage	-0.3	-	DVDD_BT*0.2	V

7.3.2 Reference clock

XTALI and XTALO are the pins used for the reference clock. The reference clock is the primary clock source for the SWL-A20S.

SWL-A20S can support 26MHz reference clock.

Reference clock source may come from either an external crystal or oscillator source.

Three hardware solutions are used for the reference clock

- External crystal option(use KSS CX3225SB CX-101F or equivalent)
- External reference clock option(i.e., XO,VCXO, or VCTCXO)
- Host reference drive option

For the last two options, the CLK_REQ output from the SWL-A20S can enable the clock reference source or assert a request to the host. Also, for the latter two options, the phase noise requirements for the SWL-A20S at the XTALO pin are shown below.

- -145dBc/Hz at 20KHz
- -150dBc/Hz at 100KHz
- -155dBc/Hz at 200KHz

The external reference clock option or host reference drive option voltage requirements are shown below.

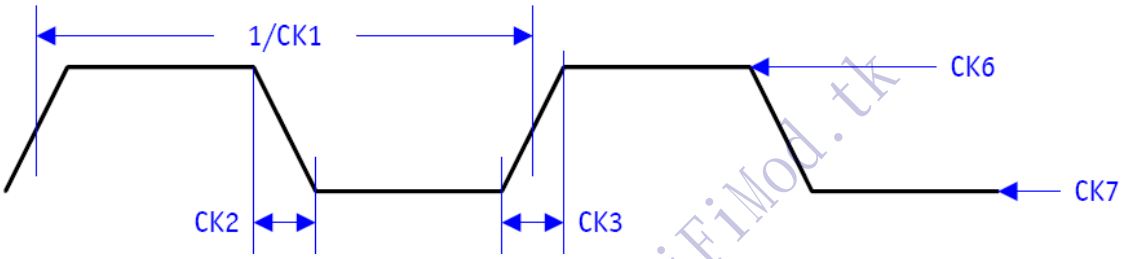


Figure 7-5 External reference clock option or Host reference drive option

Symbol	Description	Min.	Nom.	Max.	Unit
CK2	Fall Time	-	-	0.1*Period	ns
CK3	Rise Time	-	-	0.1*Period	ns
CK4	Duty Cycle (High-to-Low Ratio)	40	-	60	%
CK5	Frequency Stability	-20	-	20	ppm
CK6	Input High Voltage	0.75	-	3.46	V
CK7	Input Low Voltage	-0.55	-	0.3	V

8 Application Reference Design

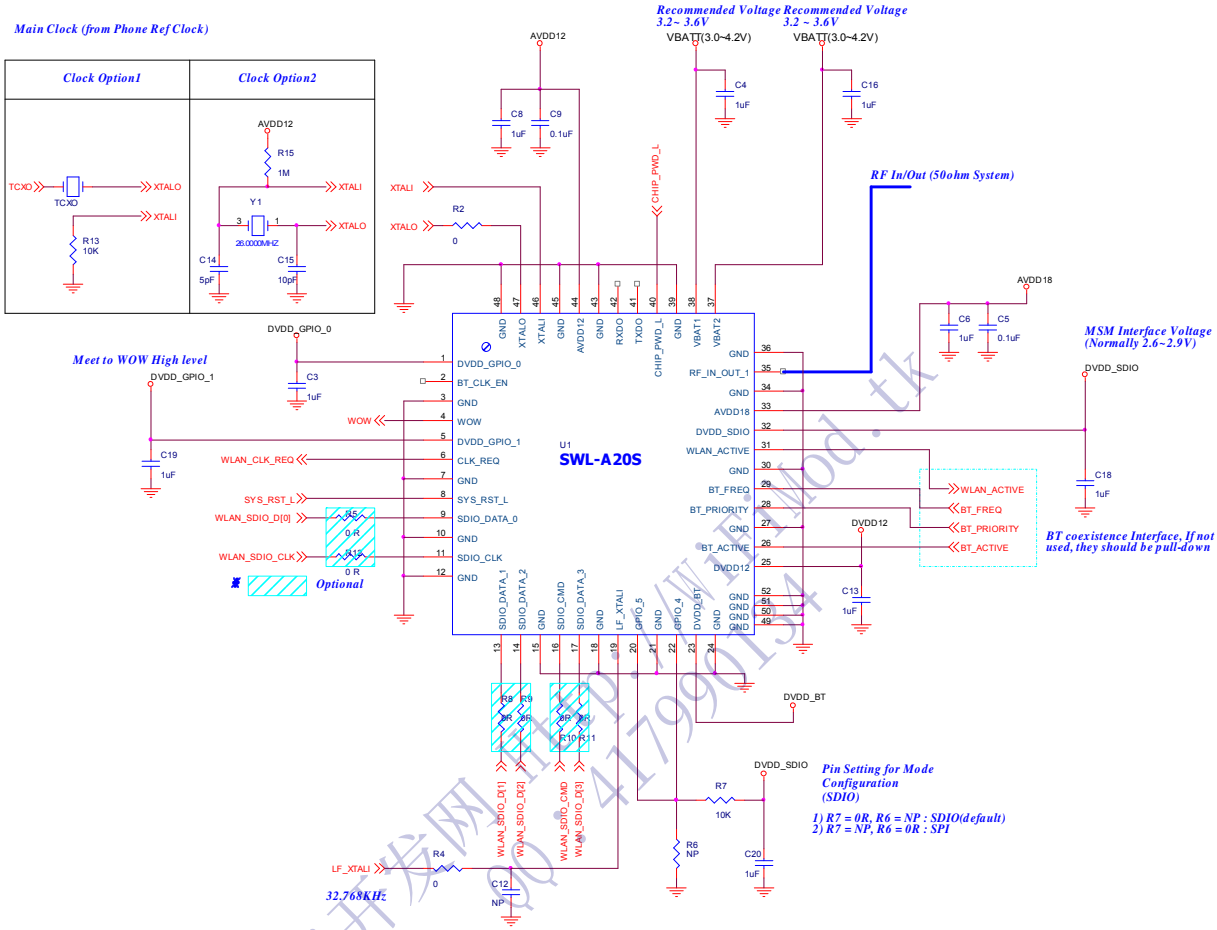
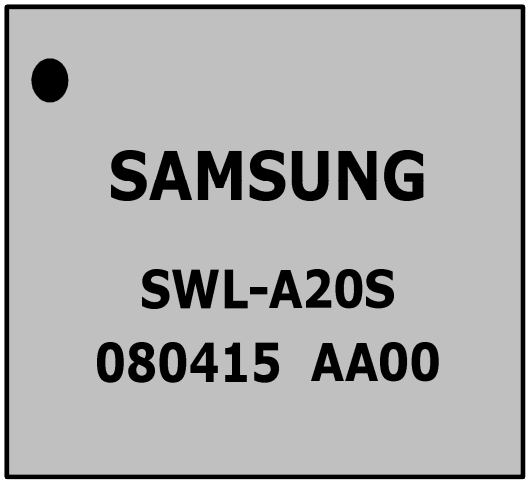


Figure 8-1 Reference Schematic for SWL-A20S SDIO Interface Application

9 Marking Information



0 8	0 4	1 5		A	A	0	0
YY	MM	DD		a	b	c	d

No.	Description
YY	Year: 20XX, XX: 00~99 (ex. 08 = 2008)
MM	Month: XX: 01~12 (ex. 04 = April)
DD	Day: XX: 1~31 (ex. 15: 15st)
a	Manufacture lot
b	Revision information
c	Factory information (0:SEMCO, 1:SEMTHAI)
d	Product sub-code

Revision History

Revision	Date	Descriptions
1	2008-04-05	Created
2	2008-04-23	Modified Printed circuit board and stencil design Added the viewpoint in the dimension and pin assignments
3	2008-07-07	Added sleep current, page 11 Updated RF Specification, page 13 Updated Additional information, page 18 Updated Sleep clock requirement, page 23
4	2008-09-10	Updated Power Consumption, page 11 Corrected typing error, page 19 Added min/max value for average output power, page14 Added frame-to-frame power fluctuation specification, page14
5	2009-3-14	Corrected typing error, page 11 Updated Reflow and Soldering, page 17 Updated Power on/off sequences, page 19
6	2009-09-10	Updated 1.8V Ripple spec, page 3 Updated Sleep current, page 11 Updated reference clock level, page 21 Updated Application reference design, page 22