

WIRELESS & SENSING

SX1501/SX1502/SX1503

4/8/16 Channel Low Voltage GPIO with NINT and NRESET

GENERAL DESCRIPTION

The SX1501, SX1502 and SX1503 are complete ultra low voltage General Purpose parallel Input/Output (GPIO) expanders ideal for low power handheld battery powered equipment. They allow easy serial expansion of I/O through a standard I²C interface. GPIO devices can provide additional control and monitoring when the microcontroller or chipset has insufficient I/O ports, or in systems where serial communication and control from a remote location is advantageous.

These devices can also act as a level shifter to connect a microcontroller running at one voltage level to a component running at a different voltage level. The core is operating as low as 1.2V while the I/O banks can operate between 1.2V and 5.5V independent of the core voltage and each other.

Each GPIO is programmable via 8-bit configuration registers. Data registers, direction registers, pull-up/pull-down registers, interrupt mask registers and interrupt registers allow the system master to program and configure 4 or 8 or 16-GPIOs using a standard 400kHz I²C interface.

The SX1501, SX1502 and SX1503 offer a unique fully programmable logic functions like a PLD to give more flexibility and reduce external logic gates used for standard applications.

The SX1501, SX1502 and SX1503 have the ability to generate mask-programmable interrupts based on falling/rising edge of any of its GPIO lines. A dedicated pin indicates to a host controller that a state change occurred in one or more of the GPIO lines.

The SX1501, SX1502 and SX1503 each come in a small QFN-UT-20/28 package. All devices are rated from -40°C to +85°C temperature range.

ORDERING INFORMATION

| Part Number | I/O Channels | Package |
|--------------------------|--------------|----------------|
| SX1501I087TRT | 4 | QFN-UT-20 |
| SX1502I087TRT | 8 | QFN-UT-20 |
| SX1503I091TRT | 16 | QFN-UT-28 |
| SX1502EVK ⁽¹⁾ | 8 | Evaluation Kit |

⁽¹⁾SX1502I087TRT based, unique evaluation kit for the three parts.

KEY PRODUCT FEATURES

- 4/8/16 channel of I/Os
 - True bi-directional style I/O
 - Programmable Pull-up/Pull-down
 - Push/Pull outputs
- 1.2V to 5.5V independent operating voltage for all supply rails (VDDM, VCC1, VCC2)
- 5.5V compatible I/Os, up to 24mA output sink (no total sink current limit)
- Fully programmable logic functions (PLD)
- 400kHz 2-wire I²C compatible slave interface
- Open drain active low interrupt output (NINT)
 - Bit maskable
 - Programmable edge sensitivity
- Power-On Reset and reset input (NRESET)
- Ultra low current consumption of typ. 1uA
- -40°C to +85°C operating temperature range
- Ultra-Thin 3x3mm QFN-UT-20 package (SX1501/SX1502)
- Ultra-Thin 4x4mm QFN-UT-28 package (SX1503)

TYPICAL APPLICATIONS

- Cell phones, PDAs, MP3 players
- Digital camera
- Portable multimedia player
- Notebooks
- GPS Units
- Industrial, ATE
- Any battery powered equipment

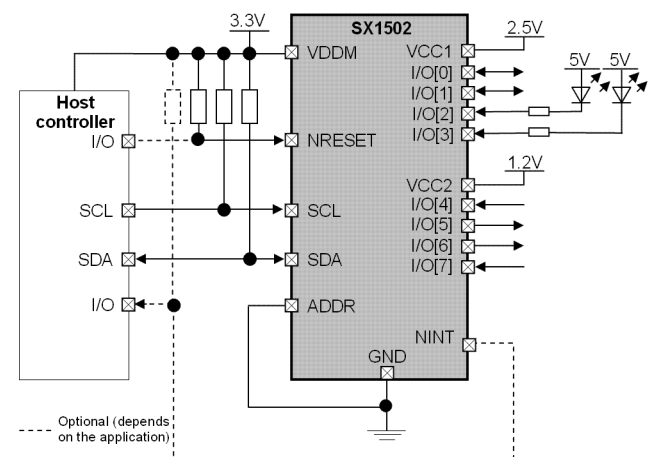


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1 PIN DESCRIPTION

1.1 SX1501 4-channel GPIO

| Pin | Symbol | Type | Description |
|-----|--------|--------------------|--|
| 1 | NRESET | DIO | Active low reset |
| 2 | SDA | DIO | I ² C serial data line |
| 3 | NC1 | - | Leave open, not connected |
| 4 | SCL | DI | I ² C serial clock line |
| 5 | I/O[0] | DIO ^(*) | I/O[0], at power-on configured as an input |
| 6 | I/O[1] | DIO ^(*) | I/O[1], at power-on configured as an input |
| 7 | VCC1 | P | I/O supply voltage |
| 8 | GND | P | Ground Pin |
| 9 | I/O[2] | DIO ^(*) | I/O[2], at power-on configured as an input High sink I/O. |
| 10 | I/O[3] | DIO ^(*) | I/O[3], at power-on configured as an input High sink I/O. |
| 11 | NINT | DO | Active low interrupt output |
| 12 | ADDR | DI | Address input, connect to VDDM or GND |
| 13 | NC2 | - | Leave open, not connected |
| 14 | VDDM | P | Main supply voltage |
| 15 | NC3 | - | Leave open, not connected |
| 16 | NC4 | - | Leave open, not connected |
| 17 | NC7 | - | Connect to VCC1 |
| 18 | GND | P | Ground Pin |
| 19 | NC5 | - | Leave open, not connected |
| 20 | NC6 | - | Leave open, not connected |

A: Analog
D: Digital
I: Input
O: Output
P: Power

(*1) This pin is programmable through the I²C interface

Table 1 – SX1501 Pin Description

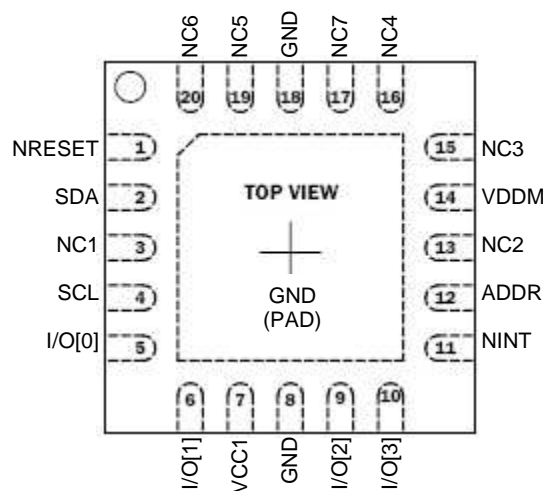


Figure 1 – SX1501 QFN-UT-20 Pinout

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1.2 SX1502 8-channel GPIO

| Pin | Symbol | Type | Description |
|-----|--------|---------|--|
| 1 | NRESET | DIO | Active low reset |
| 2 | SDA | DIO | I ² C serial data line |
| 3 | NC1 | - | Leave open, not connected |
| 4 | SCL | DI | I ² C serial clock line |
| 5 | I/O[0] | DIO (*) | I/O[0], at power-on configured as an input |
| 6 | I/O[1] | DIO (*) | I/O[1], at power-on configured as an input |
| 7 | VCC1 | P | Supply voltage for Bank A I/O[0-3] |
| 8 | GND | P | Ground Pin |
| 9 | I/O[2] | DIO (*) | I/O[2], at power-on configured as an input High sink I/O. |
| 10 | I/O[3] | DIO (*) | I/O[3], at power-on configured as an input High sink I/O. |
| 11 | NINT | DO | Active low interrupt output |
| 12 | ADDR | DI | Address input, connect to VDDM or GND |
| 13 | NC2 | - | Leave open, not connected |
| 14 | VDDM | P | Main supply voltage |
| 15 | I/O[4] | DIO (*) | I/O[4], at power-on configured as an input |
| 16 | I/O[5] | DIO (*) | I/O[5], at power-on configured as an input |
| 17 | VCC2 | P | Supply voltage for Bank B I/O[4-7] |
| 18 | GND | P | Ground Pin |
| 19 | I/O[6] | DIO (*) | I/O[6], at power-on configured as an input |
| 20 | I/O[7] | DIO (*) | I/O[7], at power-on configured as an input |

A: Analog
D: Digital
I: Input
O: Output
P: Power

(*1) This pin is programmable through the I²C interface

Table 2 – SX1502 Pin Description

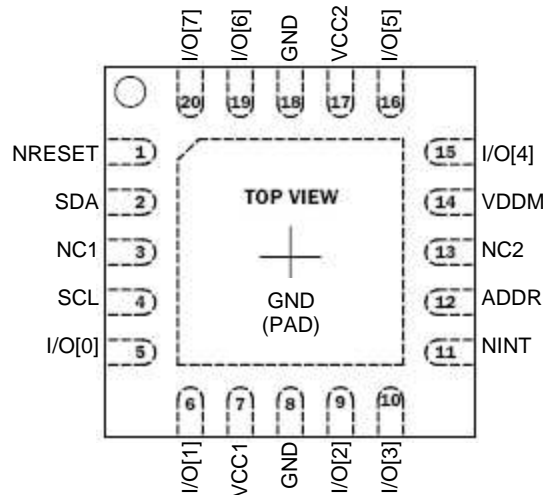


Figure 2 – SX1502 QFN-UT-20 Pinout

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1.3 SX1503 16-channel GPIO

| Pin | Symbol | Type | Description |
|-----|---------|---------|---|
| 1 | GND | P | Ground Pin |
| 2 | I/O[2] | DIO (*) | I/O[2], at power-on configured as an input |
| 3 | I/O[3] | DIO (*) | I/O[3], at power-on configured as an input |
| 4 | VCC1 | P | I/O supply voltage for Bank A I/O[0-7] |
| 5 | I/O[4] | DIO (*) | I/O[4], at power-on configured as an input |
| 6 | I/O[5] | DIO (*) | I/O[5], at power-on configured as an input |
| 7 | GND | P | Ground Pin |
| 8 | I/O[6] | DIO (*) | I/O[6], at power-on configured as an input High sink I/O. |
| 9 | I/O[7] | DIO (*) | I/O[7], at power-on configured as an input High sink I/O. |
| 10 | NINT | DO | Active low interrupt output |
| 11 | NC | - | Leave open, not connected |
| 12 | VDDM | P | Main supply voltage |
| 13 | I/O[8] | DIO (*) | I/O[8], at power-on configured as an input |
| 14 | I/O[9] | DIO (*) | I/O[9], at power-on configured as an input |
| 15 | GND | P | Ground Pin |
| 16 | I/O[10] | DIO (*) | I/O[10], at power-on configured as an input |
| 17 | I/O[11] | DIO (*) | I/O[11], at power-on configured as an input |
| 18 | VCC2 | P | I/O supply voltage for Bank B I/O[8-15] |
| 19 | I/O[12] | DIO (*) | I/O[12], at power-on configured as an input |
| 20 | I/O[13] | DIO (*) | I/O[13], at power-on configured as an input |
| 21 | GND | P | Ground Pin |
| 22 | I/O[14] | DIO (*) | I/O[14], at power-on configured as an input High sink I/O. |
| 23 | I/O[15] | DIO (*) | I/O[15], at power-on configured as an input High sink I/O. |
| 24 | NRESET | DIO | Active low reset |
| 25 | SDA | DIO | I ² C serial data line |
| 26 | SCL | DI | I ² C serial clock line |
| 27 | I/O[0] | DIO (*) | I/O[0], at power-on configured as an input |
| 28 | I/O[1] | DIO (*) | I/O[1], at power-on configured as an input |

A: Analog
D: Digital
I: Input
O: Output
P: Power

(*) This pin is programmable through the I²C interface

Table 3 – SX1503 Pin Description

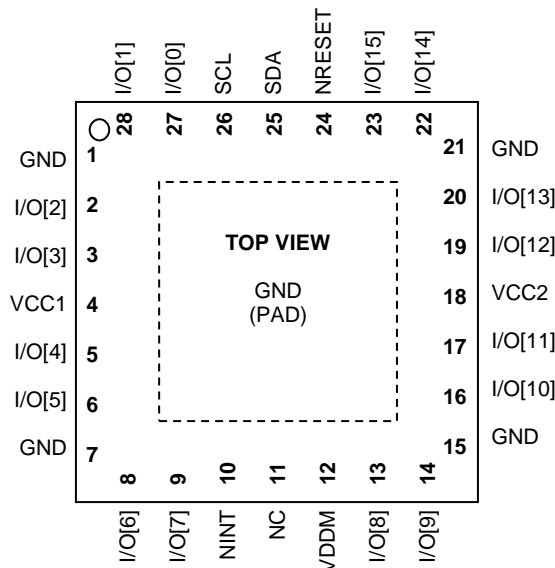


Figure 3 – SX1503 QFN-UT-28 Pinout

WIRELESS & SENSING
2 ELECTRICAL CHARACTERISTICS
2.1 Absolute Maximum Ratings

Stress above the limits listed in the following table may cause permanent failure. Exposure to absolute ratings for extended time periods may affect device reliability. The limiting values are in accordance with the Absolute Maximum Rating System (IEC 134). All voltages are referenced to ground (GND).

| Symbol | Description | Min | Max | Unit |
|-----------------------|---|--------|------|------|
| VDDM _{max} | Main supply voltage | - 0.4 | 6.0 | V |
| VCC1,2 _{max} | I/O banks supply voltage | - 0.4 | 6.0 | V |
| V _{ESD HBM} | Electrostatic handling HBM model ⁽¹⁾ | - | 1500 | V |
| V _{ESD CDM} | Electrostatic handling CDM model | - | 300 | V |
| V _{ESD MM} | Electrostatic handling MM model | - | 200 | V |
| T _A | Operating Ambient Temperature Range | -40 | +85 | °C |
| T _C | Junction Temperature Range | -40 | +125 | °C |
| T _{STG} | Storage Temperature Range | -55 | +150 | °C |
| I _{lat} | Latchup-free input pin current ⁽²⁾ | +/-100 | - | mA |

(1) Tested according to JESD22-A114A

(2) Static latch-up values are valid at maximum temperature according to JEDEC 78 specification

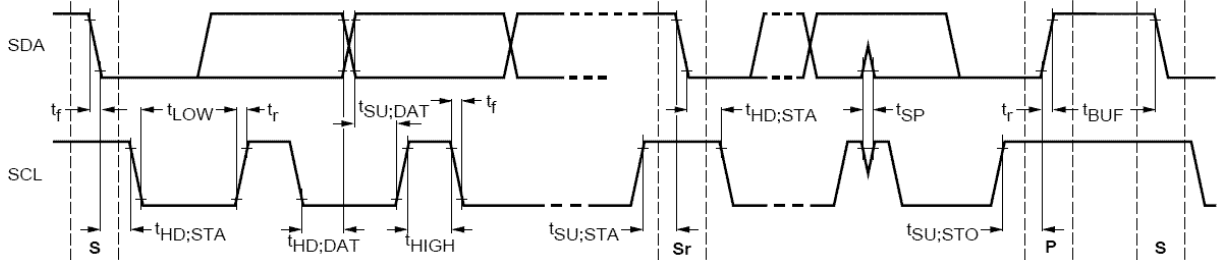
Table 4 - Absolute Maximum Ratings

2.2 Electrical Specifications

Table below applies to default registers values (Boost Mode Off), unless otherwise specified. Typical values are given for T_A = +25°C, VDDM=VCC1=VCC2=3.3V.

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---------------------------|--|---------------------------------|-----------------|----------------|--------------------|------|
| Supply | | | | | | |
| VDDM | Main supply voltage | - | 1.2 | - | 5.5 | V |
| VCC1,2 | I/O banks supply voltage | - | 1.2 | - | 5.5 | V |
| IDDM | Main supply current (I ² C inactive) | - | - | 1 | 5 | µA |
| ICC1,2 | I/O banks supply current ⁽¹⁾ | VCC1,2 ≥ 2V | - | 1 | 2 | µA |
| | | VCC1,2 < 2V | - | 0.5 | 1 | |
| I/Os set as Input | | | | | | |
| VIH | High level input voltage | - | 0.7* VCC1,2 | - | VCC1,2 +0.3 | V |
| VIL | Low level input voltage | - | -0.4 | - | 0.3* VCC1,2 | V |
| VHYS | Hysteresis of Schmitt trigger | - | - | 0.1* VCC1,2 | - | V |
| ILEAK | Input leakage current | Assuming no active pull-up/down | -1.5 | - | 1.5 | µA |
| CI | Input capacitance | - | - | - | 10 | pF |
| I/Os set as Output | | | | | | |
| VOH | High level output voltage | - | VCC1,2 - 0.3 | - | VCC1,2 | V |
| VOL | Low level output voltage | - | -0.4 | - | 0.3 | V |
| IOH | High level output source current | VCC1,2 ≥ 2V | - | - | 8 | mA |
| | | VCC1,2 < 2V | - | - | 0.3 ⁽²⁾ | |
| IOL | Low level output sink current for the high sink I/Os | VCC1,2 ≥ 2V | - | - | 24 | mA |
| | | VCC1,2 < 2V | - | - | 6 ⁽²⁾ | |
| IOL | Low level output sink current for the other I/Os. | VCC1,2 ≥ 2V | - | - | 12 | mA |
| | | VCC1,2 < 2V | - | - | 6 | |
| t _{PV} | Output data valid timing | Cf. Figure 9 | - | - | 1.5 | µs |
| NINT (Output) | | | | | | |
| VOL | Low level output voltage | - | - | - | 0.3 | V |
| IOL _M | Low level output sink current | VDDM ≥ 2V | - | - | 12 | mA |
| | | VDDM < 2V | - | - | 6 | |
| t _{IV} | Interrupt valid timing | From input data change | - | - | 1 | µs |

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| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|--|--|----------------------------------|-------------------------------------|--------------|--------------------|---------|
| t_{IR} | Interrupt reset timing | From RegInterruptSource clearing | - | - | 2 | μs |
| NRESET (Input/Output) | | | | | | |
| VOL | Low level output voltage | - | - | - | 0.3 | V |
| IOL _M | Low level output sink current | VDDM \geq 2V | - | - | 12 | mA |
| | | VDDM < 2V | - | - | 6 | |
| VIH _{MR} | High level input voltage | - | 0.7* VDDM | - | 5.5 | V |
| VIL _M | Low level input voltage | - | -0.4 | - | 0.3* VDDM | V |
| VHYS _M | Hysteresis of Schmitt trigger | - | - | 0.1* VDDM | - | V |
| ILEAK | Input leakage current | - | -1.5 | - | 1.5 | μA |
| CI | Input capacitance | - | - | - | 10 | pF |
| VPOR | Power-On-Reset voltage | Cf. Figure 7 | 0.7 | - | 0.9 | V |
| VDROPH | High brown-out voltage | Cf. Figure 7 | - | VDDM-1 | - | V |
| VDROPL | Low brown-out voltage | Cf. Figure 7 | - | 0.2 | - | V |
| t_{RESET} | Reset time | Cf. Figure 7 | - | - | 7 | ms |
| t_{PULSE} | Reset pulse from host uC | Cf. Figure 7 | 300 | - | - | ns |
| ADDR (Input) | | | | | | |
| VIH _{MA} | High level input voltage | - | 0.7* VDDM | - | VDDM +0.3 | V |
| VIL _M | Low level input voltage | - | -0.4 | - | 0.3* VDDM | V |
| VHYS _M | Hysteresis of Schmitt trigger | - | - | 0.1* VDDM | - | V |
| ILEAK | Input leakage current | - | -1.5 | - | 1.5 | μA |
| CI | Input capacitance | - | - | - | 10 | pF |
| SCL (Input) and SDA (Input/Output) ⁽³⁾ | | | | | | |
| Interface complies with slave F/S mode I ² C interface as described by Philips I ² C specification version 2.1 dated January, 2000. Please refer to that document for more detailed I ² C specifications. | | | | | | |
|  | | | | | | |
| VOL | Low level output voltage | - | - | - | 0.3 | V |
| IOL _M | Low level output sink current | VDDM \geq 2V | - | - | 12 | mA |
| | | VDDM < 2V | - | - | 6 | |
| VIH _{MR} | High level input voltage | - | 0.7* VDDM | - | 5.5 | V |
| VIL _M | Low level input voltage | - | -0.4 | - | 0.3* VDDM | V |
| f_{SCL} | SCL clock frequency | - | 0 | - | 400 | kHz |
| $t_{HD:STA}$ | Hold time (repeated) START condition | - | 0.6 | - | - | μs |
| t_{LOW} | LOW period of the SCL clock | - | 1.3 | - | - | μs |
| t_{HIGH} | HIGH period of the SCL clock | VDDM \geq 1.3V | 0.6 | - | - | μs |
| | | VDDM < 1.3V | 1 | - | - | |
| $t_{SU:STA}$ | Set-up time for a repeated START condition | - | 0.6 | - | - | μs |
| $t_{HD:DAT}$ | Data hold time | - | 0 ⁽⁴⁾ | - | 0.9 ⁽⁵⁾ | μs |
| $t_{SU:DAT}$ | Data set-up time | - | 100 ⁽⁶⁾ | - | - | |
| t_r | Rise time of both SDA and SCL signals | - | 20+0.1C _b ⁽⁷⁾ | - | 300 | ns |

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| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|----------------------|---|-------------------------------|-------------------|-----|-----|------------|
| t_f | Fall time of both SDA and SCL signals | - | $20+0.1C_b^{(7)}$ | - | 300 | ns |
| $t_{SU;STO}$ | Set-up time for STOP condition | - | 0.6 | - | - | μ s |
| t_{BUF} | Bus free time between a STOP and START condition | - | 1.3 | - | - | μ s |
| C_b | Capacitive load for each bus line | - | - | - | 400 | pF |
| V_{nL} | Noise margin at the LOW level for each connected device (including hysteresis) | - | $0.1*V_{DDM}$ | - | - | V |
| V_{nH} | Noise margin at the HIGH level for each connected device (including hysteresis) | - | $0.2*V_{DDM}$ | - | - | V |
| Miscellaneous | | | | | | |
| RPULL | Programmable pull-up/down resistors for IO[0-7] | - | - | 60 | - | k Ω |
| t_{PLD} | PLD propagation delay | $V_{CC1,2} \& V_{DDM} = 5V$ | - | - | 25 | ns |
| | | $V_{CC1,2} \& V_{DDM} = 1.2V$ | - | - | 500 | |

(1) Assuming no load connected to outputs and inputs fixed to VCC1,2 or GND.

(2) Can be increased in RegAdvanced register. Please refer to §2.2.1 for more details.

(3) All values referred to $V_{IHMR\ min}$ and $V_{ILM\ max}$ levels.

(4) A device must internally provide a hold time of at least 300ns for the SDA signal (referred to $V_{IHMR\ min}$) to bridge the undefined region of the falling edge of SCL.

(5) The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

(6) A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal.

If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\ max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C-bus specification) before the SCL line is released.

(7) C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times are allowed.

Table 5 – Electrical Specifications

2.2.1 Increasing I/O Sink and Source Current Capabilities (Boost Mode)

When bit 1 of RegAdvanced register is set, max IOH and IOL spec **when VCC1,2 is below VBOOST** can be increased together with IDDM and ICC1,2 figures as described below.

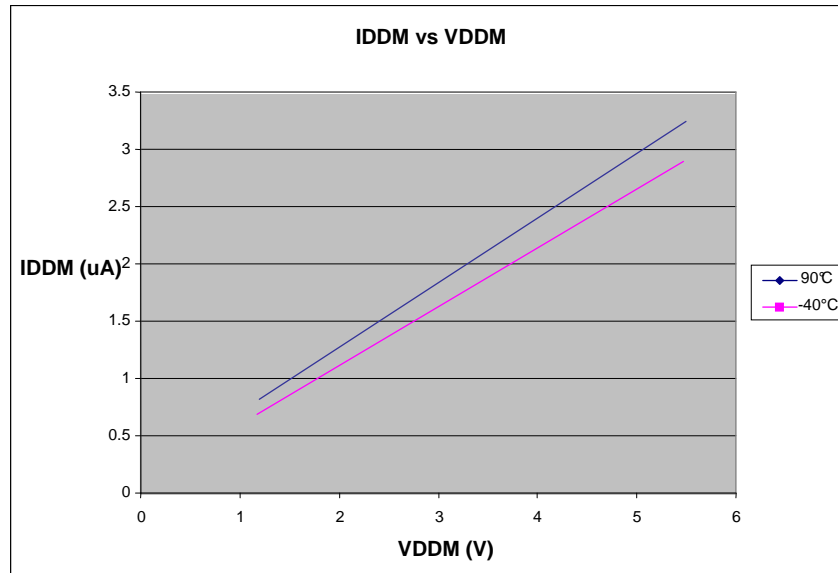
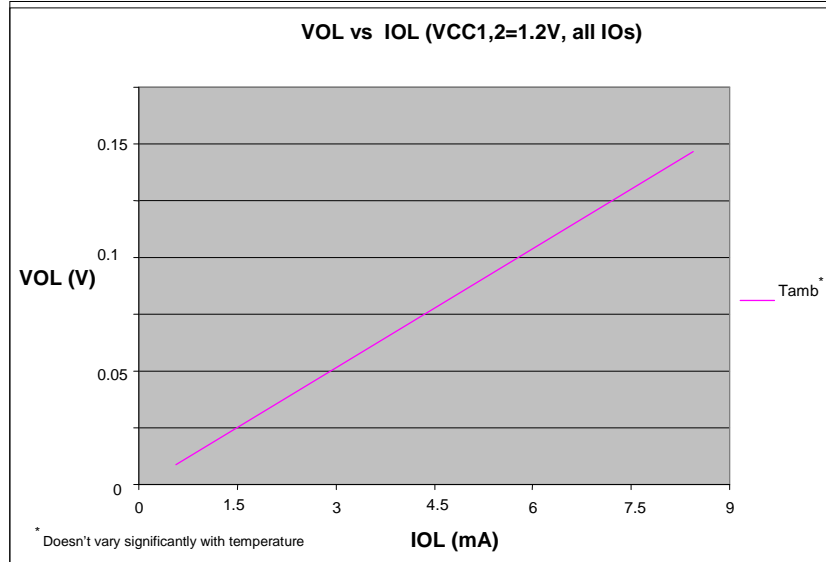
| Symbol | Description | Conditions | Min | Typ | Max | Unit | |
|---------------------------|--|---------------------------------------|------------------|-----|-----|---------|---------|
| Supply | | | | | | | |
| VBOOST | Low voltage boost threshold | - | 2.0 | 2.6 | - | V | |
| IDDM | Main supply current (I ² C inactive) | $V_{DDM} = 5.5V$ ($V_{CC1,2} < 2V$) | - | 150 | 250 | μ A | |
| | | $V_{DDM} = 1.2V$ ($V_{CC1,2} < 2V$) | - | 25 | 50 | μ A | |
| ICC1 | I/O bank A supply current | SX1501/2 | $V_{CC1} = 2V$ | - | 250 | 550 | μ A |
| | | | $V_{CC1} = 1.2V$ | - | 100 | 200 | |
| | | SX1503 | $V_{CC1} = 2V$ | - | 250 | 550 | |
| | | | $V_{CC1} = 1.2V$ | - | 100 | 200 | |
| ICC2 | I/O bank B supply current | SX1502 | $V_{CC2} = 2V$ | - | 150 | 250 | μ A |
| | | | $V_{CC2} = 1.2V$ | - | 50 | 150 | |
| | | SX1503 | $V_{CC2} = 2V$ | - | 250 | 450 | |
| | | | $V_{CC2} = 1.2V$ | - | 100 | 200 | |
| I/Os set as Output | | | | | | | |
| IOH | High level output source current for all I/Os | $V_{CC1,2} \geq V_{BOOST}$ | - | - | 8 | mA | |
| | | $V_{CC1,2} < V_{BOOST}$ | - | - | 4 | | |
| IOL | Low level output sink current for the high sink I/Os | $V_{CC1,2} \geq V_{BOOST}$ | - | - | 24 | mA | |
| | | $V_{CC1,2} < V_{BOOST}$ | - | - | 12 | | |
| | Low level output sink current for the other I/Os | $V_{CC1,2} \geq V_{BOOST}$ | - | - | 12 | mA | |
| | | $V_{CC1,2} < V_{BOOST}$ | - | - | 6 | | |
| NINT, NRESET | | | | | | | |
| IOL _M | Low level output sink current for NINT, NRESET | $V_{DDM} \geq V_{BOOST}$ | - | - | 12 | mA | |
| | | $V_{DDM} < V_{BOOST}$ | - | - | 6 | | |

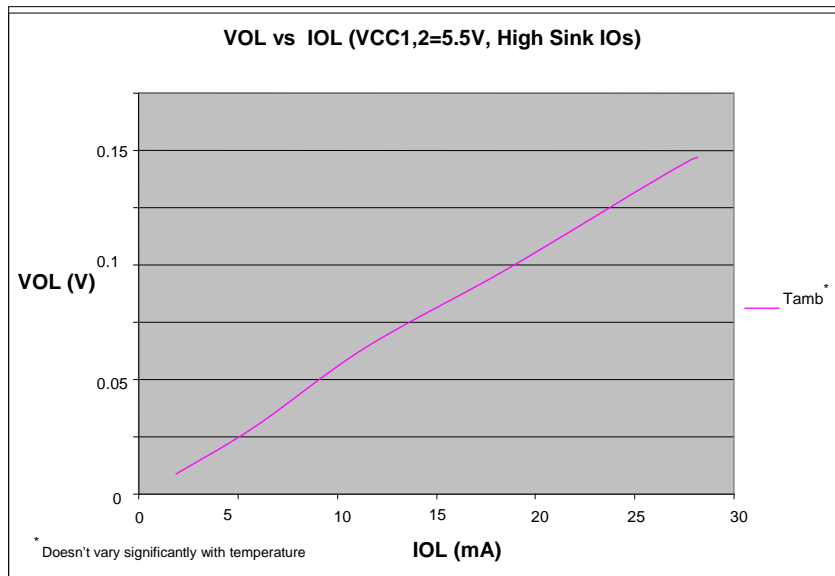
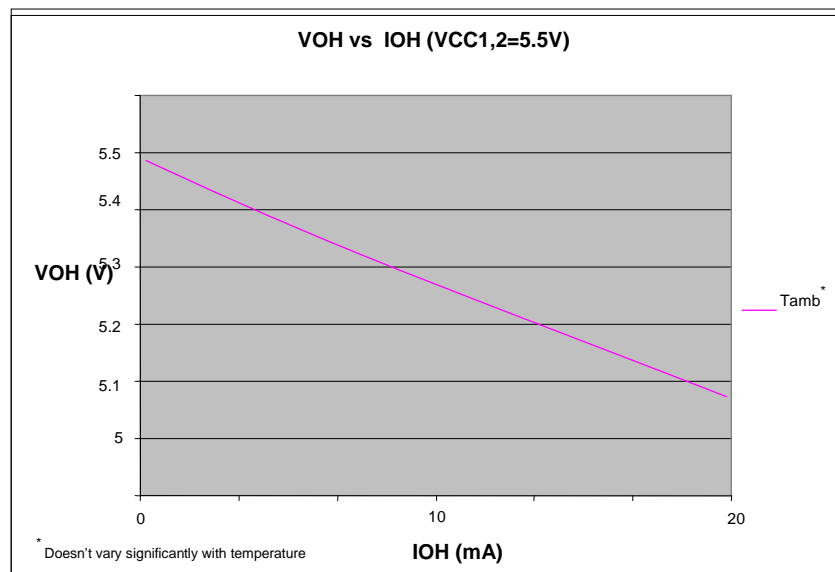
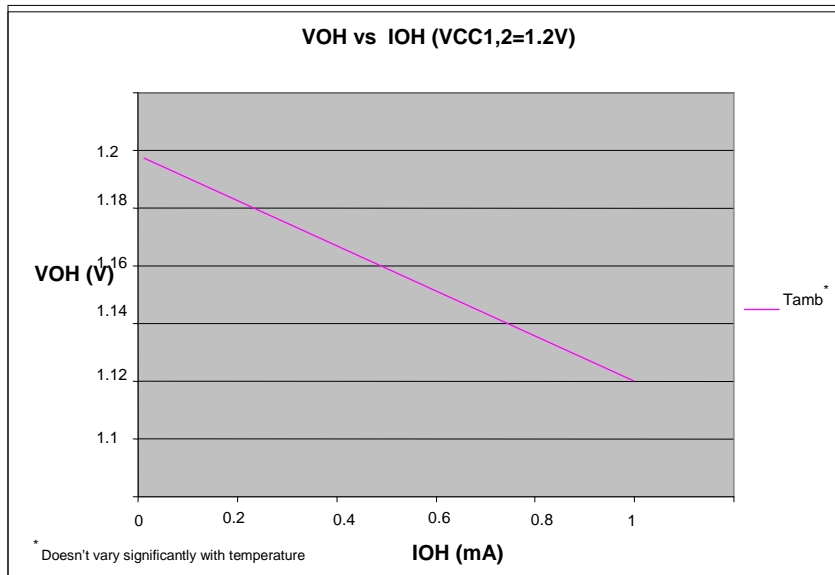
Table 6 – Electrical Specifications in Boost Mode

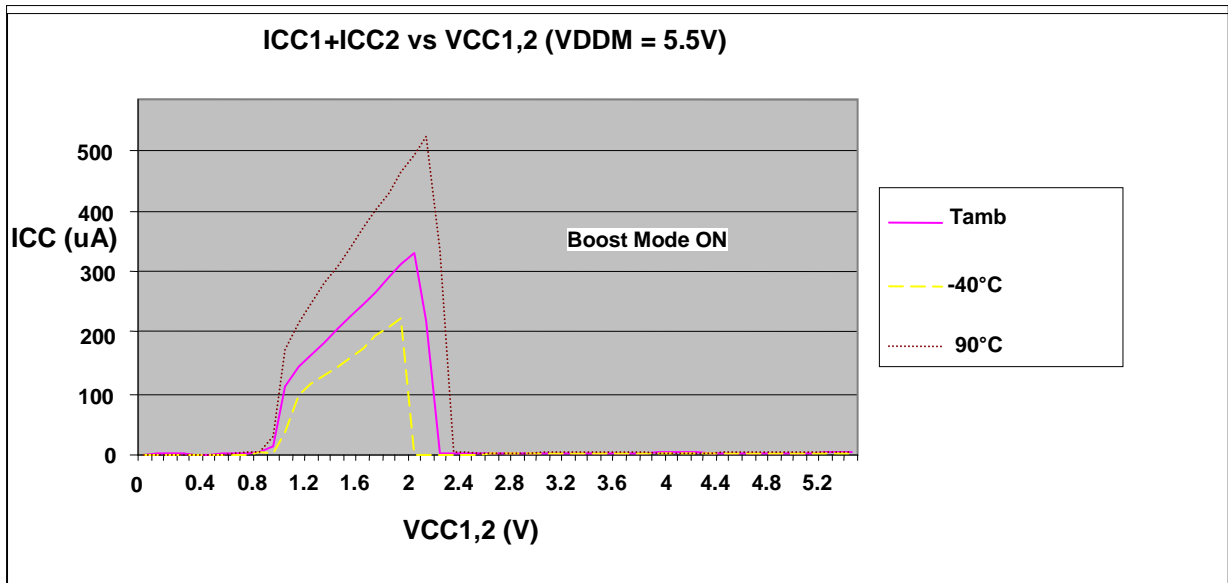
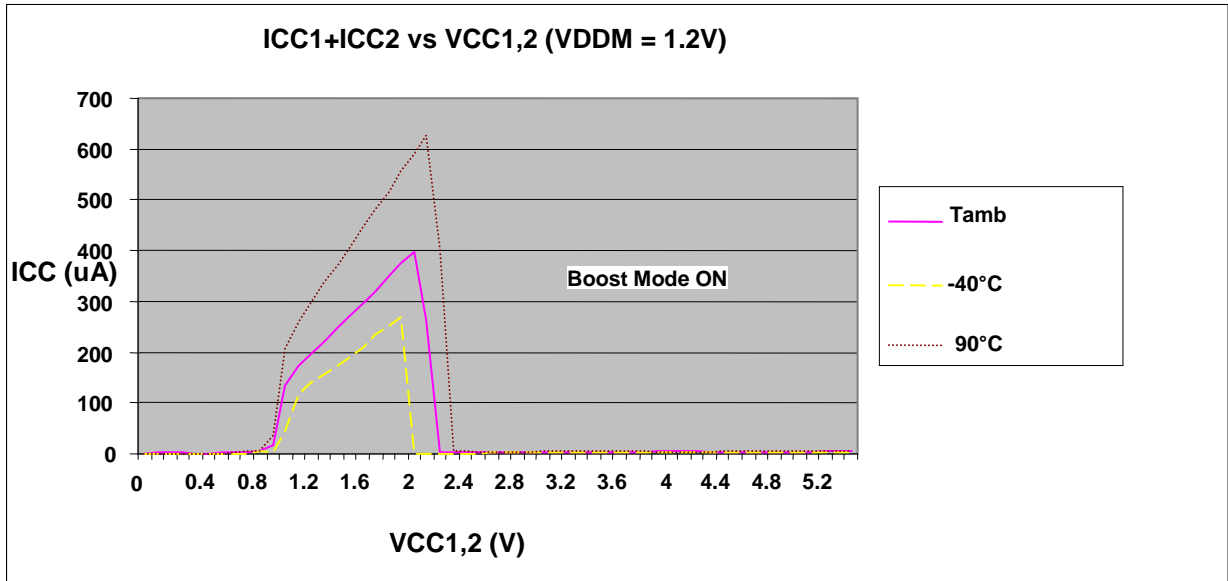
Important: RegAdvanced register doesn't affect any spec when VCC1 and VCC2 are above VBOOST.

WIRELESS & SENSING
3 TYPICAL OPERATING CHARACTERISTICS

Figures below apply to default registers values (Boost Mode Off), T_{amb} , unless otherwise specified.

3.1 IDDM vs. VDDM

3.2 VOL vs. IOL


WIRELESS & SENSING

3.3 VOH vs. IOH


WIRELESS & SENSING
3.4 ICC1+ICC2 vs. VCC1,2 when Boost Mode is ON


WIRELESS & SENSING

4 BLOCK DETAILED DESCRIPTION

4.1 SX1501 4-channel GPIO

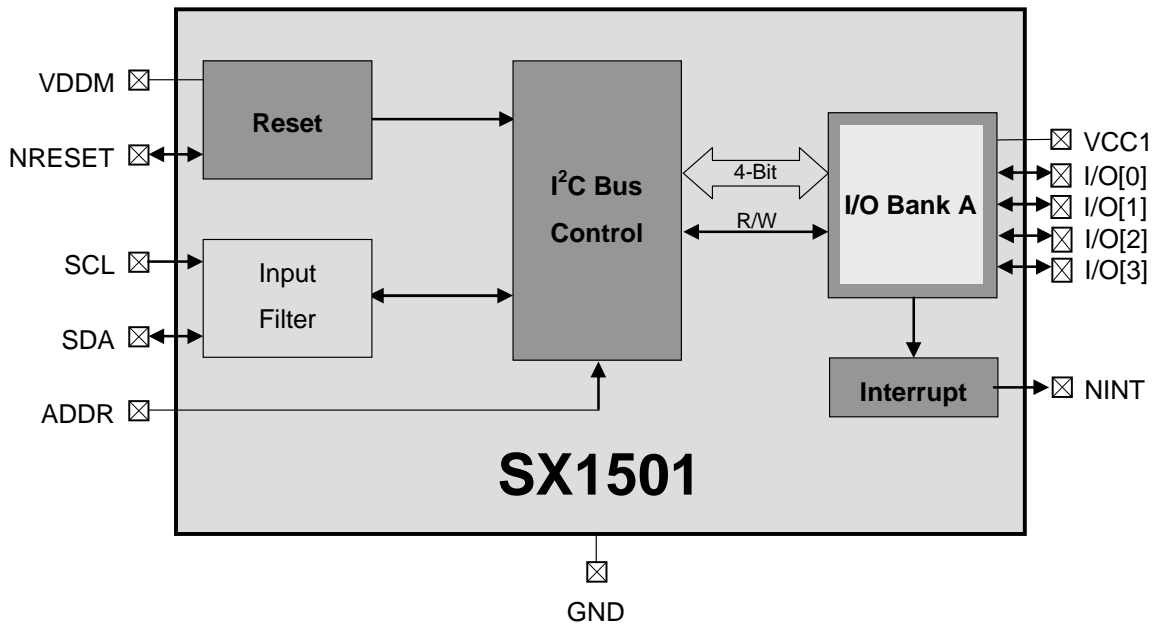


Figure 4 – 4-channel Low Voltage GPIO

4.2 SX1502 8-channel GPIO

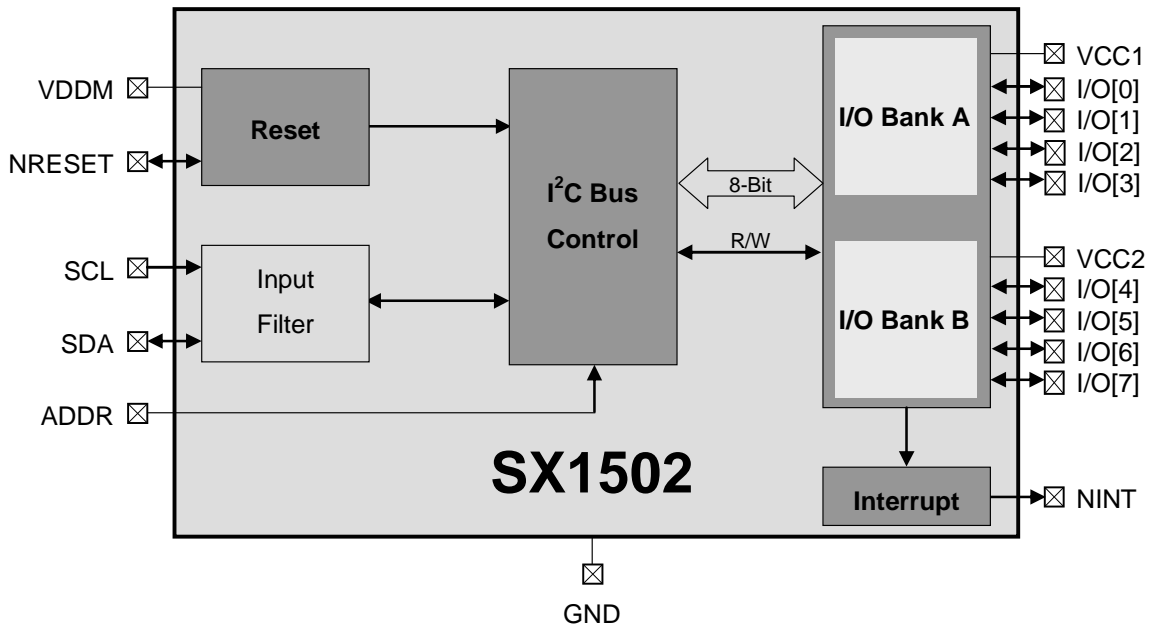


Figure 5 – 8-channel Low Voltage GPIO

WIRELESS & SENSING

4.3 SX1503 16-channel GPIO

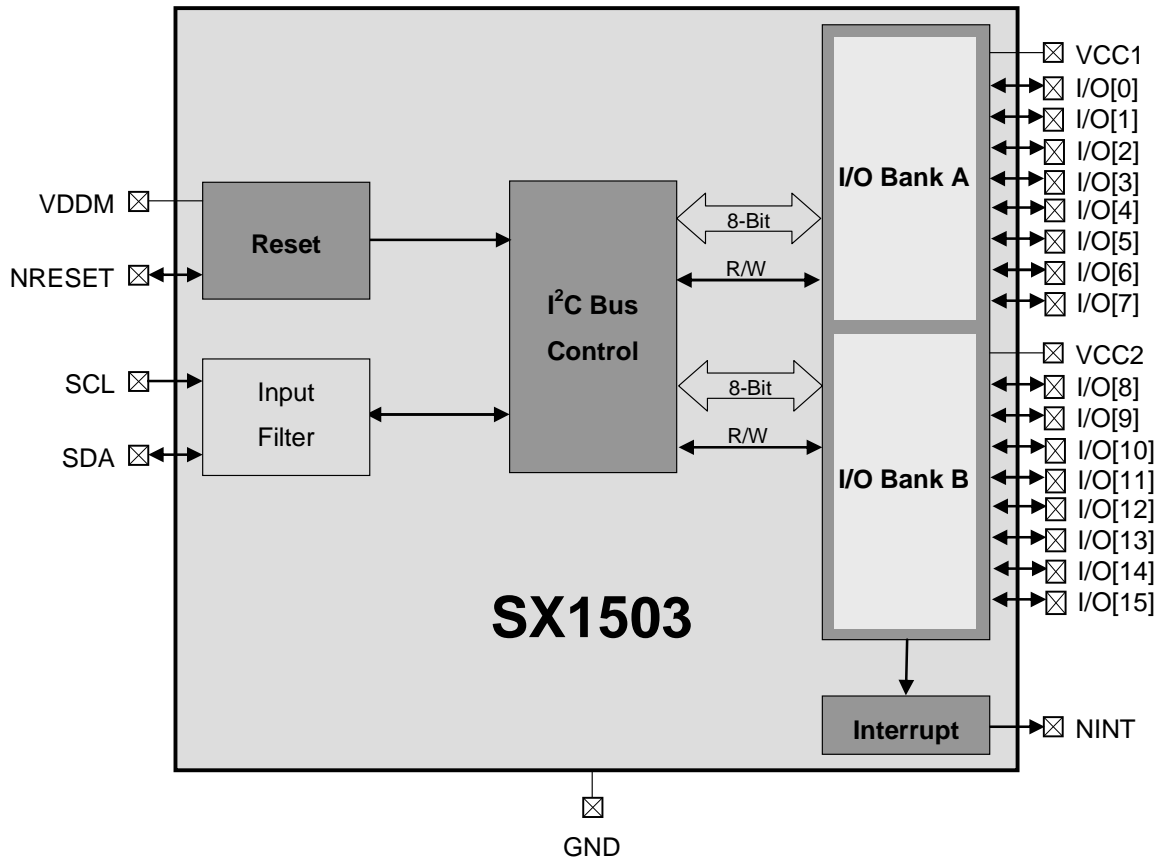


Figure 6 – 16-channel Low Voltage GPIO

4.4 Reset (NRESET)

The SX1501, SX1502 and SX1503 generate their own power on reset signal after a power supply is connected to the VDDM pin. The reset signal is made available for the user at the pin NRESET. The rising edge of the NRESET indicates that the startup sequence of the SX1501, SX1502 or SX1503 has finished. NRESET must be connected to VDDM (or greater) either directly, or via a resistor.

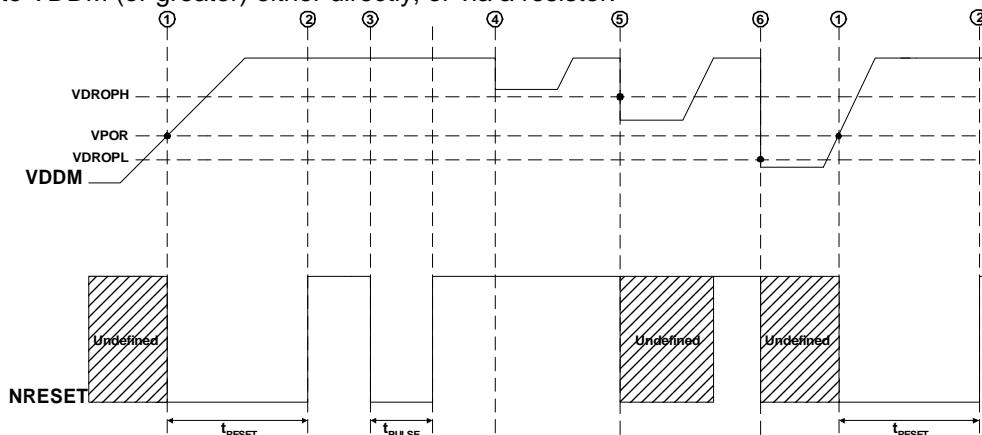


Figure 7 – Power-On / Brown-out Reset Conditions

1. Device behavior is undefined until VDDM rises above VPOR, at which point NRESET is driven to GND by the SX1501, SX1502 or SX1503.
2. After t_{RESET} , NRESET is released (high-impedance) by the SX1501, SX1502 or SX1503 to allow it to be pulled high by an external resistor.
3. In operation, the SX1501, SX1502 and SX1503 may be reset at anytime by an external device driving NRESET low during t_{PULSE} . Chip can be accessed normally again after NRESET rising edge.

WIRELESS & SENSING

4. During a brown-out event, if VDDM drops above VDROPH a reset will not occur.
5. During a brown-out event, if VDDM drops between VDROPH and VDROPL a reset may occur.
6. During a brown-out event, if VDDM drops below VDROPL a reset will occur next time VPOR is crossed.

Please note that a brown-out event is defined as a transient event on VDDM. If VDDM is attached to a battery, then the gradual decay of the battery voltage will not be interpreted as a brown-out event.

Please also note that a sharp rise in VDDM (> 1V/us) may induce a circuit reset.

4.5 2-Wire Interface (I²C)

The SX1501, SX1502 and SX1503 2-wire interface (I²C compliant) operates only in slave mode. In this configuration, the device has one or two device addresses defined by ADDR pin.

| Device | ADDR Pin | I ² C Address | Description |
|-----------------|----------|--------------------------|--|
| SX1501 & SX1502 | 0 | 0x20 (0100000) | First address of the 2-wire interface |
| | 1 | 0x21 (0100001) | Second address of the 2-wire interface |
| SX1503 | | 0x20 (0100000) | Fixed address of the 2-wire interface |

Table 7 - 2-Wire Interface Address

2 lines are used to exchange data between an external master host and the slave device:

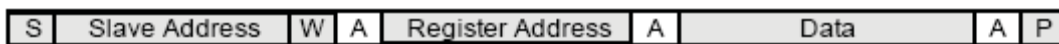
- **SCL** : Serial CLock
- **SDA** : Serial DAta

The SX1501, SX1502 and SX1503 are read-write slave-mode I²C devices and comply with the Philips I²C standard Version 2.1 dated January, 2000. The SX1501, SX1502 and SX1503 have respectively 12, 16, and 31 user-accessible internal 8-bit registers. The I²C interface has been designed for program flexibility, in that once the slave address has been sent to the SX1501, SX1502 or SX1503 enabling it to be a slave transmitter/receiver, any register can be written or read independently of each other. While there is no auto increment/decrement capability in the SX1501 and SX1502 I²C logic, a tight software loop can be designed to access the next register independent of which register you begin accessing. SX1503 implements auto increment capability. The start and stop commands frame the data-packet and the repeat start condition is allowed if necessary.

Seven bit addressing is used and ten bit addressing is not allowed. Any general call address will be ignored by the SX1501, SX1502 and SX1503. The SX1501, SX1502 and SX1503 are not CBUS compatible and can operate in standard mode (100kbit/s) or fast mode (400kbit/s).

4.5.1 WRITE

The simplest format for an I²C write is given below. After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The I²C then acknowledges that it is being addressed, and the master responds with an 8 bit data byte consisting of the register address. The slave acknowledges and the master sends the appropriate 8 bit data byte. Once again the slave acknowledges and the master terminates the transfer with the stop condition [P].



Master operations

SX1501, SX1502 or SX1503 operations (Slave)

S: Start Condition

W: Write = '0'

A: Acknowledge (sent by slave)

P: Stop condition

Slave Address: 7 bit

Register Address: 8 bit

Data: 8 bit

Figure 8 - 2-Wire Serial Interface, Write Register Operation

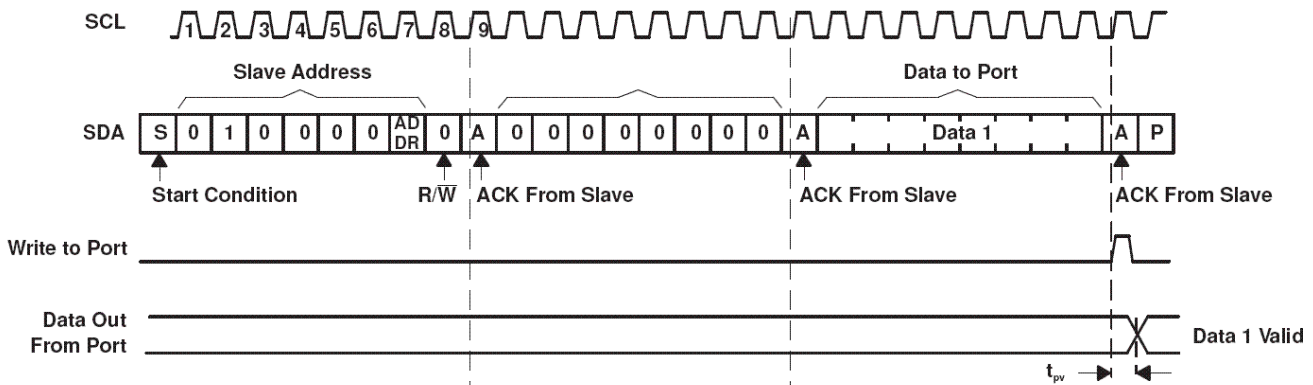
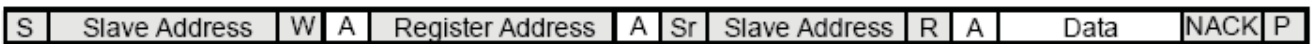
WIRELESS & SENSING


Figure 9 – Write RegData Register

Please note that SX1503 implements register address auto-increment i.e. after the Data ACK from Slave the master can write further bytes and the interface will handle the register address increment automatically. Finally the master terminates the transfer normally the stop condition [P].

4.5.2 READ

After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The I²C then acknowledges that it is being addressed, and the master responds with an 8 bit data byte consisting of the register address. The slave acknowledges and the master sends the repeated start condition [Sr]. Once again, the slave address is sent, followed by an eighth bit indicating a read. The slave responds with an acknowledge and the previously addressed 8 bit data byte; the master then sends a non-acknowledge (NACK). Finally, the master terminates the transfer with the stop condition [P].



- Master operations
- SX1501, SX1502 or SX1503 operations (Slave)

S: Start Condition
W: Write = '0'
R: Read = '1'
A: Acknowledge (sent by slave)
NACK: Non-Acknowledge (sent by master)
Sr: Repeated Start Condition
P: Stop condition

Slave Address: 7 bit
Register Address: 8 bit
Data: 8 bit

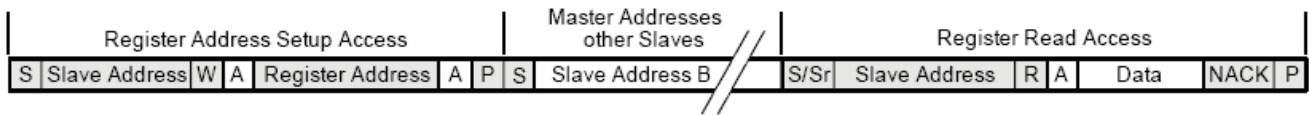
Figure 10 - 2-Wire Serial Interface, Read Register Operation

Please note that SX1503 implements register address auto-increment i.e. after the Data byte from Slave the master can acknowledge (ACK) to indicate that it wants to read the next byte and the interface will handle the register address increment automatically. Finally the master terminates the transfer normally with a NACK followed by the stop condition [P].

4.5.3 READ - STOP separated format (SX1501 and SX1502 only)

When operating SX1501 or SX1502, stop-separated reads can also be used. This format allows a master to set up the register address pointer for a read and return to that slave at a later time to read the data. In this format the slave address followed by a write command are sent after a start [S] condition. The slave then acknowledges it is being addressed, and the master responds with the 8-bit register address. The master sends a Stop or Restart condition and may then address another slave. After performing other tasks, the master can send a start or restart condition to the slave with a read command. The slave acknowledges this request and returns the data from the register location that had previously been set up.

WIRELESS & SENSING



- Master operations
- SX1501, SX1502 or SX1503 operations (Slave)

S: Start Condition
W: Write = '0'
R: Read = '1'
A: Acknowledge (sent by slave)
NACK: Non-Acknowledge (sent by master)
Sr: Repeated Start Condition
P: Stop condition

Slave Address: 7 bit
Register Address: 8 bit
Data: 8 bit

Figure 11 - 2-Wire Serial Interface, Read – Stop Separated Mode Operation

4.6 Interrupt (NINT)

At start-up, the transition detection logic is reset, and NINT is released to a high-impedance state. The interrupt mask register is set to 0xFF, disabling the interrupt output for transitions on all I/O ports. The transition flags are cleared to indicate no data changes.

An interrupt NINT can be generated on any programmed combination of I/Os rising and/or falling edges through the RegInterruptMask and RegSense registers. If needed, the I/Os which triggered the interrupt can then be identified by reading RegInterruptSource register.

When NINT is low (i.e. interrupt occurred), it can be reset back high (i.e. cleared) by writing 0xFF in RegInterruptSource (this will also clear corresponding bits in RegEventStatus register). SX1503 also allows the interrupt to be cleared automatically when reading RegData register (Cf. RegAdvanced)

Example: We want to detect rising edge of I/O[1] on SX1502 (NINT will go low).

1. We enable interrupt on I/O[1] in RegInterruptMask
⇒ RegInterruptMask = "XXXXXX0X"

2. We set edge sense for I/O[1] in RegSense
⇒ RegSenseLow = "XXXX01XX"

4.7 Programmable Logic Functions (PLD)

The SX1501, SX1502 and SX1503 offer a unique fully programmable logic functions like a PLD to give more flexibility and reduce external logic gates used for standard applications. Since the whole truth table is fully programmable, the SX1501, SX1502, and SX1503 can implement combinatory functions ranging from the basic AND/OR gates to the most complicated ones with up to four 3-to-1 PLDs or two 3-to-2 PLDs which can also be externally cascaded if needed.

In all cases, any IO not configured for PLD functionality retains its GPIO functionality while I/Os used by the PLD have their direction automatically set accordingly.

Please note that while RegDir corresponding bits are ignored for PLD operation they may still be set to input to access unused PLD inputs as normal GPI (PLD truth table can define some inputs to have no effect on PLD output) and/or generate interrupt based on any of the PLD inputs or outputs bits.

4.7.1 SX1501

The SX1501 I/Os can be configured to provide any combinational 2-to-1 logic function using I/O[0-2] whilst retaining GPIO capability on I/O[3] OR provide a combinational 3-to-1 decode function using all 4 I/O ports.

| RegPLDMode 1:0 | SX1501 I/Os | | | |
|-------------------|-------------|---------|--------|--------|
| | 3 | 2 | 1 | 0 |
| 00 | GPIO | GPIO | GPIO | GPIO |
| 01 | GPIO | PLD OUT | PLD IN | PLD IN |
| 10 | PLD OUT | PLD IN | PLD IN | PLD IN |

Table 8 – SX1501 PLD Modes Settings

WIRELESS & SENSING
4.7.2 SX1502

The SX1502 I/Os can be configured as per the SX1501, and can additionally be configured to provide a 2-to-1 logic function on I/O[4-6], 3-to-1 logic function on I/O[4-7], or 3-to-2 logic decode on I/O[0-4].

| RegPLDMode | | SX1502 I/Os | | | | | | | |
|------------|-----|-------------|---------|--------|---------|---------|---------|--------|--------|
| 5:4 | 1:0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 00 | 00 | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO |
| 00 | 01 | GPIO | GPIO | GPIO | GPIO | GPIO | PLD OUT | PLD IN | PLD IN |
| 00 | 10 | GPIO | GPIO | GPIO | GPIO | PLD OUT | PLD IN | PLD IN | PLD IN |
| 00 | 11 | GPIO | GPIO | GPIO | PLD OUT | PLD OUT | PLD IN | PLD IN | PLD IN |
| 01 | 00 | GPIO | PLD OUT | PLD IN | PLD IN | GPIO | GPIO | GPIO | GPIO |
| 01 | 01 | GPIO | PLD OUT | PLD IN | PLD IN | GPIO | PLD OUT | PLD IN | PLD IN |
| 01 | 10 | GPIO | PLD OUT | PLD IN | PLD IN | PLD OUT | PLD IN | PLD IN | PLD IN |
| 01 | 11 | GPIO | GPIO | GPIO | PLD OUT | PLD OUT | PLD IN | PLD IN | PLD IN |
| 10 | 00 | PLD OUT | PLD IN | PLD IN | PLD IN | GPIO | GPIO | GPIO | GPIO |
| 10 | 01 | PLD OUT | PLD IN | PLD IN | PLD IN | GPIO | PLD OUT | PLD IN | PLD IN |
| 10 | 10 | PLD OUT | PLD IN | PLD IN | PLD IN | PLD OUT | PLD IN | PLD IN | PLD IN |
| 10 | 11 | GPIO | GPIO | GPIO | PLD OUT | PLD OUT | PLD IN | PLD IN | PLD IN |

Table 9 – SX1502 PLD Modes Settings

4.7.3 SX1503

Each of the two I/O banks of the SX1503 I/Os can be configured as per the SX1502.

| RegPLDModeB | | SX1503 I/Os | | | | | | | |
|-------------|-----|-------------|---------|--------|---------|---------|---------|--------|--------|
| 5:4 | 1:0 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| 00 | 00 | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO |
| 00 | 01 | GPIO | GPIO | GPIO | GPIO | GPIO | PLD OUT | PLD IN | PLD IN |
| 00 | 10 | GPIO | GPIO | GPIO | GPIO | PLD OUT | PLD IN | PLD IN | PLD IN |
| 00 | 11 | GPIO | GPIO | GPIO | PLD OUT | PLD OUT | PLD IN | PLD IN | PLD IN |
| 01 | 00 | GPIO | PLD OUT | PLD IN | PLD IN | GPIO | GPIO | GPIO | GPIO |
| 01 | 01 | GPIO | PLD OUT | PLD IN | PLD IN | GPIO | PLD OUT | PLD IN | PLD IN |
| 01 | 10 | GPIO | PLD OUT | PLD IN | PLD IN | PLD OUT | PLD IN | PLD IN | PLD IN |
| 01 | 11 | GPIO | GPIO | GPIO | PLD OUT | PLD OUT | PLD IN | PLD IN | PLD IN |
| 10 | 00 | PLD OUT | PLD IN | PLD IN | PLD IN | GPIO | GPIO | GPIO | GPIO |
| 10 | 01 | PLD OUT | PLD IN | PLD IN | PLD IN | GPIO | PLD OUT | PLD IN | PLD IN |
| 10 | 10 | PLD OUT | PLD IN | PLD IN | PLD IN | PLD OUT | PLD IN | PLD IN | PLD IN |
| 10 | 11 | GPIO | GPIO | GPIO | PLD OUT | PLD OUT | PLD IN | PLD IN | PLD IN |

Table 10 – SX1503 PLD Modes Settings (Bank B)

| RegPLDModeA | | SX1503 I/Os | | | | | | | |
|-------------|-----|-------------|---------|--------|---------|---------|---------|--------|--------|
| 5:4 | 1:0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 00 | 00 | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO |
| 00 | 01 | GPIO | GPIO | GPIO | GPIO | GPIO | PLD OUT | PLD IN | PLD IN |
| 00 | 10 | GPIO | GPIO | GPIO | GPIO | PLD OUT | PLD IN | PLD IN | PLD IN |
| 00 | 11 | GPIO | GPIO | GPIO | PLD OUT | PLD OUT | PLD IN | PLD IN | PLD IN |
| 01 | 00 | GPIO | PLD OUT | PLD IN | PLD IN | GPIO | GPIO | GPIO | GPIO |
| 01 | 01 | GPIO | PLD OUT | PLD IN | PLD IN | GPIO | PLD OUT | PLD IN | PLD IN |
| 01 | 10 | GPIO | PLD OUT | PLD IN | PLD IN | PLD OUT | PLD IN | PLD IN | PLD IN |
| 01 | 11 | GPIO | GPIO | GPIO | PLD OUT | PLD OUT | PLD IN | PLD IN | PLD IN |
| 10 | 00 | PLD OUT | PLD IN | PLD IN | PLD IN | GPIO | GPIO | GPIO | GPIO |
| 10 | 01 | PLD OUT | PLD IN | PLD IN | PLD IN | GPIO | PLD OUT | PLD IN | PLD IN |
| 10 | 10 | PLD OUT | PLD IN | PLD IN | PLD IN | PLD OUT | PLD IN | PLD IN | PLD IN |
| 10 | 11 | GPIO | GPIO | GPIO | PLD OUT | PLD OUT | PLD IN | PLD IN | PLD IN |

Table 11 – SX1503 PLD Modes Settings (Bank B)

WIRELESS & SENSING
4.7.4 Tutorial

The generic method described in this paragraph can be applied to any of the SX1501, SX1502 or SX1503.

Example: We want to implement an AND gate between I/O[0] and IO[1] on SX1502

1. Identify in the tables above the RegPLDMode setting to be programmed.
What we need corresponds to the second line of the SX1502 PLD Table => RegPLDMode = "xx00xx01"
2. Fill corresponding RegPLDTableX with the wanted truth table.
As mentioned in RegPLDMode description, using PLD 2-to-1 mode on I/O[0-2] implies to fill the truth table located in RegPLDTable0(3:0)

| I/O[1] | I/O[0] | I/O[2] |
|--------|--------|--------|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

=> RegPLDTable0 = "xxx1000"

WIRELESS & SENSING
5 CONFIGURATION REGISTERS
5.1 SX1501 4-channel GPIO

| Address | Name | Description | Default |
|---------|--------------------|----------------------------|-----------|
| 0x00 | RegData | Data register | 1111 1111 |
| 0x01 | RegDir | Direction register | 1111 1111 |
| 0x02 | RegPullUp | Pull-up register | 0000 0000 |
| 0x03 | RegPullDown | Pull-down register | 0000 0000 |
| 0x04 | Reserved | Unused | XXXX XXXX |
| 0x05 | RegInterruptMask | Interrupt mask register | 1111 1111 |
| 0x06 | RegSenseHigh | Unused | XXXX XXXX |
| 0x07 | RegSenseLow | Sense register | 0000 0000 |
| 0x08 | RegInterruptSource | Interrupt source register | 0000 0000 |
| 0x09 | RegEventStatus | Event status register | 0000 0000 |
| 0x10 | RegPLDMode | PLD mode register | 0000 0000 |
| 0x11 | RegPLDTable0 | PLD truth table 0 | 0000 0000 |
| 0x12 | RegPLDTable1 | Unused | XXXX XXXX |
| 0x13 | RegPLDTable2 | PLD truth table 2 | 0000 0000 |
| 0x14 | RegPLDTable3 | Unused | XXXX XXXX |
| 0x15 | RegPLDTable4 | Unused | XXXX XXXX |
| 0xAB | RegAdvanced | Advanced settings register | 0000 0000 |

Bits set as output take '1' as default value.

Table 12 – SX1501 Configuration Registers Overview

| Addr | Name | Default | Bits | Description |
|------|--------------------|---------|------|---|
| 0x00 | RegData | 0xFF | 7:4 | Reserved. Must be set to 1 (default value) |
| | | | 3:0 | Write: Data to be output to the output-configured IOs Read: Data seen at the IOs, independent of the direction configured. |
| 0x01 | RegDir | 0xFF | 7:4 | Reserved. Must be set to 1 (default value) |
| | | | 3:0 | Configures direction for each IO. 0 : IO is configured as an output 1 : IO is configured as an input |
| 0x02 | RegPullUp | 0x00 | 7:4 | Reserved. Must be set to 0 (default value) |
| | | | 3:0 | Enables the pull-up for each IO 0 : Pull-up is disabled 1 : Pull-up is enabled |
| 0x03 | RegPullDown | 0x00 | 7:4 | Reserved. Must be set to 0 (default value) |
| | | | 3:0 | Enables the pull-down for each IO 0 : Pull-down is disabled 1 : Pull-down is enabled |
| 0x04 | Reserved | 0xFF | 7:0 | Unused |
| 0x05 | RegInterruptMask | 0xFF | 7:4 | Reserved. Must be set to 1 (default value) |
| | | | 3:0 | Configures which [input-configured] IO will trigger an interrupt on NINT pin 0 : An event on this IO will trigger an interrupt 1 : An event on this IO will NOT trigger an interrupt |
| 0x06 | RegSenseHigh | 0xFF | 7:0 | Unused |
| 0x07 | RegSenseLow | 0x00 | 7:6 | Edge sensitivity of I/O[3] |
| | | | 5:4 | Edge sensitivity of I/O[2] |
| | | | 3:2 | Edge sensitivity of I/O[1] |
| | | | 1:0 | Edge sensitivity of I/O[0] |
| 0x08 | RegInterruptSource | 0x00 | 7:4 | Reserved. Must be set to 0 (default value) |
| | | | 3:0 | Interrupt source (from IOs set in RegInterruptMask) 0 : No interrupt has been triggered by this IO 1 : An interrupt has been triggered by this IO (an event as configured in relevant RegSense register occurred). Writing '1' clears the bit in RegInterruptSource and in RegEventStatus. When all bits are cleared, NINT signal goes back high. |
| 0x09 | | 0x00 | 7:4 | Reserved. Must be set to 0 (default value) |

WIRELESS & SENSING

| Addr | Name | Default | Bits | Description |
|------|----------------|---------|--------------------------------------|--|
| | RegEventStatus | | 3:0 | Event status of all IOs. 0 : No event has occurred on this IO 1 : An event has occurred on this IO (an edge as configured in relevant RegSense register occurred). Writing '1' clears the bit in RegEventStatus and in RegInterruptSource if relevant. If the edge sensitivity of the IO is changed, the bit(s) will be cleared automatically |
| 0x10 | RegPLDMode | 0x00 | 7:2 1:0 | Reserved. Must be set to 0 (default value) PLDMode 00 : PLD disabled – Normal GPIO mode for I/O[3:0] 01 : PLD 2-to-1 mode – I/O[2] is a decode of I/O[1:0] as defined in RegPLDTable0 10 : PLD 3-to-1 mode – I/O[3] is a decode of I/O[2:0] as defined in RegPLDTable2 11 : Not used |
| 0x11 | RegPLDTable0 | 0x00 | 7:4 3 2 1 0 | Reserved. Must be set to 0 (default value) Value to be output on I/O[2] when I/O[1:0] = 11 Value to be output on I/O[2] when I/O[1:0] = 10 Value to be output on I/O[2] when I/O[1:0] = 01 Value to be output on I/O[2] when I/O[1:0] = 00 |
| 0x12 | RegPLDTable1 | 0xXX | 7:0 | Unused |
| 0x13 | RegPLDTable2 | 0x00 | 7 6 5 4 3 2 1 0 | Value to be output on I/O[3] when I/O[2:0] = 111 Value to be output on I/O[3] when I/O[2:0] = 110 Value to be output on I/O[3] when I/O[2:0] = 101 Value to be output on I/O[3] when I/O[2:0] = 100 Value to be output on I/O[3] when I/O[2:0] = 011 Value to be output on I/O[3] when I/O[2:0] = 010 Value to be output on I/O[3] when I/O[2:0] = 001 Value to be output on I/O[3] when I/O[2:0] = 000 |
| 0x14 | RegPLDTable3 | 0xXX | 7:0 | Unused |
| 0x15 | RegPLDTable4 | 0xXX | 7:0 | Unused |
| 0xAB | RegAdvanced | 0x00 | 7.2 1 0 | Reserved. Must be set to 0 (default value) Boost Mode (Cf. §2.2.1) 0: OFF 1: ON Reserved. Must be set to 0 (default value) |

Table 13 – SX1501 Configuration Registers Description

5.2 SX1502 8-channel GPIO

| Address | Name | Description | Default |
|---------|--------------------|-----------------------------|------------|
| 0x00 | RegData | Data register | 1111 1111* |
| 0x01 | RegDir | Direction register | 1111 1111 |
| 0x02 | RegPullUp | Pull-up register | 0000 0000 |
| 0x03 | RegPullDown | Pull-down register | 0000 0000 |
| 0x04 | Reserved | Unused | XXXX XXXX |
| 0x05 | RegInterruptMask | Interrupt mask register | 1111 1111 |
| 0x06 | RegSenseHigh | Sense register for I/O[7:4] | 0000 0000 |
| 0x07 | RegSenseLow | Sense register for I/O[3:0] | 0000 0000 |
| 0x08 | RegInterruptSource | Interrupt source register | 0000 0000 |
| 0x09 | RegEventStatus | Event status register | 0000 0000 |
| 0x10 | RegPLDMode | PLD mode register | 0000 0000 |
| 0x11 | RegPLDTable0 | PLD truth table 0 | 0000 0000 |
| 0x12 | RegPLDTable1 | PLD truth table 1 | 0000 0000 |
| 0x13 | RegPLDTable2 | PLD truth table 2 | 0000 0000 |
| 0x14 | RegPLDTable3 | PLD truth table 3 | 0000 0000 |
| 0x15 | RegPLDTable4 | PLD truth table 4 | 0000 0000 |
| 0xAB | RegAdvanced | Advanced settings register | 0000 0000 |

*Bits set as output take '1' as default value.

Table 14 – SX1502 Configuration Registers Overview

| Addr | Name | Default | Bits | Description |
|------|---------|---------|------|---|
| 0x00 | RegData | 0xFF | 7:0 | Write: Data to be output to the output-configured IOs Read: Data seen at the IOs, independent of the direction configured. |
| 0x01 | RegDir | 0xFF | 7:0 | Configures direction for each IO. 0 : IO is configured as an output 1 : IO is configured as an input |

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| Addr | Name | Default | Bits | Description | |
|------|--|---------|------|--|---|
| 0x02 | RegPullUp | 0x00 | 7:0 | Enables the pull-up for each IO 0 : Pull-up is disabled 1 : Pull-up is enabled | |
| 0x03 | RegPullDown | 0x00 | 7:0 | Enables the pull-down for each IO 0 : Pull-down is disabled 1 : Pull-down is enabled | |
| 0x04 | Reserved | 0xFF | 7:0 | Unused | |
| 0x05 | RegInterruptMask | 0xFF | 7:0 | Configures which [input-configured] IO will trigger an interrupt on NINT pin 0 : An event on this IO will trigger an interrupt 1 : An event on this IO will NOT trigger an interrupt | |
| 0x06 | RegSenseHigh | 0x00 | 7:6 | Edge sensitivity of I/O[7] | 00 : None 01 : Rising 10 : Falling 11 : Both |
| | | | 5:4 | Edge sensitivity of I/O[6] | |
| | | | 3:2 | Edge sensitivity of I/O[5] | |
| | | | 1:0 | Edge sensitivity of I/O[4] | |
| 0x07 | RegSenseLow | 0x00 | 7:6 | Edge sensitivity of I/O[3] | 00 : None 01 : Rising 10 : Falling 11 : Both |
| | | | 5:4 | Edge sensitivity of I/O[2] | |
| | | | 3:2 | Edge sensitivity of I/O[1] | |
| | | | 1:0 | Edge sensitivity of I/O[0] | |
| 0x08 | RegInterruptSource | 0x00 | 7:0 | Interrupt source (from IOs set in RegInterruptMask) 0 : No interrupt has been triggered by this IO 1 : An interrupt has been triggered by this IO (an event as configured in relevant RegSense register occurred). Writing '1' clears the bit in RegInterruptSource and in RegEventStatus When all bits are cleared, NINT signal goes back high. | |
| 0x09 | RegEventStatus | 0x00 | 7:0 | Event status of all IOs. 0 : No event has occurred on this IO 1 : An event has occurred on this IO (an edge as configured in relevant RegSense register occurred). Writing '1' clears the bit in RegEventStatus and in RegInterruptSource if relevant. If the edge sensitivity of the IO is changed, the bit(s) will be cleared automatically | |
| 0x10 | RegPLDMode | 0x00 | 7:6 | Reserved. Must be set to 0 (default value) | |
| | | | 5:4 | PLDModeHigh (applies to I/O[7:4]) 00 : PLD disabled – Normal GPIO mode for I/O[7:4] 01 : PLD 2-to-1 mode – I/O[6] is a decode of I/O[5:4] as defined in RegPLDTable0 10 : PLD 3-to-1 mode – I/O[7] is a decode of I/O[6:4] as defined in RegPLDTable1 11 : Reserved | |
| | | | 3:2 | Reserved. Must be set to 0 (default value) | |
| | | | 1:0 | PLDModeLow (applies to I/O[3:0]) 00 : PLD disabled – Normal GPIO mode for I/O[3:0] 01 : PLD 2-to-1 mode – I/O[2] is a decode of I/O[1:0] as defined in RegPLDTable0 10 : PLD 3-to-1 mode – I/O[3] is a decode of I/O[2:0] as defined in RegPLDTable2 11 : PLD 3-to-2 mode – I/O[4:3] are decodes of I/O[2:0] as defined in RegPLDTable3 and RegPLDTable4 | |
| 0x11 | RegPLDTable0 | 0x00 | 7 | Value to be output on I/O[6] when I/O[5:4] = 11 | Applies only when PLDModeHigh is set to PLD 2-to-1 mode |
| | | | 6 | Value to be output on I/O[6] when I/O[5:4] = 10 | |
| | | | 5 | Value to be output on I/O[6] when I/O[5:4] = 01 | |
| | | | 4 | Value to be output on I/O[6] when I/O[5:4] = 00 | |
| | | | 3 | Value to be output on I/O[2] when I/O[1:0] = 11 | Applies only when PLDModeLow is set to PLD 2-to-1 mode |
| | | | 2 | Value to be output on I/O[2] when I/O[1:0] = 10 | |
| | | | 1 | Value to be output on I/O[2] when I/O[1:0] = 01 | |
| | | | 0 | Value to be output on I/O[2] when I/O[1:0] = 00 | |
| 0x12 | RegPLDTable1 | 0x00 | 7 | Value to be output on I/O[7] when I/O[6:4] = 111 | Applies only when PLDModeHigh is set to PLD 3-to-1 mode |
| | | | 6 | Value to be output on I/O[7] when I/O[6:4] = 110 | |
| | | | 5 | Value to be output on I/O[7] when I/O[6:4] = 101 | |
| | | | 4 | Value to be output on I/O[7] when I/O[6:4] = 100 | |
| | | | 3 | Value to be output on I/O[7] when I/O[6:4] = 011 | |
| | | | 2 | Value to be output on I/O[7] when I/O[6:4] = 010 | |
| | | | 1 | Value to be output on I/O[7] when I/O[6:4] = 001 | |
| 0 | Value to be output on I/O[7] when I/O[6:4] = 000 | | | | |
| 0x13 | RegPLDTable2 | 0x00 | 7 | Value to be output on I/O[3] when I/O[2:0] = 111 | Applies only when PLDModeLow is set to PLD 3-to-1 mode |
| | | | 6 | Value to be output on I/O[3] when I/O[2:0] = 110 | |
| | | | 5 | Value to be output on I/O[3] when I/O[2:0] = 101 | |
| | | | 4 | Value to be output on I/O[3] when I/O[2:0] = 100 | |
| | | | 3 | Value to be output on I/O[3] when I/O[2:0] = 011 | |
| | | | 2 | Value to be output on I/O[3] when I/O[2:0] = 010 | |
| 1 | Value to be output on I/O[3] when I/O[2:0] = 001 | | | | |

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| Addr | Name | Default | Bits | Description |
|------|--------------|---------|------|--|
| 0x14 | RegPLDTable3 | 0x00 | 0 | Value to be output on I/O[3] when I/O[2:0] = 000 |
| | | | 7 | Value to be output on I/O[4] when I/O[2:0] = 111 |
| | | | 6 | Value to be output on I/O[4] when I/O[2:0] = 110 |
| | | | 5 | Value to be output on I/O[4] when I/O[2:0] = 101 |
| | | | 4 | Value to be output on I/O[4] when I/O[2:0] = 100 |
| | | | 3 | Value to be output on I/O[4] when I/O[2:0] = 011 |
| | | | 2 | Value to be output on I/O[4] when I/O[2:0] = 010 |
| | | | 1 | Value to be output on I/O[4] when I/O[2:0] = 001 |
| 0x15 | RegPLDTable4 | 0x00 | 0 | Value to be output on I/O[4] when I/O[2:0] = 000 |
| | | | 7 | Value to be output on I/O[3] when I/O[2:0] = 111 |
| | | | 6 | Value to be output on I/O[3] when I/O[2:0] = 110 |
| | | | 5 | Value to be output on I/O[3] when I/O[2:0] = 101 |
| | | | 4 | Value to be output on I/O[3] when I/O[2:0] = 100 |
| | | | 3 | Value to be output on I/O[3] when I/O[2:0] = 011 |
| | | | 2 | Value to be output on I/O[3] when I/O[2:0] = 010 |
| | | | 1 | Value to be output on I/O[3] when I/O[2:0] = 001 |
| 0xAB | RegAdvanced | 0x00 | 7:2 | Reserved. Must be set to 0 (default value) |
| | | | 1 | Boost Mode (Cf. §2.2.1) 0: OFF 1: ON |
| | | | 0 | Reserved. Must be set to 0 (default value) |

Table 15 – SX1502 Configuration Registers Description

5.3 SX1503 16-channel GPIO

| Address | Name | Description | Default |
|---------|---------------------|--|-----------|
| 0x00 | RegDataB | Data register for Bank B I/O[15:8] | 1111 1111 |
| 0x01 | RegDataA | Data register for Bank A I/O[7:0] | 1111 1111 |
| 0x02 | RegDirB | Direction register for Bank B I/O[15:8] | 1111 1111 |
| 0x03 | RegDirA | Direction register for Bank A I/O[7:0] | 1111 1111 |
| 0x04 | RegPullUpB | Pull-up register for Bank B I/O[15:8] | 0000 0000 |
| 0x05 | RegPullUpA | Pull-up register for Bank A I/O[7:0] | 0000 0000 |
| 0x06 | RegPullDownB | Pull-down register for Bank B I/O[15:8] | 0000 0000 |
| 0x07 | RegPullDownA | Pull-down register for Bank A I/O[7:0] | 0000 0000 |
| 0x08 | RegInterruptMaskB | Interrupt mask register for Bank B I/O[15:8] | 1111 1111 |
| 0x09 | RegInterruptMaskA | Interrupt mask register for Bank A I/O[7:0] | 1111 1111 |
| 0x0A | RegSenseHighB | Sense register for I/O[15:12] | 0000 0000 |
| 0x0B | RegSenseHighA | Sense register for I/O[7:4] | 0000 0000 |
| 0x0C | RegSenseLowB | Sense register for I/O[11:8] | 0000 0000 |
| 0x0D | RegSenseLowA | Sense register for I/O[3:0] | 0000 0000 |
| 0x0E | RegInterruptSourceB | Interrupt source register for Bank B I/O[15:8] | 0000 0000 |
| 0x0F | RegInterruptSourceA | Interrupt source register for Bank A I/O[7:0] | 0000 0000 |
| 0x10 | RegEventStatusB | Event status register for Bank B I/O[15:8] | 0000 0000 |
| 0x11 | RegEventStatusA | Event status register for Bank A I/O[7:0] | 0000 0000 |
| 0x20 | RegPLDModeB | PLD mode register for Bank B I/O[15:8] | 0000 0000 |
| 0x21 | RegPLDModeA | PLD mode register for Bank A I/O[7:0] | 0000 0000 |
| 0x22 | RegPLDTable0B | PLD truth table 0 for Bank B I/O[15:8] | 0000 0000 |
| 0x23 | RegPLDTable0A | PLD truth table 0 for Bank A I/O[7:0] | 0000 0000 |
| 0x24 | RegPLDTable1B | PLD truth table 1 for Bank B I/O[15:8] | 0000 0000 |
| 0x25 | RegPLDTable1A | PLD truth table 1 for Bank A I/O[7:0] | 0000 0000 |
| 0x26 | RegPLDTable2B | PLD truth table 2 for Bank B I/O[15:8] | 0000 0000 |
| 0x27 | RegPLDTable2A | PLD truth table 2 for Bank A I/O[7:0] | 0000 0000 |
| 0x28 | RegPLDTable3B | PLD truth table 3 for Bank B I/O[15:8] | 0000 0000 |
| 0x29 | RegPLDTable3A | PLD truth table 3 for Bank A I/O[7:0] | 0000 0000 |
| 0x2A | RegPLDTable4B | PLD truth table 4 for Bank B I/O[15:8] | 0000 0000 |
| 0x2B | RegPLDTable4A | PLD truth table 4 for Bank A I/O[7:0] | 0000 0000 |
| 0xAD | RegAdvanced | Advanced settings register | 0000 0000 |

Bits set as output take "1" as default value.

Table 16 – SX1503 Configuration Registers Overview

| Addr | Name | Default | Bits | Description |
|------|------|---------|------|-------------|
|------|------|---------|------|-------------|

WIRELESS & SENSING

| Addr | Name | Default | Bits | Description | |
|------|---------------------|---------|------|---|---|
| 0x00 | RegDataB | 0xFF | 7:0 | Write: Data to be output to the output-configured IOs Read: Data seen at the IOs, independent of the direction configured. | |
| 0x01 | RegDataA | 0xFF | 7:0 | Write: Data to be output to the output-configured IOs Read: Data seen at the IOs, independent of the direction configured. | |
| 0x02 | RegDirB | 0xFF | 7:0 | Configures direction for each IO. 0 : IO is configured as an output 1 : IO is configured as an input | |
| 0x03 | RegDirA | 0xFF | 7:0 | Configures direction for each IO. 0 : IO is configured as an output 1 : IO is configured as an input | |
| 0x04 | RegPullUpB | 0x00 | 7:0 | Enables the pull-up for each IO 0 : Pull-up is disabled 1 : Pull-up is enabled | |
| 0x05 | RegPullUpA | 0x00 | 7:0 | Enables the pull-up for each IO 0 : Pull-up is disabled 1 : Pull-up is enabled | |
| 0x06 | RegPullDownB | 0x00 | 7:0 | Enables the pull-down for each IO 0 : Pull-down is disabled 1 : Pull-down is enabled | |
| 0x07 | RegPullDownA | 0x00 | 7:0 | Enables the pull-down for each IO 0 : Pull-down is disabled 1 : Pull-down is enabled | |
| 0x08 | RegInterruptMaskB | 0xFF | 7:0 | Configures which [input-configured] IO will trigger an interrupt on NINT pin 0 : An event on this IO will trigger an interrupt 1 : An event on this IO will NOT trigger an interrupt | |
| 0x09 | RegInterruptMaskA | 0xFF | 7:0 | Configures which [input-configured] IO will trigger an interrupt on NINT pin 0 : An event on this IO will trigger an interrupt 1 : An event on this IO will NOT trigger an interrupt | |
| 0x0A | RegSenseHighB | 0x00 | 7:6 | Edge sensitivity of I/O[15] | 00 : None 01 : Rising 10 : Falling 11 : Both |
| | | | 5:4 | Edge sensitivity of I/O[14] | |
| | | | 3:2 | Edge sensitivity of I/O[13] | |
| | | | 1:0 | Edge sensitivity of I/O[12] | |
| 0x0B | RegSenseHighA | 0x00 | 7:6 | Edge sensitivity of I/O[7] | 00 : None 01 : Rising 10 : Falling 11 : Both |
| | | | 5:4 | Edge sensitivity of I/O[6] | |
| | | | 3:2 | Edge sensitivity of I/O[5] | |
| | | | 1:0 | Edge sensitivity of I/O[4] | |
| 0x0C | RegSenseLowB | 0x00 | 7:6 | Edge sensitivity of I/O[11] | 00 : None 01 : Rising 10 : Falling 11 : Both |
| | | | 5:4 | Edge sensitivity of I/O[10] | |
| | | | 3:2 | Edge sensitivity of I/O[9] | |
| | | | 1:0 | Edge sensitivity of I/O[8] | |
| 0x0D | RegSenseLowA | 0x00 | 7:6 | Edge sensitivity of I/O[3] | 00 : None 01 : Rising 10 : Falling 11 : Both |
| | | | 5:4 | Edge sensitivity of I/O[2] | |
| | | | 3:2 | Edge sensitivity of I/O[1] | |
| | | | 1:0 | Edge sensitivity of I/O[0] | |
| 0x0E | RegInterruptSourceB | 0x00 | 7:0 | Interrupt source (from IOs set in RegInterruptMaskB) 0 : No interrupt has been triggered by this IO 1 : An interrupt has been triggered by this IO (an event as configured in relevant RegSense register occurred). Writing '1' clears the bit in RegInterruptSourceB and in RegEventStatusB When all bits of both RegInterruptSourceA/B are cleared, NINT signal goes back high. | |
| 0x0F | RegInterruptSourceA | 0x00 | 7:0 | Interrupt source (from IOs set in RegInterruptMaskA) 0 : No interrupt has been triggered by this IO 1 : An interrupt has been triggered by this IO (an event as configured in relevant RegSense register occurred). Writing '1' clears the bit in RegInterruptSourceA and in RegEventStatusA When all bits of both RegInterruptSourceA/B are cleared, NINT signal goes back high. | |
| 0x10 | RegEventStatusB | 0x00 | 7:0 | Event status of all IOs. 0 : No event has occurred on this IO 1 : An event has occurred on this IO (an edge as configured in relevant RegSense register occurred). Writing '1' clears the bit in RegEventStatusB and in RegInterruptSourceB if relevant. If the edge sensitivity of the IO is changed, the bit(s) will be cleared automatically | |

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| Addr | Name | Default | Bits | Description |
|------|-----------------|---------|------|---|
| 0x11 | RegEventStatusA | 0x00 | 7:0 | Event status of all IOs. 0 : No event has occurred on this IO 1 : An event has occurred on this IO (an edge as configured in relevant RegSense register occurred). Writing '1' clears the bit in RegEventStatusA and in RegInterruptSourceA if relevant. If the edge sensitivity of the IO is changed, the bit(s) will be cleared automatically |
| 0x20 | RegPLDModeB | 0x00 | 7:6 | Reserved. Must be set to 0 (default value) |
| | | | 5:4 | PLDModeHighB (applies to I/O[15:12]) 00 : PLD disabled – Normal GPIO mode for I/O[15:12] 01 : PLD 2-to-1 mode – I/O[14] is a decode of I/O[13:12] as defined in RegPLDTable0B 10 : PLD 3-to-1 mode – I/O[15] is a decode of I/O[14:12] as defined in RegPLDTable1B 11 : Reserved |
| | | | 3:2 | Reserved. Must be set to 0 (default value) |
| | | | 1:0 | PLDModeLowB (applies to I/O[11:8]) 00 : PLD disabled – Normal GPIO mode for I/O[11:8] 01 : PLD 2-to-1 mode – I/O[10] is a decode of I/O[9:8] as defined in RegPLDTable0B 10 : PLD 3-to-1 mode – I/O[11] is a decode of I/O[10:8] as defined in RegPLDTable2B 11 : PLD 3-to-2 mode – I/O[12:11] are decodes of I/O[10:8] as defined in RegPLDTable3B and RegPLDTable4B |
| 0x21 | RegPLDModeA | 0x00 | 7:6 | Reserved. Must be set to 0 (default value) |
| | | | 5:4 | PLDModeHighA (applies to I/O[7:4]) 00 : PLD disabled – Normal GPIO mode for I/O[7:4] 01 : PLD 2-to-1 mode – I/O[6] is a decode of I/O[5:4] as defined in RegPLDTable0A 10 : PLD 3-to-1 mode – I/O[7] is a decode of I/O[6:4] as defined in RegPLDTable1A 11 : Reserved |
| | | | 3:2 | Reserved. Must be set to 0 (default value) |
| | | | 1:0 | PLDModeLowA (applies to I/O[3:0]) 00 : PLD disabled – Normal GPIO mode for I/O[3:0] 01 : PLD 2-to-1 mode – I/O[2] is a decode of I/O[1:0] as defined in RegPLDTable0A 10 : PLD 3-to-1 mode – I/O[3] is a decode of I/O[2:0] as defined in RegPLDTable2A 11 : PLD 3-to-2 mode – I/O[4:3] are decodes of I/O[2:0] as defined in RegPLDTable3A and RegPLDTable4A |
| 0x22 | RegPLDTable0B | 0x00 | 7 | Value to be output on I/O[14] when I/O[13:12] = 11 |
| | | | 6 | Value to be output on I/O[14] when I/O[13:12] = 10 |
| | | | 5 | Value to be output on I/O[14] when I/O[13:12] = 01 |
| | | | 4 | Value to be output on I/O[14] when I/O[13:12] = 00 |
| | | | 3 | Value to be output on I/O[10] when I/O[9:8] = 11 |
| | | | 2 | Value to be output on I/O[10] when I/O[9:8] = 10 |
| | | | 1 | Value to be output on I/O[10] when I/O[9:8] = 01 |
| | | | 0 | Value to be output on I/O[10] when I/O[9:8] = 00 |
| 0x23 | RegPLDTable0A | 0x00 | 7 | Value to be output on I/O[6] when I/O[5:4] = 11 |
| | | | 6 | Value to be output on I/O[6] when I/O[5:4] = 10 |
| | | | 5 | Value to be output on I/O[6] when I/O[5:4] = 01 |
| | | | 4 | Value to be output on I/O[6] when I/O[5:4] = 00 |
| | | | 3 | Value to be output on I/O[2] when I/O[1:0] = 11 |
| | | | 2 | Value to be output on I/O[2] when I/O[1:0] = 10 |
| | | | 1 | Value to be output on I/O[2] when I/O[1:0] = 01 |
| | | | 0 | Value to be output on I/O[2] when I/O[1:0] = 00 |
| 0x24 | RegPLDTable1B | 0x00 | 7 | Value to be output on I/O[15] when I/O[14:12] = 111 |
| | | | 6 | Value to be output on I/O[15] when I/O[14:12] = 110 |
| | | | 5 | Value to be output on I/O[15] when I/O[14:12] = 101 |
| | | | 4 | Value to be output on I/O[15] when I/O[14:12] = 100 |
| | | | 3 | Value to be output on I/O[15] when I/O[14:12] = 011 |
| | | | 2 | Value to be output on I/O[15] when I/O[14:12] = 010 |
| | | | 1 | Value to be output on I/O[15] when I/O[14:12] = 001 |
| | | | 0 | Value to be output on I/O[15] when I/O[14:12] = 000 |
| 0x25 | RegPLDTable1A | 0x00 | 7 | Value to be output on I/O[7] when I/O[6:4] = 111 |
| | | | 6 | Value to be output on I/O[7] when I/O[6:4] = 110 |
| | | | 5 | Value to be output on I/O[7] when I/O[6:4] = 101 |
| | | | 4 | Value to be output on I/O[7] when I/O[6:4] = 100 |
| | | | 3 | Value to be output on I/O[7] when I/O[6:4] = 011 |
| | | | 2 | Value to be output on I/O[7] when I/O[6:4] = 010 |
| | | | 1 | Value to be output on I/O[7] when I/O[6:4] = 001 |
| | | | 0 | Value to be output on I/O[7] when I/O[6:4] = 000 |
| 0x26 | RegPLDTable2B | 0x00 | 7 | Value to be output on I/O[11] when I/O[10:8] = 111 |
| | | | 6 | Value to be output on I/O[11] when I/O[10:8] = 110 |

WIRELESS & SENSING

| Addr | Name | Default | Bits | Description | |
|------|---------------|---------|------|---|--|
| | | | 5 | Value to be output on I/O[11] when I/O[10:8] = 101 | 3-to-1 mode |
| | | | 4 | Value to be output on I/O[11] when I/O[10:8] = 100 | |
| | | | 3 | Value to be output on I/O[11] when I/O[10:8] = 011 | |
| | | | 2 | Value to be output on I/O[11] when I/O[10:8] = 010 | |
| | | | 1 | Value to be output on I/O[11] when I/O[10:8] = 001 | |
| | | | 0 | Value to be output on I/O[11] when I/O[10:8] = 000 | |
| 0x27 | RegPLDTable2A | 0x00 | 7 | Value to be output on I/O[3] when I/O[2:0] = 111 | Applies only when PLDModelLowA is set to PLD 3-to-1 mode |
| | | | 6 | Value to be output on I/O[3] when I/O[2:0] = 110 | |
| | | | 5 | Value to be output on I/O[3] when I/O[2:0] = 101 | |
| | | | 4 | Value to be output on I/O[3] when I/O[2:0] = 100 | |
| | | | 3 | Value to be output on I/O[3] when I/O[2:0] = 011 | |
| | | | 2 | Value to be output on I/O[3] when I/O[2:0] = 010 | |
| | | | 1 | Value to be output on I/O[3] when I/O[2:0] = 001 | |
| | | | 0 | Value to be output on I/O[3] when I/O[2:0] = 000 | |
| 0x28 | RegPLDTable3B | 0x00 | 7 | Value to be output on I/O[11] when I/O[10:8] = 111 | Applies only when PLDModelLowB is set to PLD 3-to-2 mode |
| | | | 6 | Value to be output on I/O[11] when I/O[10:8] = 110 | |
| | | | 5 | Value to be output on I/O[11] when I/O[10:8] = 101 | |
| | | | 4 | Value to be output on I/O[11] when I/O[10:8] = 100 | |
| | | | 3 | Value to be output on I/O[11] when I/O[10:8] = 011 | |
| | | | 2 | Value to be output on I/O[11] when I/O[10:8] = 010 | |
| | | | 1 | Value to be output on I/O[11] when I/O[10:8] = 001 | |
| | | | 0 | Value to be output on I/O[11] when I/O[10:8] = 000 | |
| 0x29 | RegPLDTable3A | 0x00 | 7 | Value to be output on I/O[3] when I/O[2:0] = 111 | Applies only when PLDModelLowA is set to PLD 3-to-2 mode |
| | | | 6 | Value to be output on I/O[3] when I/O[2:0] = 110 | |
| | | | 5 | Value to be output on I/O[3] when I/O[2:0] = 101 | |
| | | | 4 | Value to be output on I/O[3] when I/O[2:0] = 100 | |
| | | | 3 | Value to be output on I/O[3] when I/O[2:0] = 011 | |
| | | | 2 | Value to be output on I/O[3] when I/O[2:0] = 010 | |
| | | | 1 | Value to be output on I/O[3] when I/O[2:0] = 001 | |
| | | | 0 | Value to be output on I/O[3] when I/O[2:0] = 000 | |
| 0x2A | RegPLDTable4B | 0x00 | 7 | Value to be output on I/O[12] when I/O[10:8] = 111 | Applies only when PLDModelLowB is set to PLD 3-to-2 mode |
| | | | 6 | Value to be output on I/O[12] when I/O[10:8] = 110 | |
| | | | 5 | Value to be output on I/O[12] when I/O[10:8] = 101 | |
| | | | 4 | Value to be output on I/O[12] when I/O[10:8] = 100 | |
| | | | 3 | Value to be output on I/O[12] when I/O[10:8] = 011 | |
| | | | 2 | Value to be output on I/O[12] when I/O[10:8] = 010 | |
| | | | 1 | Value to be output on I/O[12] when I/O[10:8] = 001 | |
| | | | 0 | Value to be output on I/O[12] when I/O[10:8] = 000 | |
| 0x2B | RegPLDTable4A | 0x00 | 7 | Value to be output on I/O[4] when I/O[2:0] = 111 | Applies only when PLDModelLowA is set to PLD 3-to-2 mode |
| | | | 6 | Value to be output on I/O[4] when I/O[2:0] = 110 | |
| | | | 5 | Value to be output on I/O[4] when I/O[2:0] = 101 | |
| | | | 4 | Value to be output on I/O[4] when I/O[2:0] = 100 | |
| | | | 3 | Value to be output on I/O[4] when I/O[2:0] = 011 | |
| | | | 2 | Value to be output on I/O[4] when I/O[2:0] = 010 | |
| | | | 1 | Value to be output on I/O[4] when I/O[2:0] = 001 | |
| | | | 0 | Value to be output on I/O[4] when I/O[2:0] = 000 | |
| 0xAD | RegAdvanced | 0x00 | 7:3 | Reserved. Must be set to 0 (default value) | |
| | | | 2 | Autoclear NINT on RegData read (Cf. §4.6) 0: OFF.RegInterruptSource must be manually cleared directly or via RegEventStatus 1: ON.RegInterruptSource is automatically cleared when RegDataB or RegDataA is read | |
| | | | 1 | Boost Mode (Cf. §2.2.1) 0: OFF 1: ON | |
| | | | 0 | Reserved. Must be set to 0 (default value) | |

Table 17 – SX1503 Configuration Registers Description

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6 APPLICATION INFORMATION

6.1 Typical Application Circuit

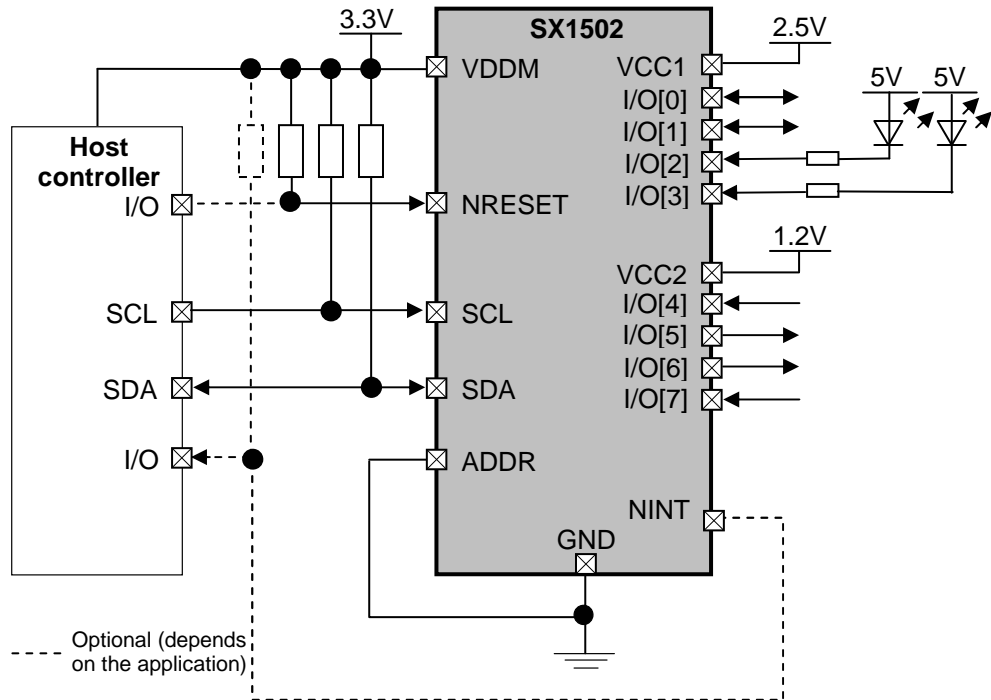
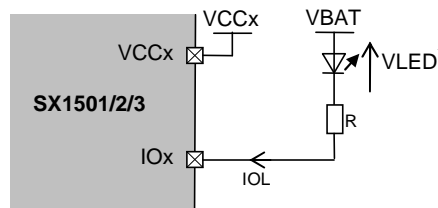


Figure 12 - Typical Application Schematic

6.2 Typical LED Operation

Typical LED operation is described below. The LED is usually connected to a high voltage (VBAT) to take advantage of the high sink current of the I/O and to accommodate high LED threshold voltages (VLED).



^{*}LED colour/technology dependent

Figure 13 – Typical LED Operation

Important:

- ❖ VCCx must exceed VBAT-VLED (VCCx = VBAT is recommended) else the LED will never be completely OFF
- ❖ R must be calculated for IOL not to exceed its max spec (Cf. Table 5)

6.2.1 LED ON/OFF Control

| | RegDir[x] | RegData[x] |
|---------|--------------|------------|
| LED ON | "0" (Output) | "0" |
| LED OFF | | "1" |

Table 18 – LED ON/OFF Control

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6.2.2 LED Intensity Control

When the max IOL spec is not enough it is possible to drive simultaneously multiple I/Os connected together hence increasing the total sink capability.

Example: on an SX1502, by driving an LED with both IO[2] and IO[3] one can sink up to $24+24=48\text{mA}$.

Driving an LED with multiple I/Os can also be used to implement more intensity steps for the LED.

Example: with two I/Os capable of sinking each 24mA the LED can sink a total of 0mA (no I/O set to "0"), 24mA (one I/O set to "0") or 48mA (both I/Os set to "0") => 3 LED intensity steps (4 steps with 3 I/Os, 5 steps with 4 I/Os, etc)

6.3 Keypad Implementation

SX1501, SX1502, and SX1503 can be used to implement keypad applications up to 8×8 matrix (i.e. 64 keys)

Example: We want to implement a 4×4 matrix keypad on SX1502

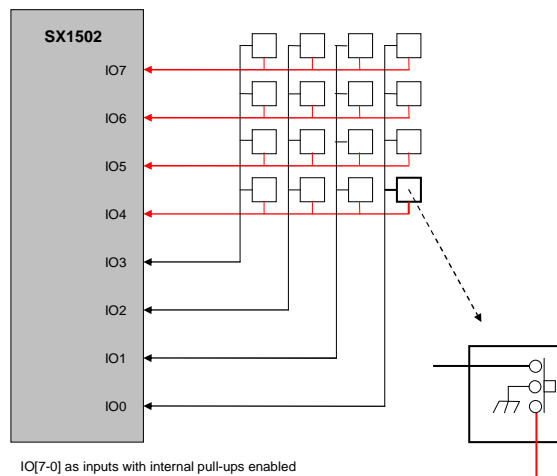


Figure 14 – 4×4 keypad connection to SX1502

1. Set all I/Os as inputs with internal pull-up ($\text{RegDir} = 0\text{xFF}$, $\text{RegPullUp} = 0\text{xFF}$)
2. Set NINT to be triggered on any IO's falling edge ($\text{RegInterruptMask} = 0\text{x00}$, $\text{RegSenseHigh} = 0\text{xAA}$, $\text{RegSenseLow} = 0\text{xAA}$)
3. When NINT goes low read RegData (or $\text{RegInterruptSource}$) to know the X:Y coordinates of the button which has been pressed.
4. Clear NINT ($\text{RegInterruptSource} = 0\text{xFF}$, can be done automatically on SX1503 depending on RegAdvanced setting)
5. Restart from point 3

6.4 Level Shifter Implementation Hints

Because of their I/O banks with independent supply voltages between 1.2V and 5.5V , the SX1502 and SX1503 can be easily used to perform level shifting of signals from one I/O bank to another (uC reads I/O from one I/O bank and sends it back to the other I/O bank)

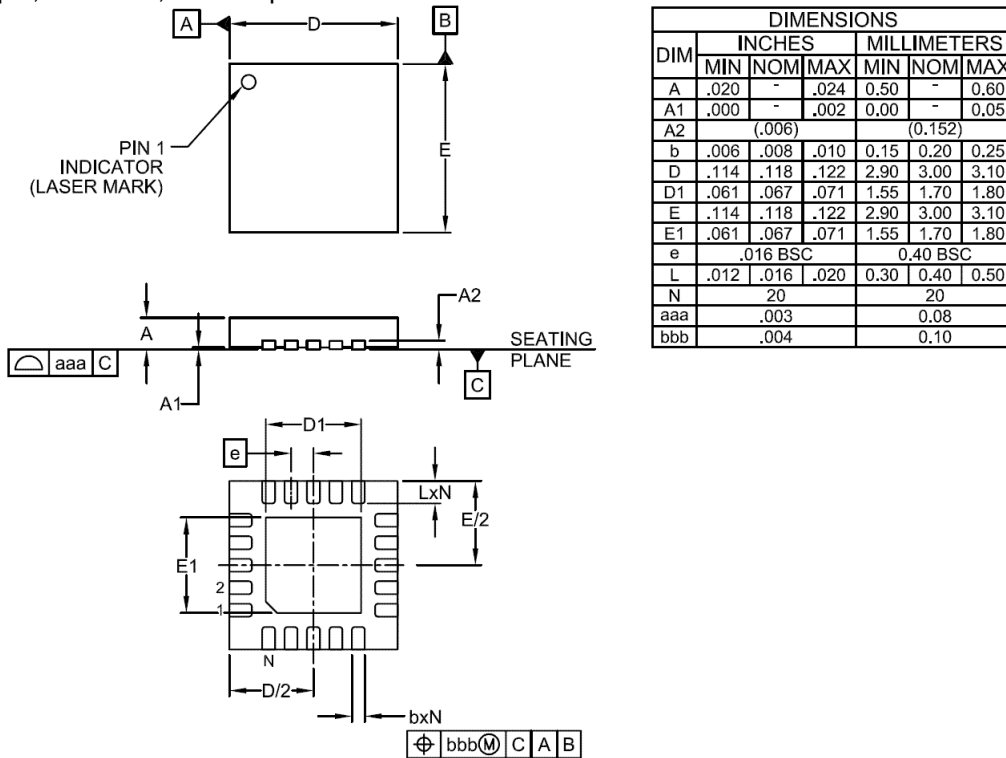
This can save significant BOM cost in a final application where only a few slow signals need to be level-shifted.

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7 PACKAGING INFORMATION

7.1 QFN-UT 20-pin Outline Drawing

QFN-UT 20-pin, 3 x 3 mm, 0.4 mm pitch

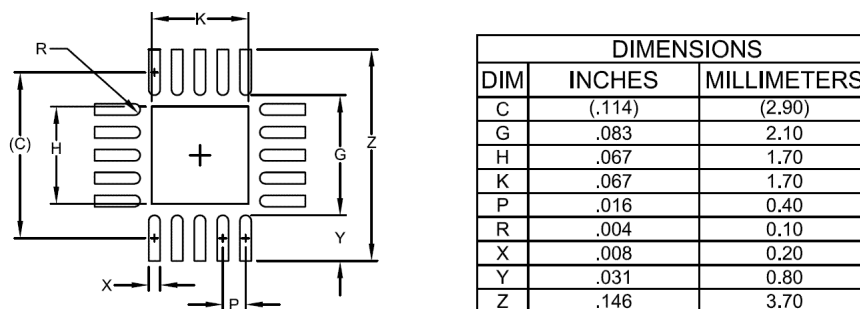


NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 1.90 x 1.90mm.

Figure 15 - Packaging Information – QFN-UT 20-pin Outline Drawing

7.2 QFN-UT 20-pin Land Pattern



NOTES:

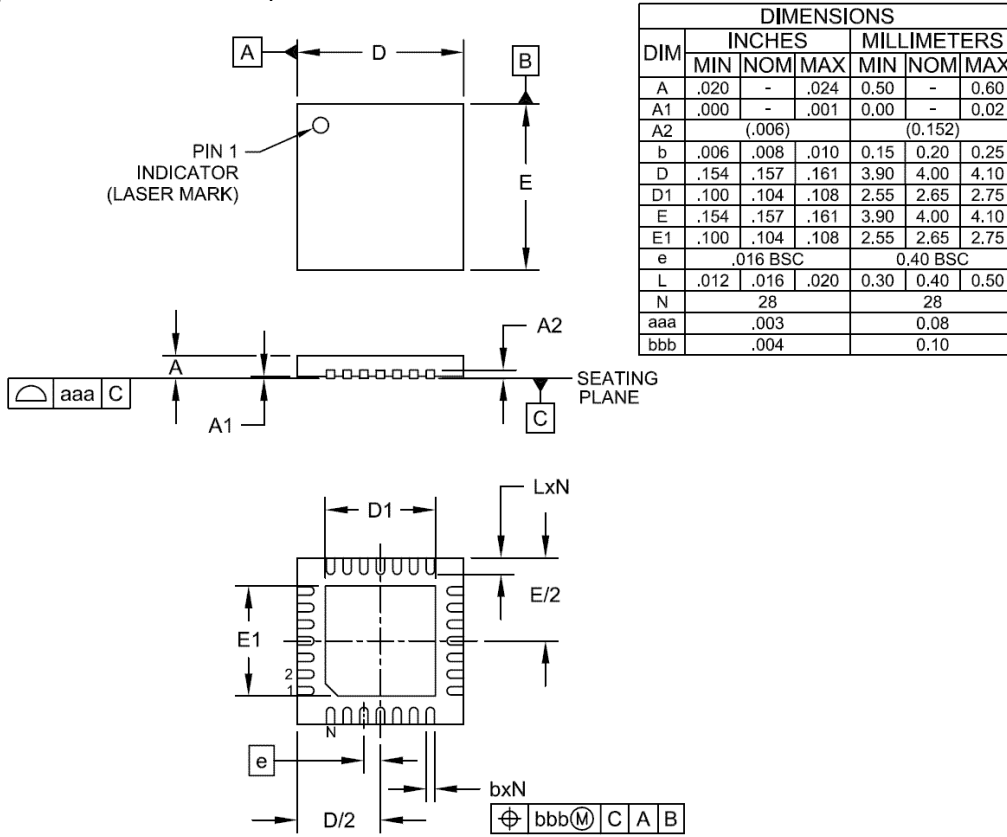
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Figure 16 - Packaging Information – QFN-UT 20-pin Land Pattern

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7.3 QFN-UT 28-pin Outline Drawing

QFN-UT 28-pin, 4 x 4 mm, 0.4 mm pitch

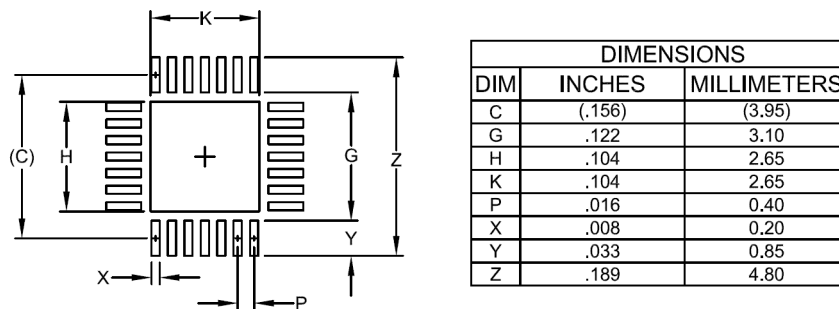


NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Figure 17 - Packaging Information – QFN-UT 28-pin Outline Drawing

7.4 QFN-UT 28-pin Land Pattern



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE-DIMENSIONS APPLY IN BOTH X AND Y DIRECTIONS.

Figure 18 - Packaging Information – QFN-UT 28-pin Land Pattern

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8 SOLDERING PROFILE

The soldering reflow profile for the SX1501, SX1502 and SX1503 is described in the standard IPC/JEDEC J-STD-020C. For detailed information please go to <http://www.jedec.org/download/search/jstd020c.pdf>

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|-------------------------|------------------|
| Average Ramp-Up Rate ($T_{s_{max}}$ to T_p) | 3 °C/second max. | 3° C/second max. |
| Preheat | | |
| - Temperature Min ($T_{s_{min}}$) | 100 °C | 150 °C |
| - Temperature Max ($T_{s_{max}}$) | 150 °C | 200 °C |
| - Time ($t_{s_{min}}$ to $t_{s_{max}}$) | 60-120 seconds | 60-180 seconds |
| Time maintained above: | | |
| - Temperature (T_L) | 183 °C | 217 °C |
| - Time (t_L) | 60-150 seconds | 60-150 seconds |
| Peak/Classification Temperature (T_p) | See Table 4.1 | See Table 4.2 |
| Time within 5 °C of actual Peak Temperature (t_p) | 10-30 seconds | 20-40 seconds |
| Ramp-Down Rate | 6 °C/second max. | 6 °C/second max. |
| Time 25 °C to Peak Temperature | 6 minutes max. | 8 minutes max. |

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

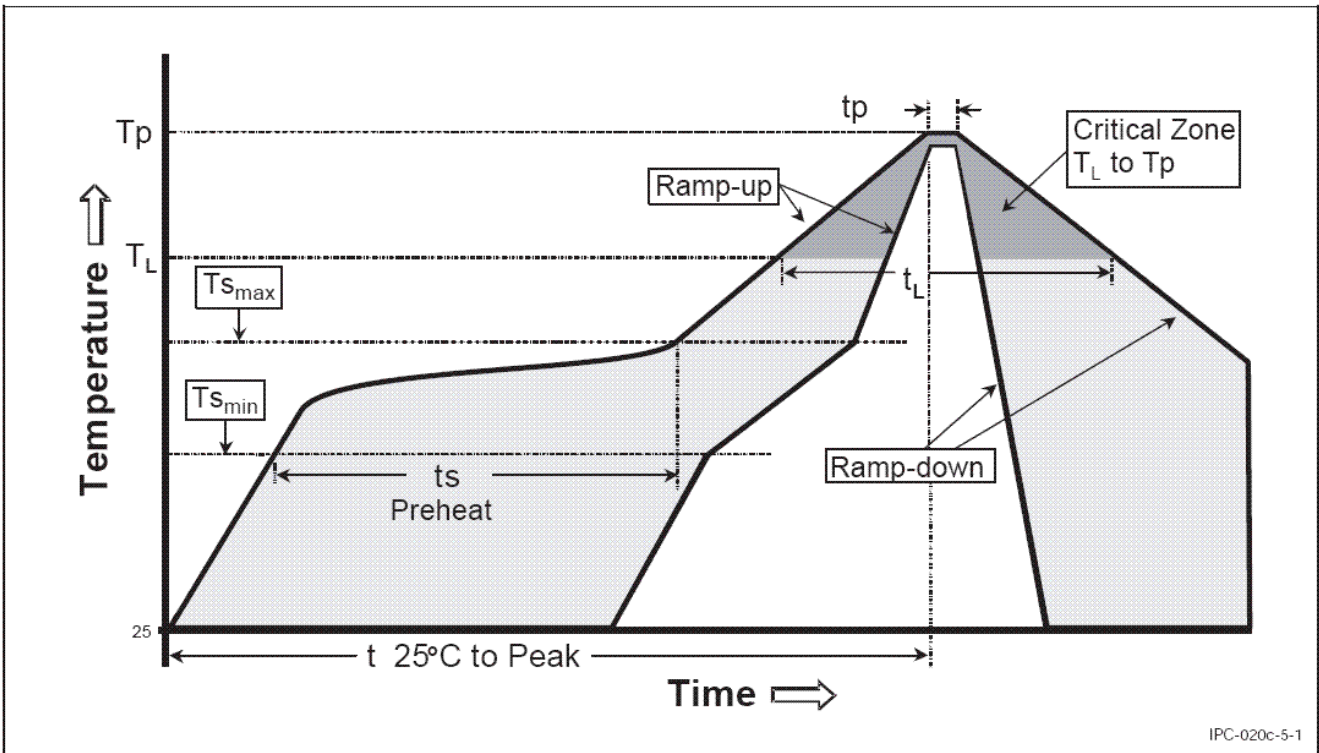


Figure 19 - Classification Reflow Profile (IPC/JEDEC J-STD-020C)

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