

## SX1701A – Datasheet

### Highly linear wideband LNA

### Single-channel, single-ended to differential conversion

#### GENERAL DESCRIPTION

The SX1701A is an integrated LNA operating over a wide frequency range from 40 MHz to 2.5 GHz. It is optimized for high OIP2 and OIP3 with minimum current consumption. It also performs a single-ended to differential conversion with 3 selectable gains.

#### APPLICATIONS

- Digital Set Top Boxes (Satellite and Terrestrial)
- CATV Distribution Systems
- Active Splitter
- Data Communications Systems
- Active Balun

#### KEY PRODUCT FEATURES

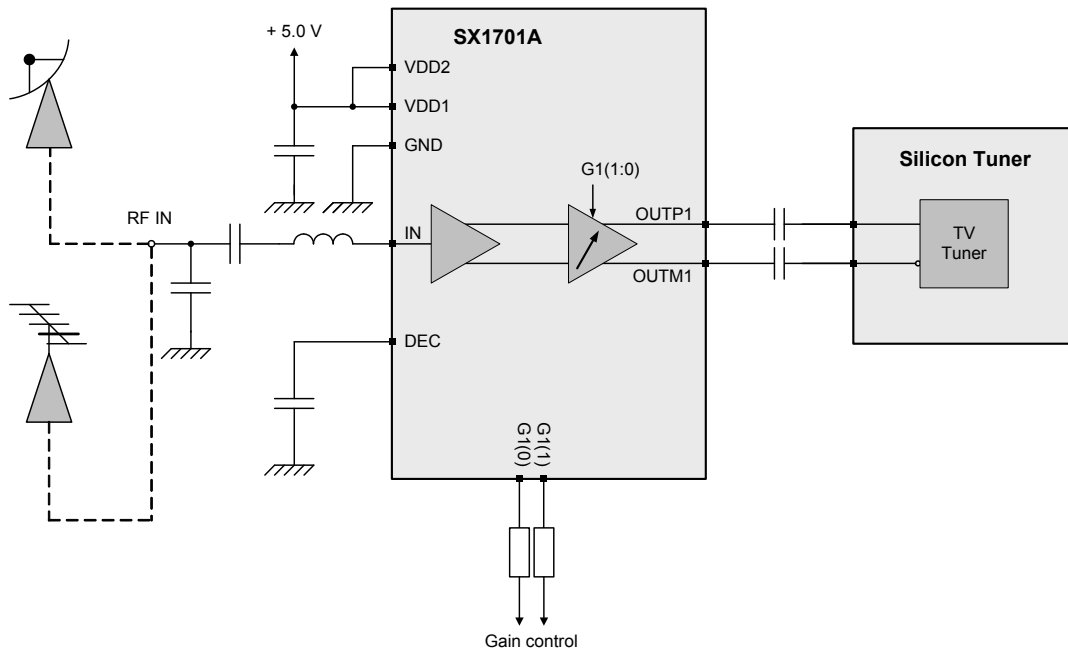
- Single-ended input / Differential outputs
- Programmable gain: 6, 12 and 18 dB
- High Linearity: OIP2 of 57 dBm and OIP3 of 22 dBm
- Noise Figure of 7 dB
- 75  $\Omega$  Input impedance
- 100  $\Omega$  differential output impedance
- Current consumption of 130 mA at maximum gain
- ESD protection (Normal ESD handling procedures should be observed)
- Very small package: MLPQ-16, 4 mm x 4 mm (equivalent to QFN-16, 4 mm x 4 mm)

#### ORDERING INFORMATION

Part number	Temperature range	Package
SX1701AI085TRT	-40 °C to +85 °C	Lead Free MLPQ-16

Note: This device is WEEE and RoHS compliant.

#### TYPICAL APPLICATION



**TABLE OF CONTENTS**

<b>1</b>	<b>Simplified Block Diagram</b> .....	<b>3</b>
<b>2</b>	<b>Pin Description</b> .....	<b>4</b>
2.1.1	Pin Connections .....	4
2.1.2	Gain Control Pins .....	4
<b>3</b>	<b>Electrical Characteristics</b> .....	<b>5</b>
3.1	Absolute Maximum Ratings .....	5
3.2	Specifications .....	5
3.2.1	Operating Range.....	5
3.2.2	Electrical Specifications .....	6
3.3	Typical Operating Characteristics.....	7
<b>4</b>	<b>Application Information</b> .....	<b>9</b>
<b>5</b>	<b>Application Example with Single-Ended Outputs</b> .....	<b>10</b>
5.1	75 $\Omega$ Single-Ended Input to Dual 50 $\Omega$ Single-Ended Outputs (Active Splitter) .....	10
<b>6</b>	<b>Package Outline Drawing</b> .....	<b>11</b>
<b>7</b>	<b>Marking Information</b> .....	<b>11</b>
<b>8</b>	<b>Land Pattern Drawing</b> .....	<b>12</b>

## 1 SIMPLIFIED BLOCK DIAGRAM

The simplified block diagram of the SX1701A is illustrated below in Figure 1.

The amplifier comprises two main stages. The first stage performs the single-ended to differential conversion. The second stage is implemented with two cascaded stages and performs the gain control.

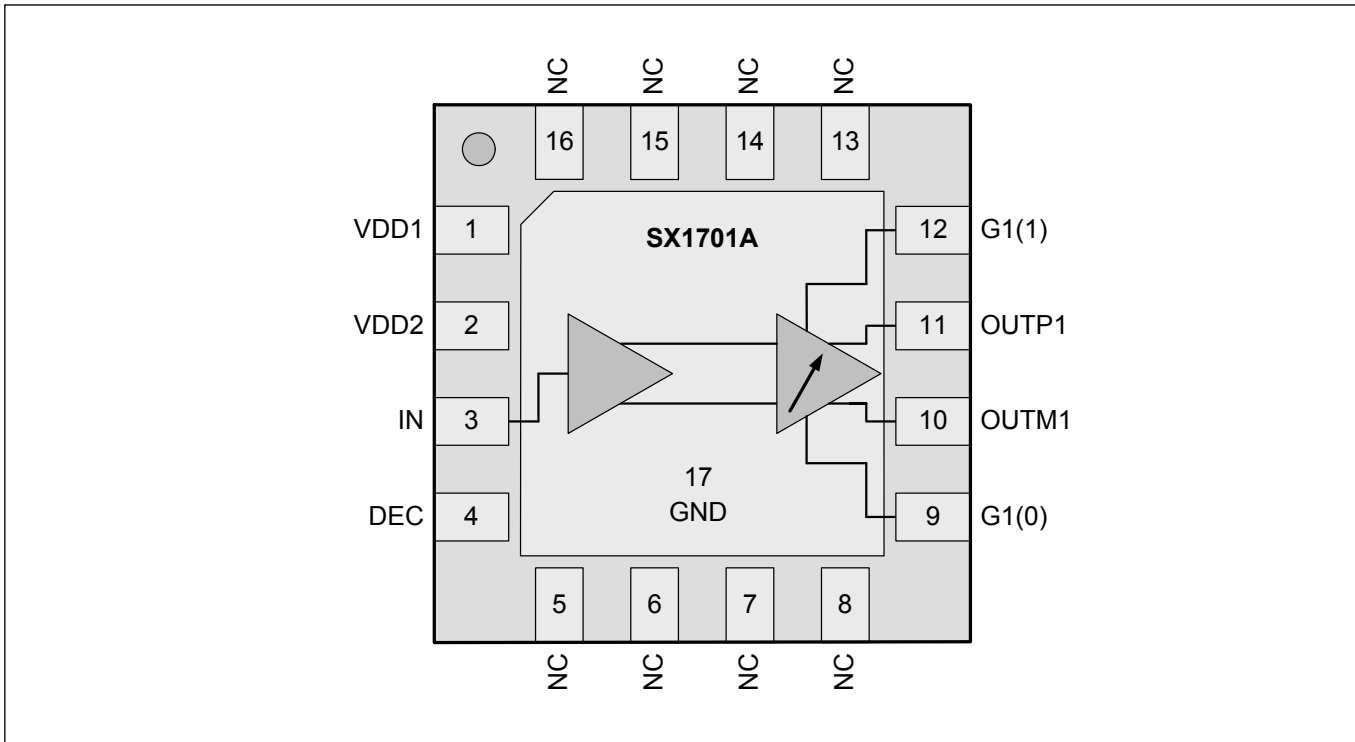


Figure 1. Simplified block diagram of the SX1701A.

## 2 PIN DESCRIPTION

### 2.1.1 Pin Connections

The pin description of the SX1701A is given in Table 1.

Number	Name	Type	Description
1	VDD1	Input	Supply voltage
2	VDD2	Input	Supply voltage
3	IN	Input	LNA input
4	DEC	Input	Decoupling capacitor
5	NC	None	No Connect
6	NC	None	No Connect
7	NC	None	No Connect
8	NC	None	No Connect
9	G1(0)	Input	Gain Control 0
10	OUTM1	Output	Differential output -
11	OUTP1	Output	Differential output +
12	G1(1)	Input	Gain Control 1
13	NC	None	No Connect
14	NC	None	No Connect
15	NC	None	No Connect
16	NC	None	No Connect
17	GND	Input	Ground pad

Table 1. Pin description.

### 2.1.2 Gain Control Pins

The gain setting for each channel is given in Table 2.

G1(1:0)	Description
0 0	Channel OFF (default value set by pull-down devices)
0 1	Channel ON, G = 6 dB
1 0	Channel ON, G = 12 dB
1 1	Channel ON, G = 18 dB

Table 2. Channel gain setting.

### 3 ELECTRICAL CHARACTERISTICS

#### 3.1 ABSOLUTE MAXIMUM RATINGS

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Description	Min.	Max.	Unit
VDDmr	Supply voltage	-0.5	5.5	V
Tmr	Storage temperature	-55	+125	°C
Tjmr	Junction Temperature	-	+125	°C
Pmr	Input level	-	0	dBm

Table 3. Absolute Maximum ratings.

#### 3.2 SPECIFICATIONS

##### 3.2.1 Operating Range

Symbol	Description	Min.	Max.	Unit
VDDop	Supply voltage	4.5	5.3	V
Trop	Temperature	-40	+85	°C

Table 4. Operating Range.

### 3.2.2 Electrical Specifications

The table below gives the electrical specifications of the LNA under the following conditions:

VDD = 5.0 V, Temperature = 25 °C, Input frequency = 1 GHz, Gain = 18 dB, Pin = -20dBm, unless otherwise specified.

Symbol	Description	Condition	Min	Typ	Max	Unit	
RIN	Input impedance	Single-ended	-	75	-	Ω	
ROUT	Output impedance	Differential	-	100	-	Ω	
FR	Frequency range		0.04	-	2.5	GHz	
G	Gain	S <sub>21</sub>	-	6	-	dB	
		Programmable	-	12	-		
			-	18	-		
GFLAT	Gain Flatness	Rs = 75 Ω, maximum gain	-	±1	-	dB	
NF	Noise figure	Rs = 75 Ω	G = 18 dB	-	7	-	dB
			G = 12 dB	-	9	-	
			G = 6 dB	-	13	-	
P1dB	Output P1dB compression point		-	13	-	dBm	
OIP3	Output 3 <sup>rd</sup> order intermodulation (differential)	f <sub>1</sub> = 1.0 GHz	G = 18 dB	-	22	-	dBm
		f <sub>2</sub> = 1.1 GHz	G = 12 dB	-	21	-	
			G = 6 dB	-	19	-	
OIP2	Output 2 <sup>nd</sup> order intermodulation (differential)	f <sub>1</sub> = 1.0 GHz	@ f <sub>1</sub> + f <sub>2</sub>	-	53	-	dBm
		f <sub>2</sub> = 1.1 GHz	@ f <sub>2</sub> - f <sub>1</sub>	-	57	-	
IDD	Current consumption	1 channel enabled		-	130	-	mA
		2 channels enabled		-	200	-	
		3 channels enabled		-	270	-	
IRL	Input Return loss	-20.log( s <sub>11</sub>  )	-	15		dB	
ORL	Output Return loss	-20.log( s <sub>i1</sub>  )	-	20		dB	
ISOUTIN	RF out to RF in Isolation	-20.log( s <sub>11</sub>  )	50	-	-	dB	
ISOUTDWN	RF in to RF out isolation in shut down mode	-20.log( s <sub>i1</sub>  )	-	50	-	dB	
CMRR	Common mode rejection at the output		-	20	-	dB	
VESD	ESD robustness on all pins	HBM	3	-	-	kV	

Table 5. Electrical Specifications.

### 3.3 TYPICAL OPERATING CHARACTERISTICS

The curves below give the typical RF performances of the LNA under the following conditions:

VDD = 5.0 V, Temperature = 25 °C,  $Z_{Source} = 75\Omega$ ,  $Z_{Load} = 100\Omega$  differential, Frequency range = 40 MHz to 2.5 GHz, input matching network according to application schematics of figure 4.

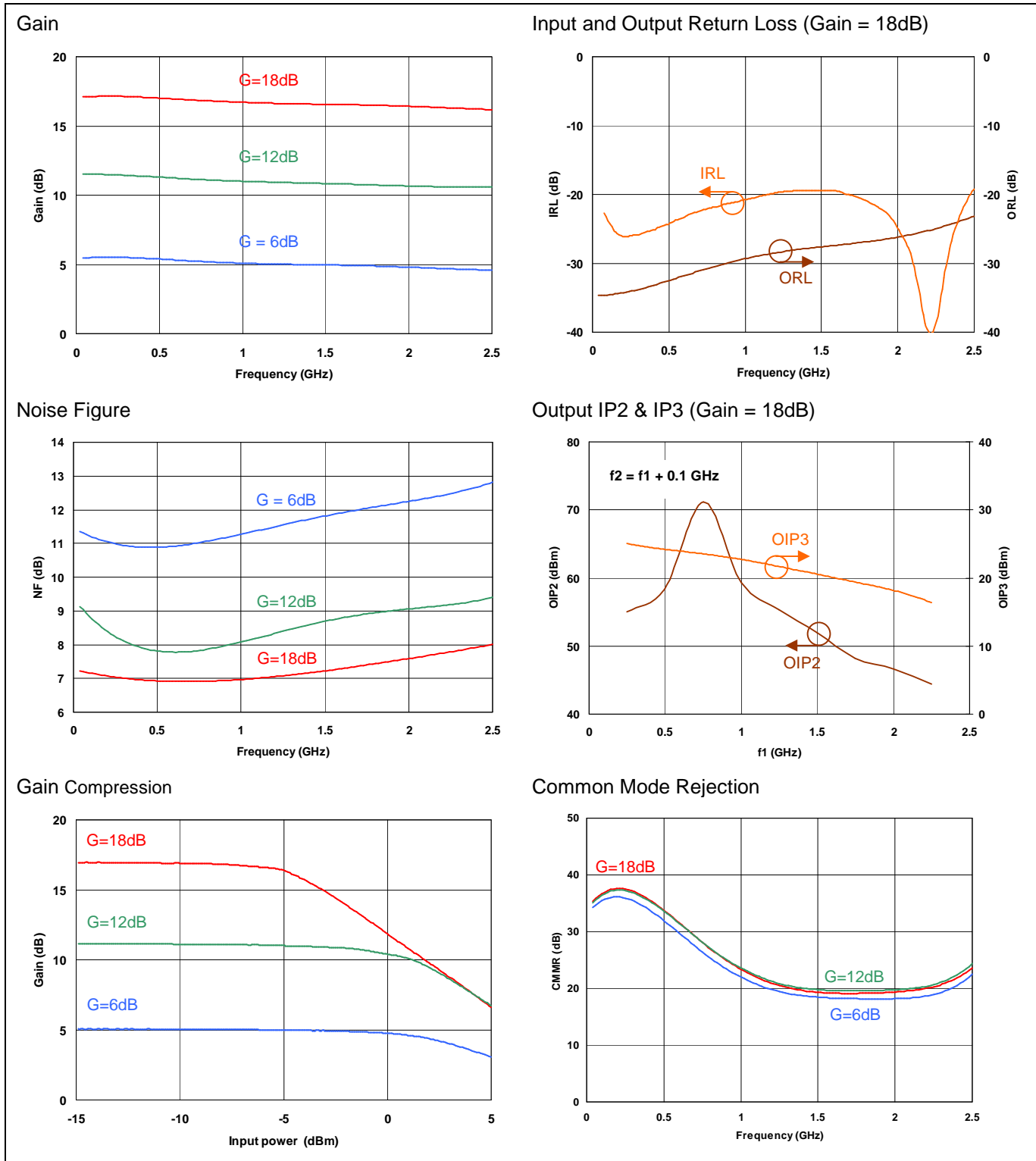


Figure 2. Typical Operating Characteristics Curves.

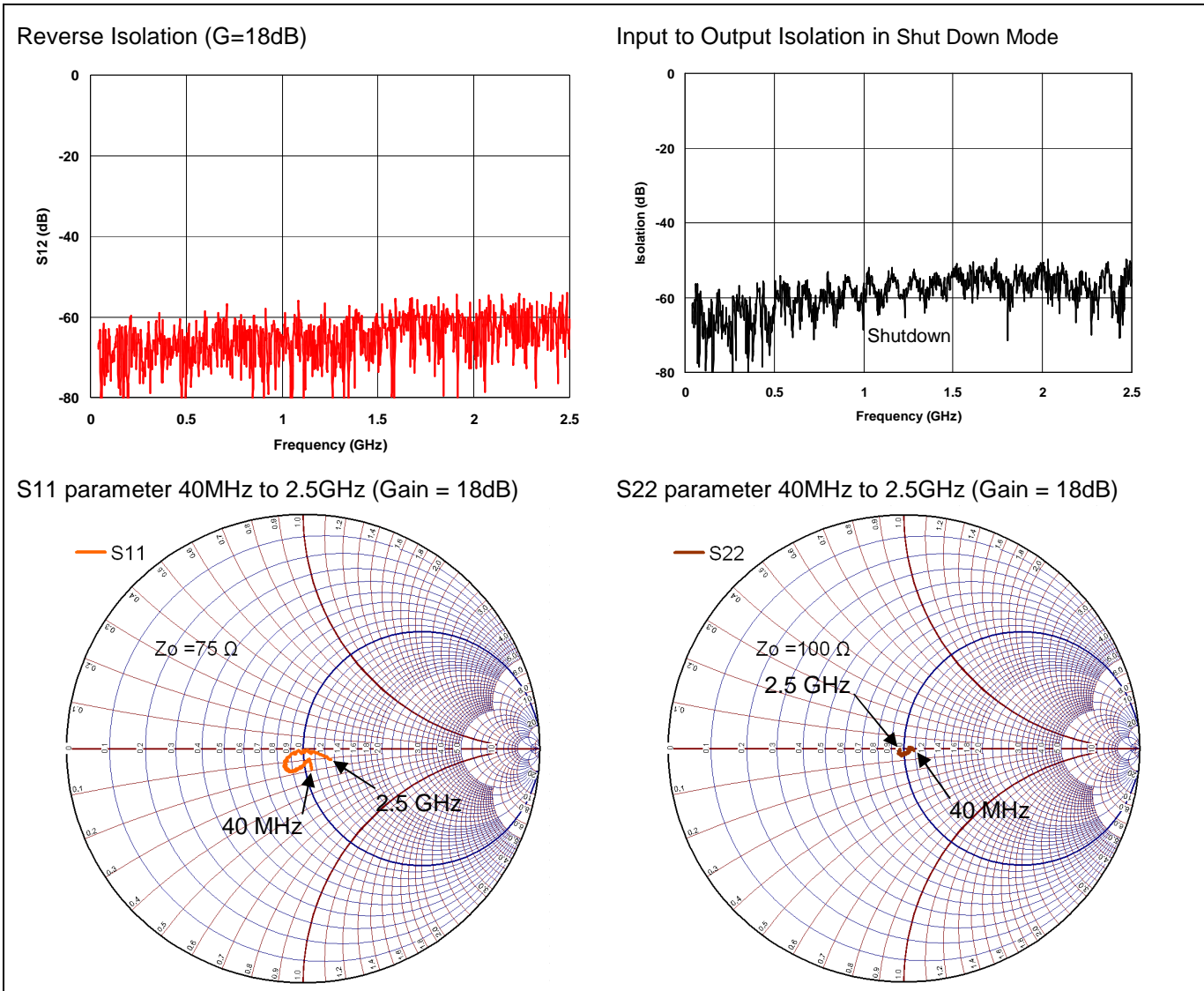


Figure 3. Typical Operating Characteristics Curves.



#### 4 APPLICATION INFORMATION

Figure 4, below, shows the recommended board schematic. Typical component values are shown and are subject to change depending on the PCB layout and material used. Please refer to the Semtech SX1701A reference design at [www.semtech.com](http://www.semtech.com).

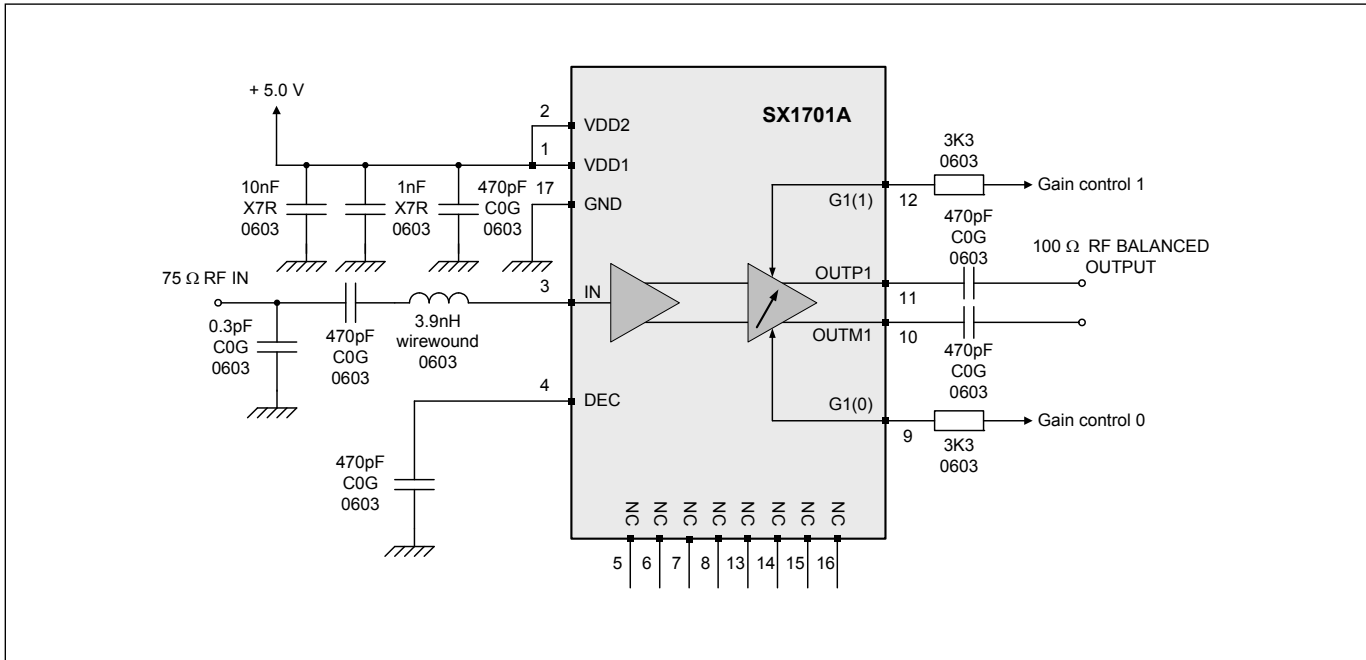


Figure 4. Application board schematic.

## 5 APPLICATION EXAMPLE WITH SINGLE-ENDED OUTPUTS

Although intended for differential output operation, the SX1701A may be used in the single-ended outputs configuration of Figure 5. Note that some degradation in device performance may be experienced, including a 3 dB reduction in power gain.

### 5.1 75 Ω SINGLE-ENDED INPUT TO DUAL 50 Ω SINGLE-ENDED OUTPUTS (ACTIVE SPLITTER)

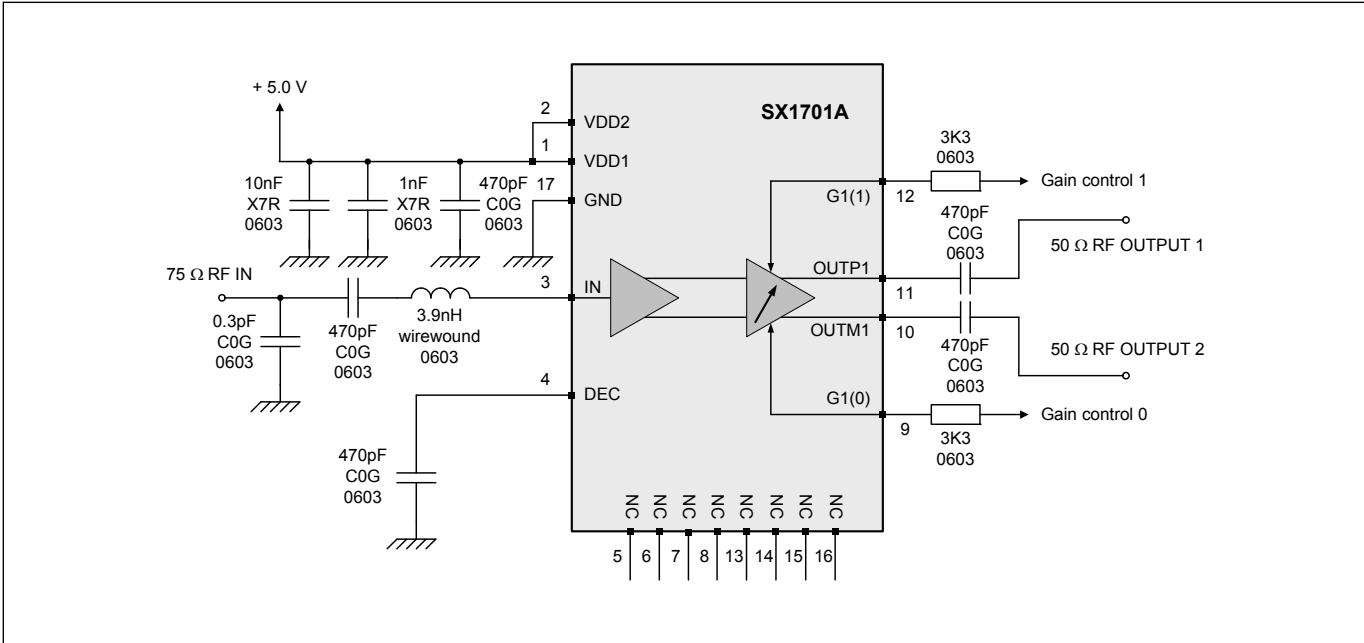


Figure 5. Active balun application example.

## 6 PACKAGE OUTLINE DRAWING

SX1701A is assembled in a MLPQ-16, 4 mm x 4 mm as shown in Figure 6.

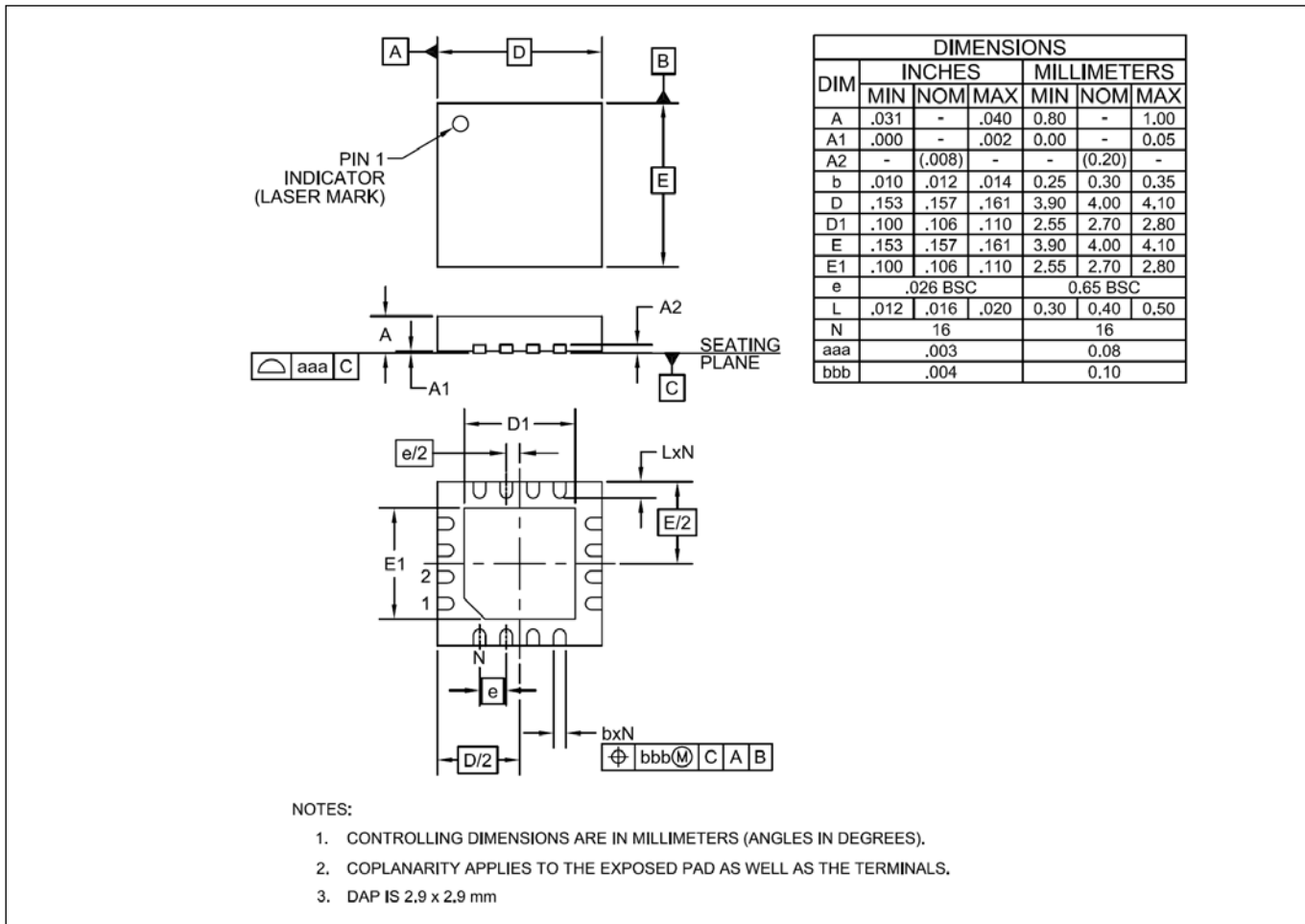


Figure 6. Package outline drawing.

## 7 MARKING INFORMATION



Figure 7. Marking information.

## 8 LAND PATTERN DRAWING

The land pattern of MLPQ-16 package, 4 mm x 4 mm is shown in Figure 8.

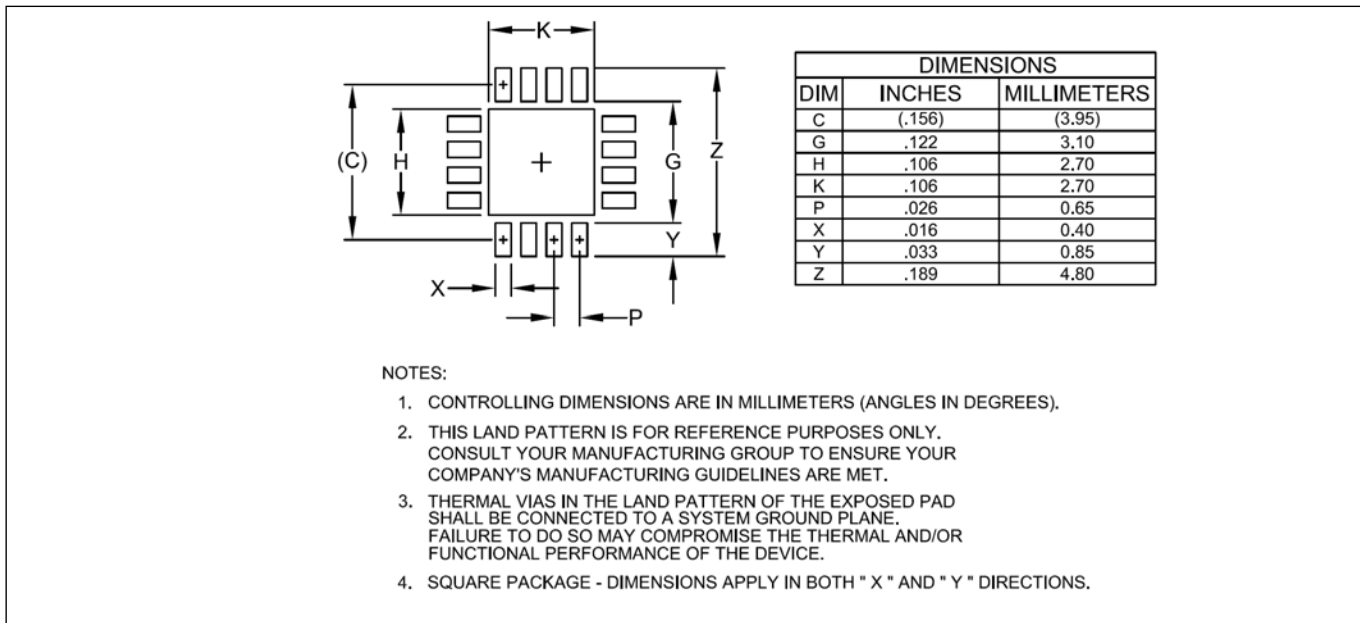


Figure 8. Land pattern drawing.

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