1 Product Overview

1.1 Features

- ESD / transient protection of high speed data lines according to:
  - **IEC61000-4-2 (ESD): ±16 kV (air/contact discharge)**
  - **IEC61000-4-4 (EFT): ±2kV / ±40 A (5/50 ns)**
  - **IEC61000-4-5 (surge): ±3 A (8/20 µs)**
- Bi-directional working voltage up to: V_{RWM} **= ±5.5 V**
- Line capacitance: C_L **=7pF (typical) at** f **= 1 MHz**
- Clamping voltage: V_{CL} **= 13 V (typical) at** I_{TLP} **= 16 A** with R_{DYN} **= 0.22 Ω (typical)**
- Very low reverse current: I_R **< 1 nA (typical)**
- Minimized clamping overshoot due to extremely low parasitic inductance
- Small form factor SMD Size 0201 and low profile (0.58 mm x 0.28 mm x 0.15 mm)
- Bidirectional and symmetric I/V characteristics for optimized design and assembly
- Pb-free (RoHS compliant) and halogen free package

Guidelines for optimized PCB design and assembly process available [2]

1.2 Application Examples

- ESD Protection of highly susceptible IC/ASICs in audio, headset, human digital interfaces
- Dedicated solution to boost space saving and high performance in miniaturized modern electronics

1.3 Product Description

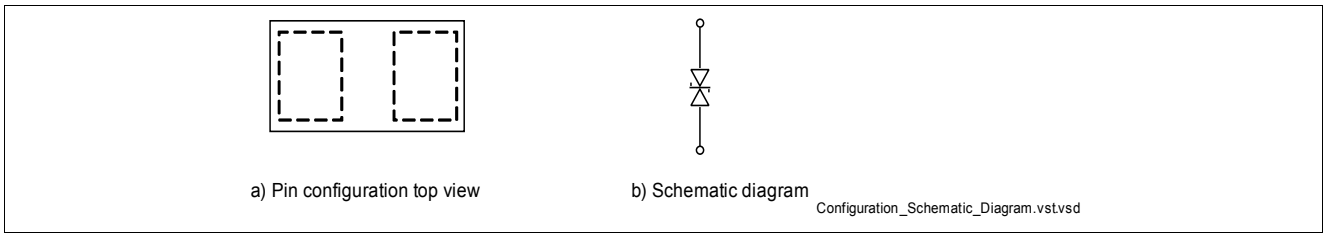

Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Part Information

Type	Package	Configuration
SXESD230V05A	WLL-2-1	1 line, bi-directional

1) The device does not have any marking or date code on the device backside. The Marking code is on pad side.

2 Maximum Ratings

Table 2-1 Maximum Ratings at T_A = 25 °C, unless otherwise specified [1)]

Parameter	Symbol	Values	Unit
Reverse working voltage	V_{RWM}	±5.5	V
ESD (air / contact) discharge[2)]	V_{ESD}	±16	kV
Peak pulse power[3)]	P_{PK}	56	W
Peak pulse current[3)]	I_{PP}	±3	A
Operating temperature range	T_{OP}	-55 to 125	°C
Storage temperature	T_{stg}	-65 to 150	°C

1) Device is electrically symmetrical
2) V_{ESD} according to IEC61000-4-2 (R = 330 Ω, C = 150 pF discharge network)
3) Stress pulse: 8/20µs current waveform according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3 Electrical Characteristics

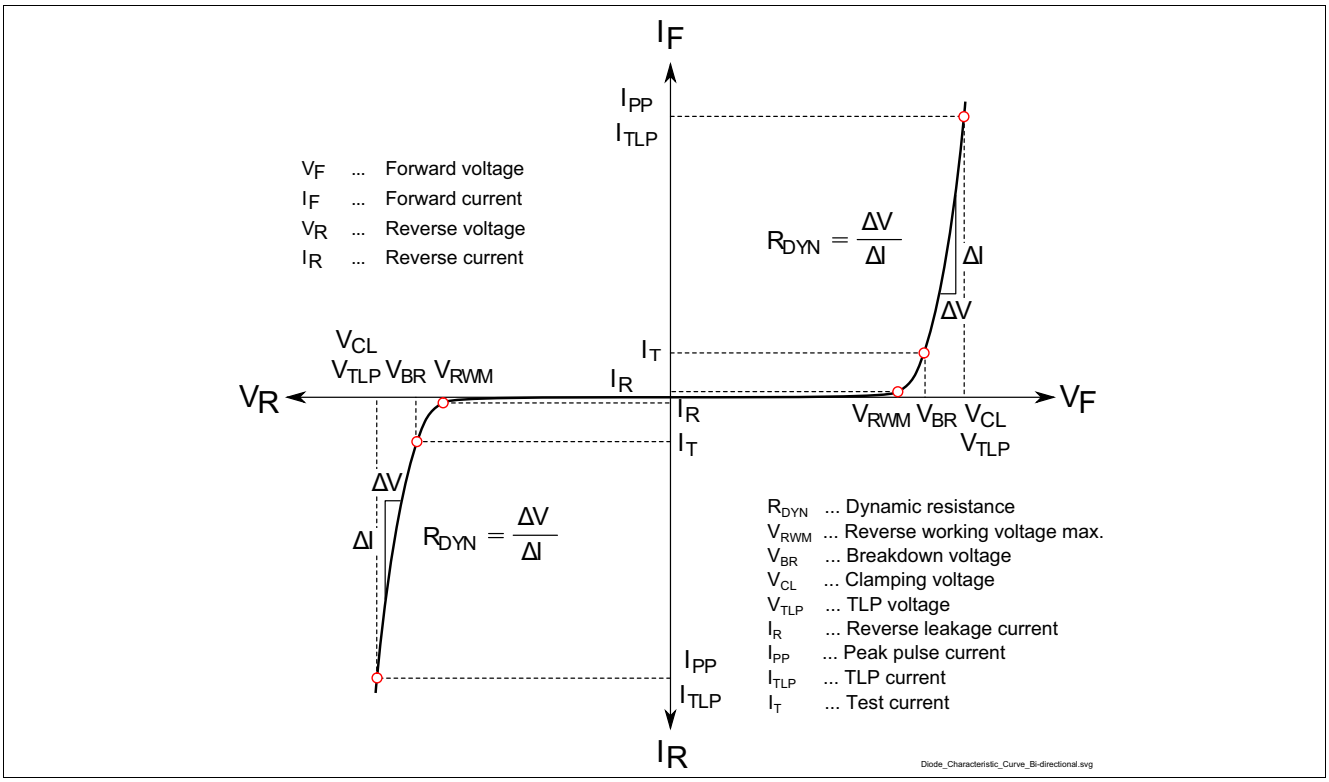

Figure 3-1 Definitions of electrical characteristics

Table 3-1 DC Characteristics at T_A = 25 °C, unless otherwise specified [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Breakdown voltage	V_{BR}	6.05	8	–	V	I_T = 1 mA
Reverse current	I_R	–	–	100	nA	V_R = 5.5 V

1) Device is electrically symmetrical

Table 3-2 RF Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	_	7	11	pF	V_R = 0 V, f = 1 MHz
		_	11		pF	V_R = 0 V, f = 1 GHz

Table 3-3 ESD and Surge Characteristics at T_A = 25 °C, unless otherwise specified[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage[2)]	V_{CL}	-	-	10.5	V	I_{TLP} = 1 A, t_p = 100 ns
		-	-	15		I_{TLP} = 16 A, t_p = 100 ns
Clamping voltage[3)]		-	-	11.3		I_{PP} = 1 A, t_p = 8/20 µs
		-	-	14		I_{PP} = 3 A, t_p = 8/20 µs
Dynamic resistance[2)]	R_{DYN}	-	0.22	-	Ω	t_p = 100 ns

1) Device is electrically symmetrical
2) Please refer to Application Note AN210[1]. TLP parameter: Z_0 = 50 Ω , t_p = 100ns, t_r = 0.6 ns.
3) Stress pulse: 8/20µs current waveform according to IEC61000-4-5

4 Typical Characteristics Diagrams

Typical characteristics diagrams at T_A = 25°C, unless otherwise specified

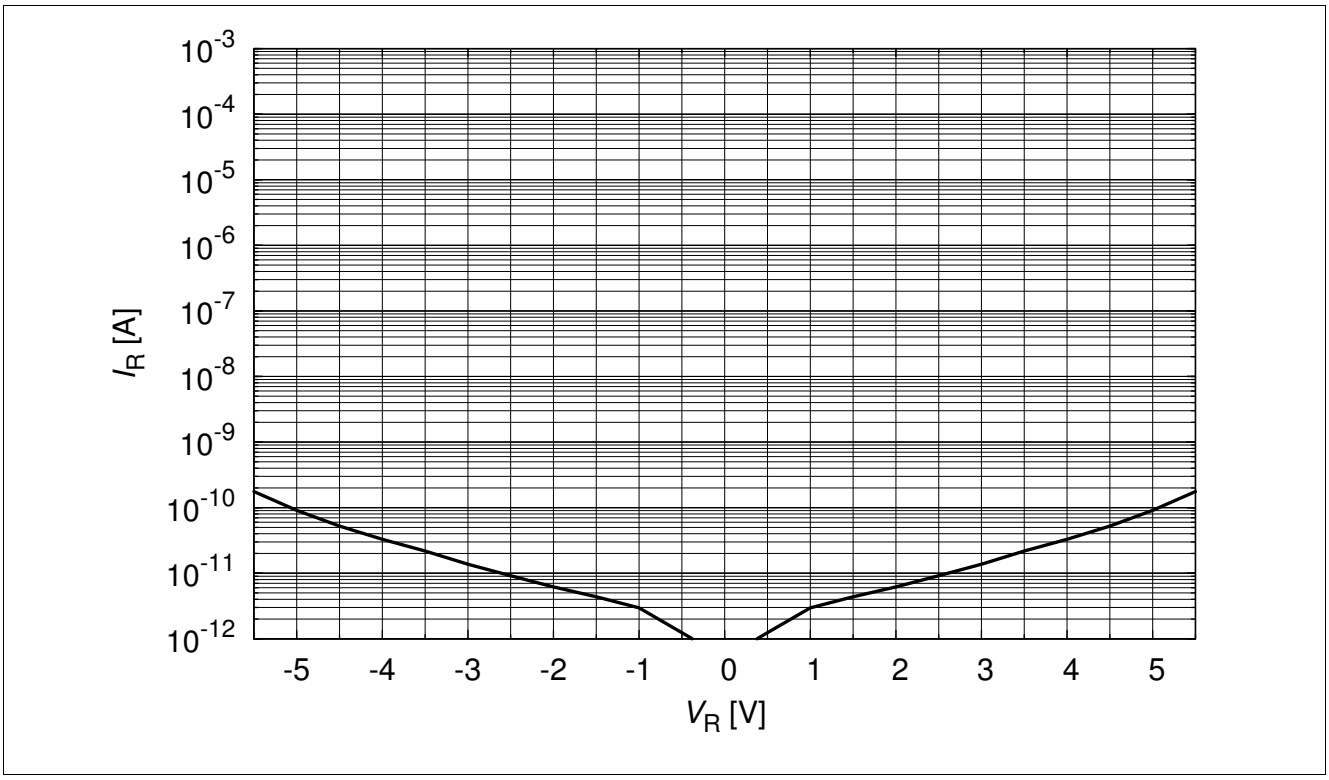

Figure 4-1 Reverse leakage current: $I_R = f(V_R)$

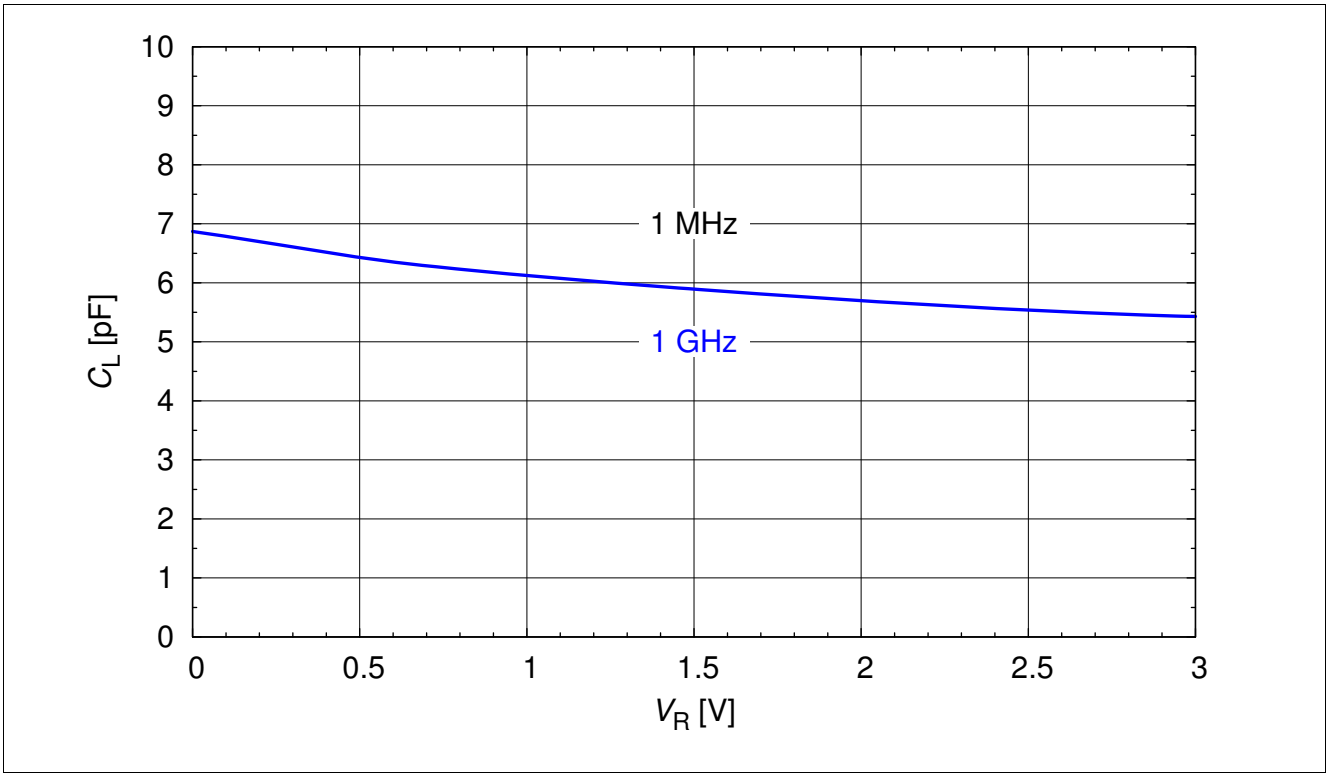

Figure 4-2 Line capacitance: $C_L = f(V_R)$

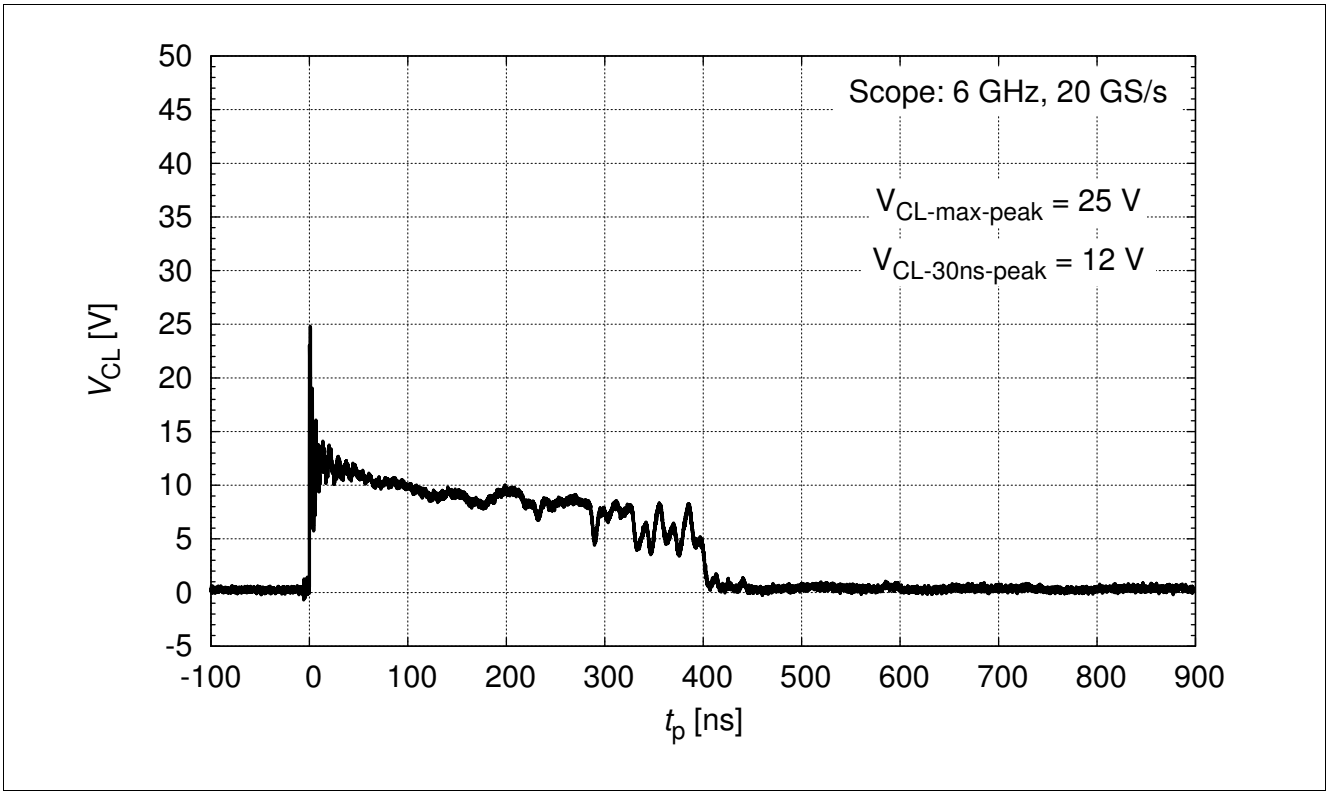

Figure 4-3 Clamping voltage (ESD): V_{CL} = $f(t)$, 8 kV positive pulse

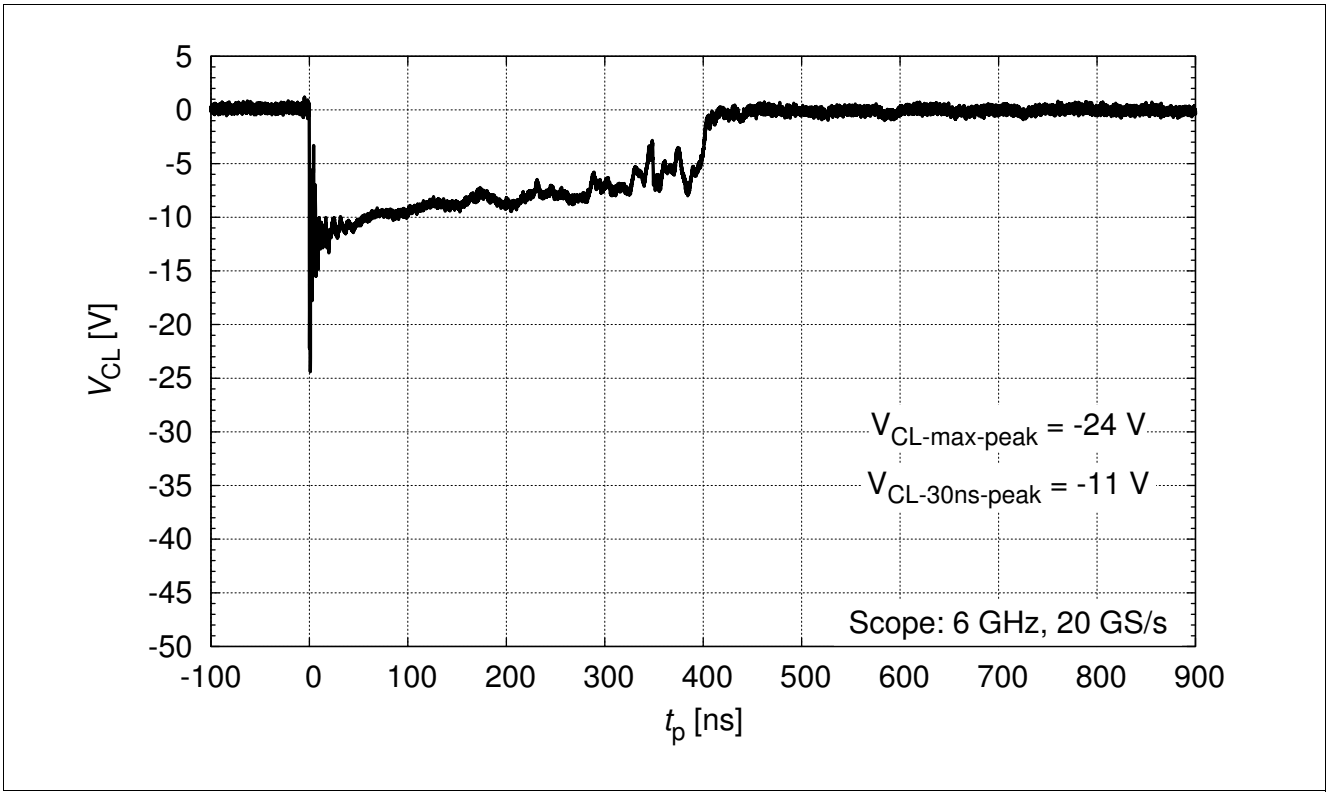

Figure 4-4 Clamping voltage (ESD) V_{CL} = $f(t)$, 8 kV negative pulse

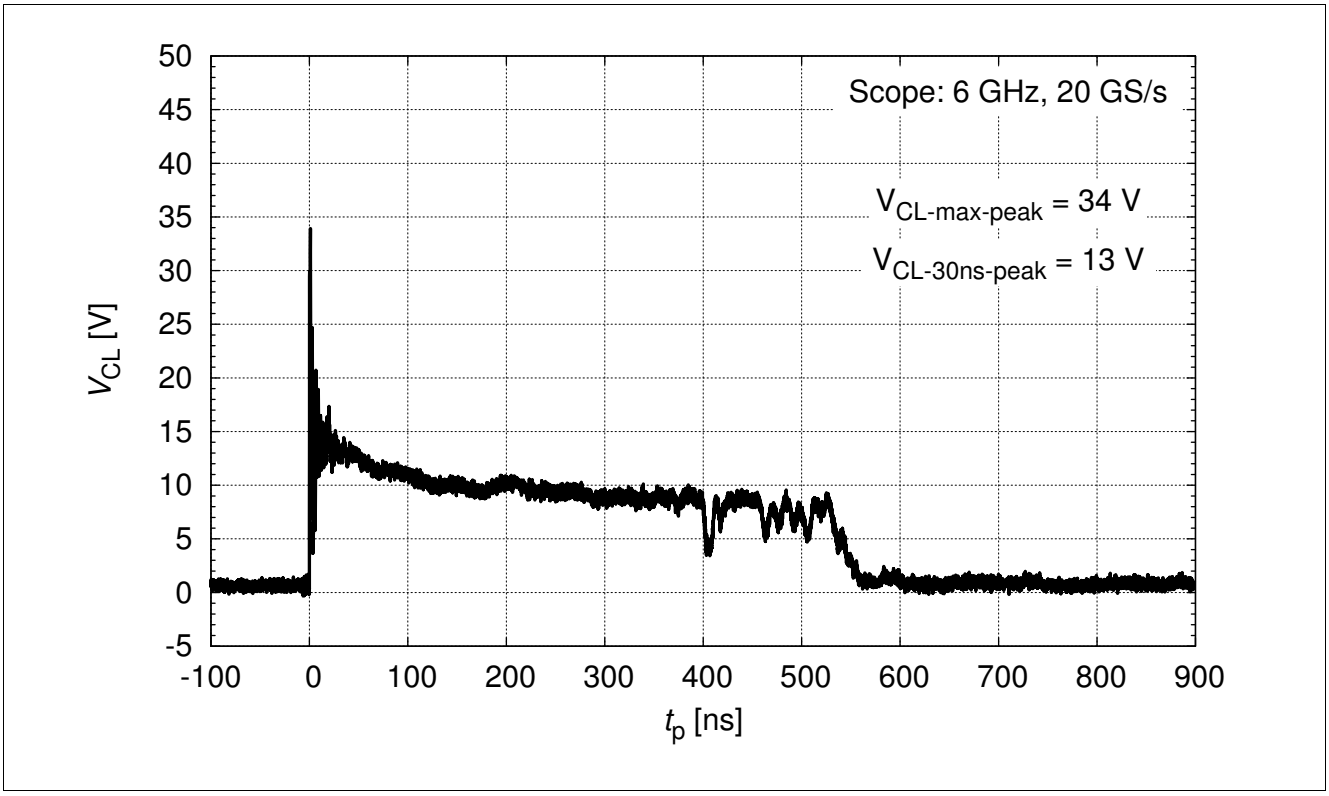

Figure 4-5 Clamping voltage (ESD) $V_{CL} = f(t)$, 15 kV positive pulse

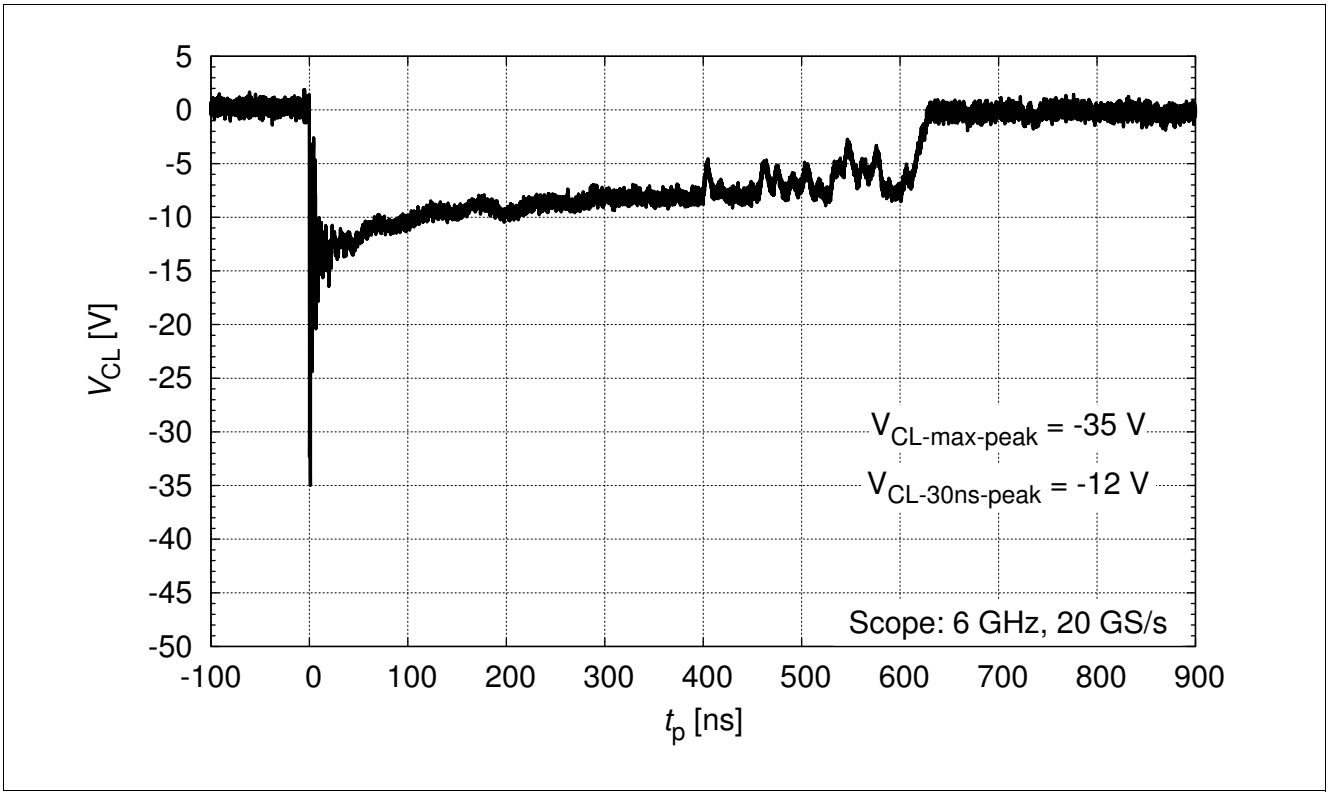

Figure 4-6 Clamping voltage (ESD) $V_{CL} = f(t)$, 15 kV negative pulse

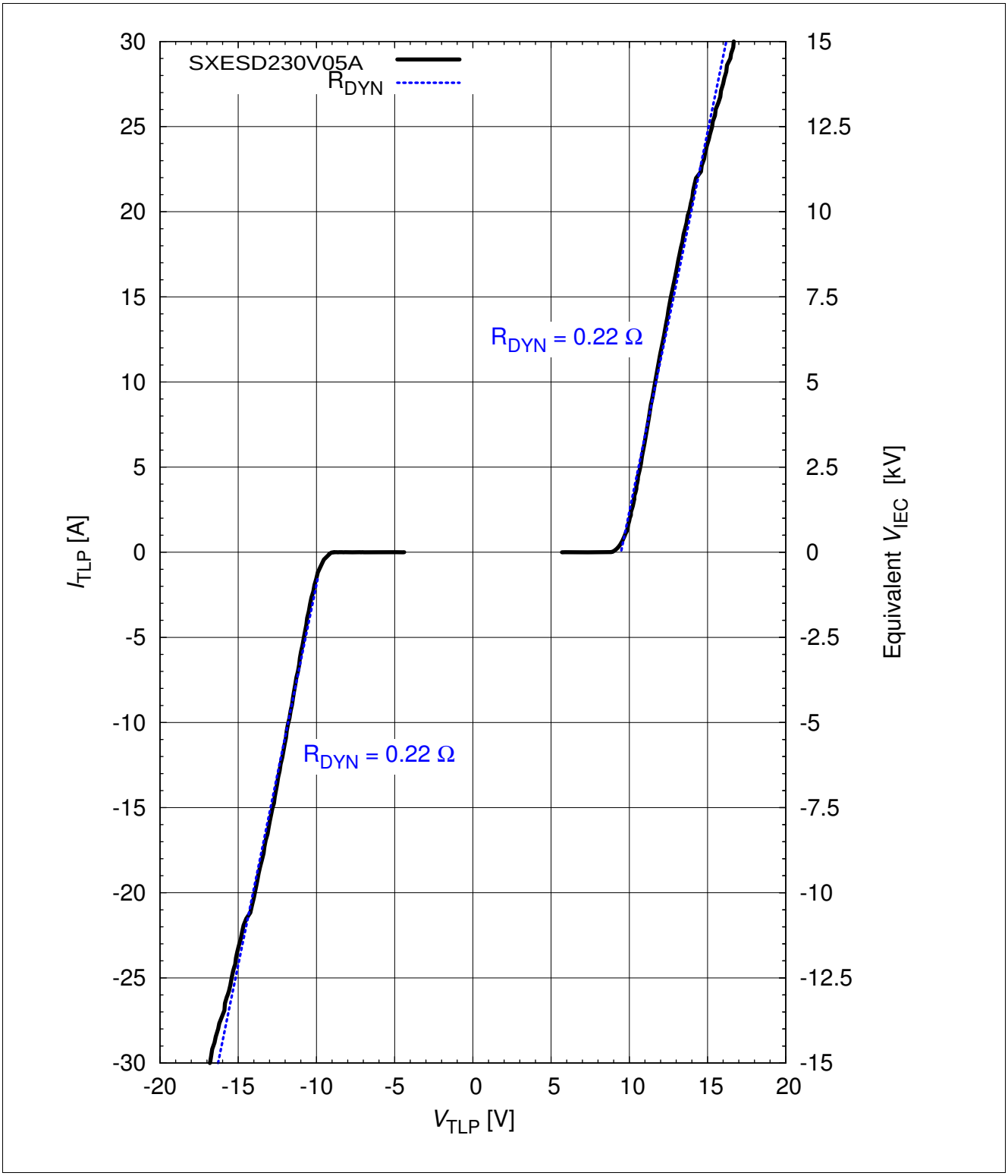

Figure 4-7 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$[1]

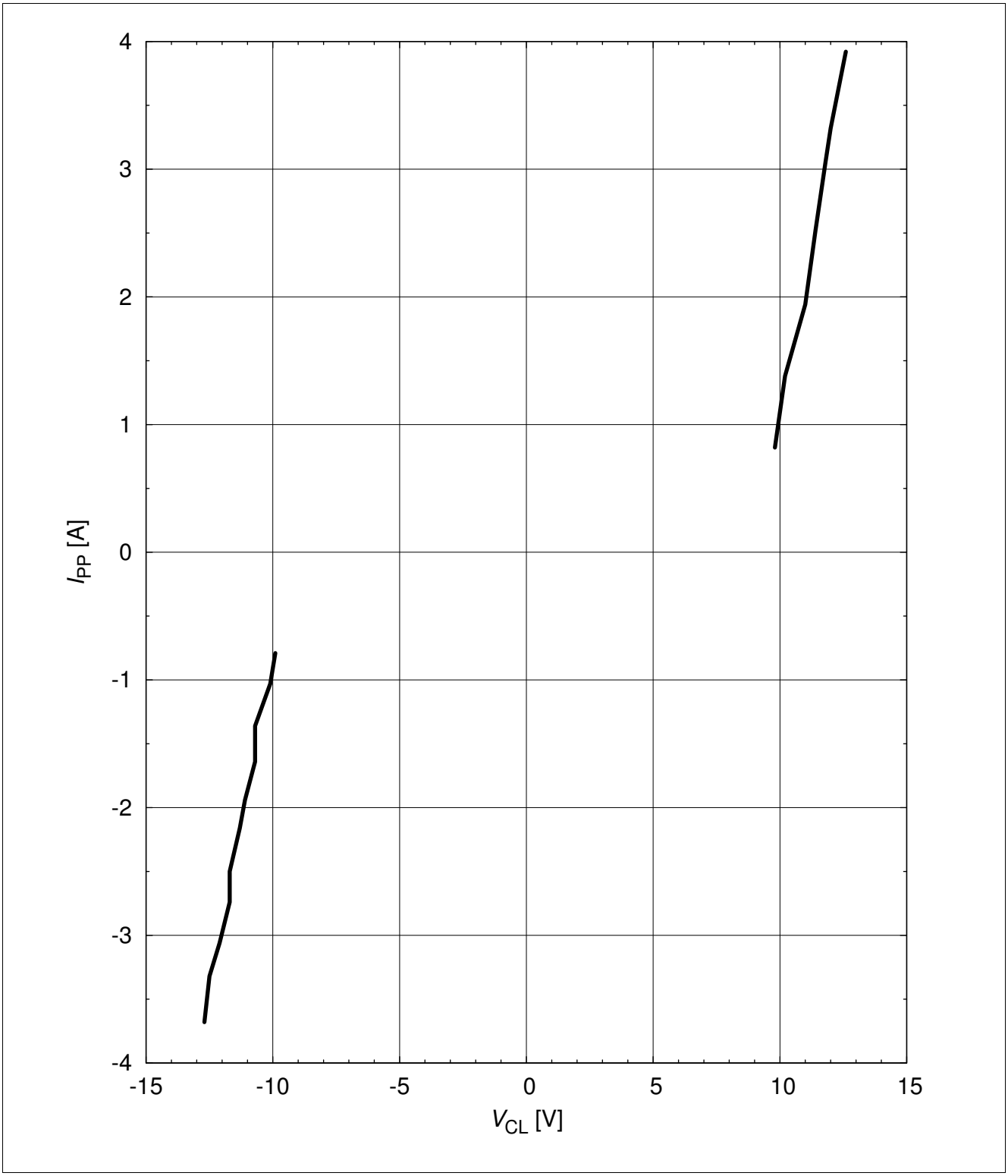

Figure 4-8 Clamping voltage (Surge): $I_{PP} = f(V_{CL})$[1]

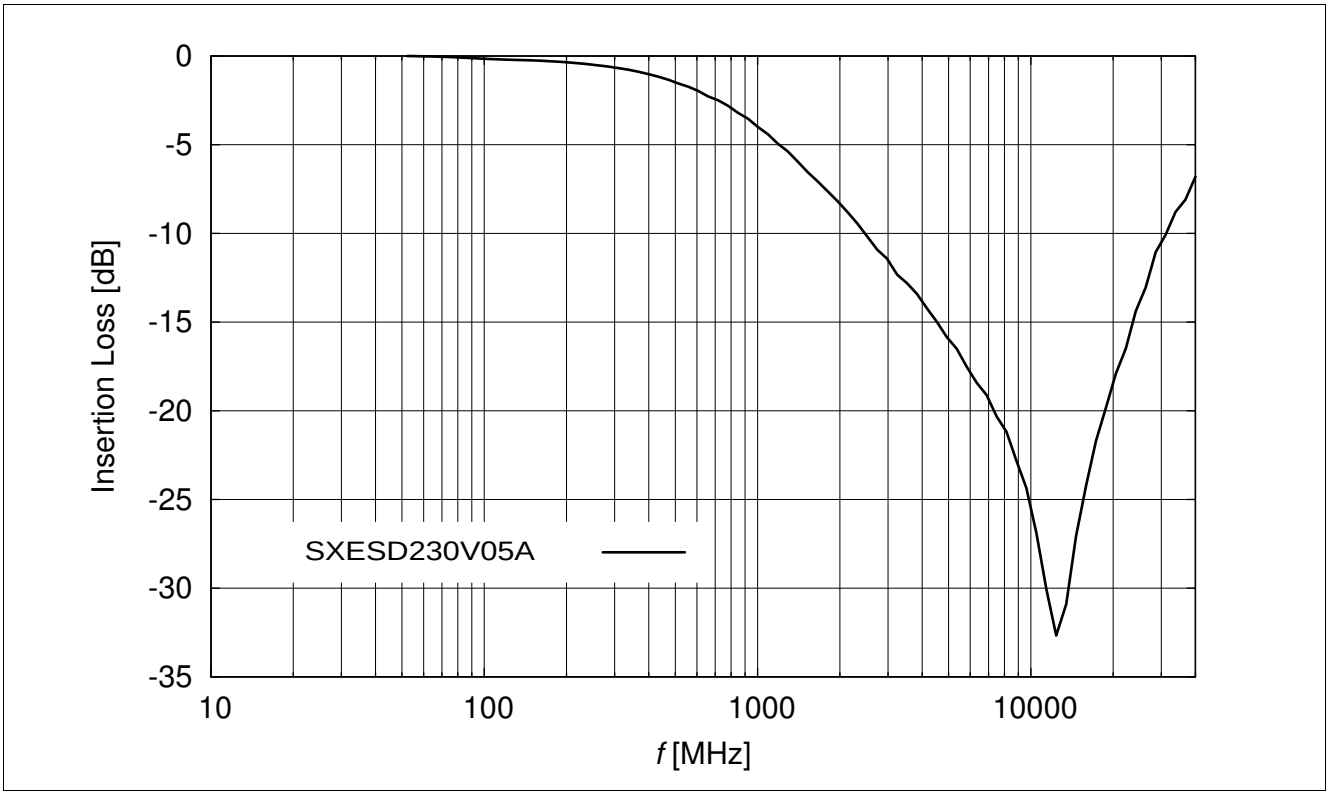

Figure 4-9 Insertion loss vs. frequency in a 50 Ω system

5 Package

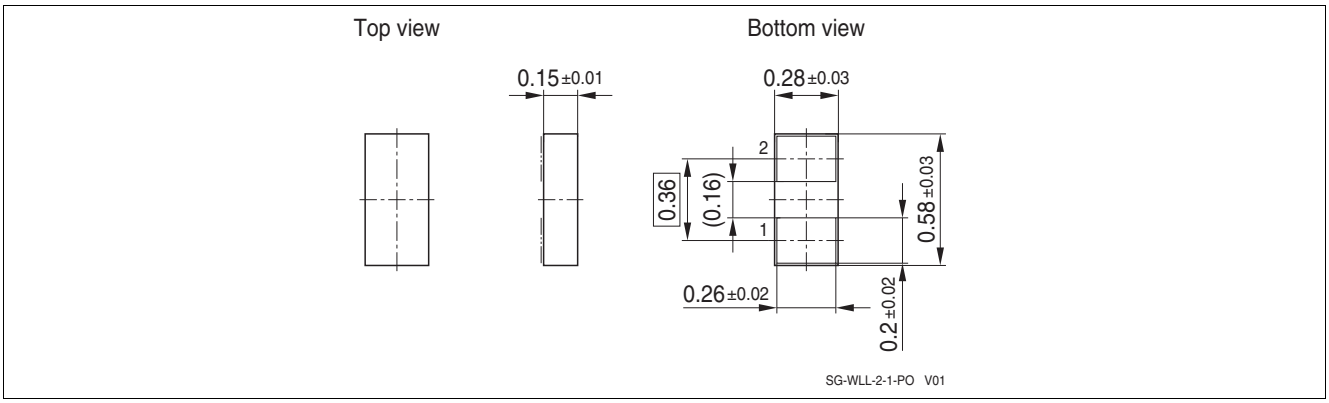

Figure 5-1 WLL-2-1 Package outline (dimension in mm)

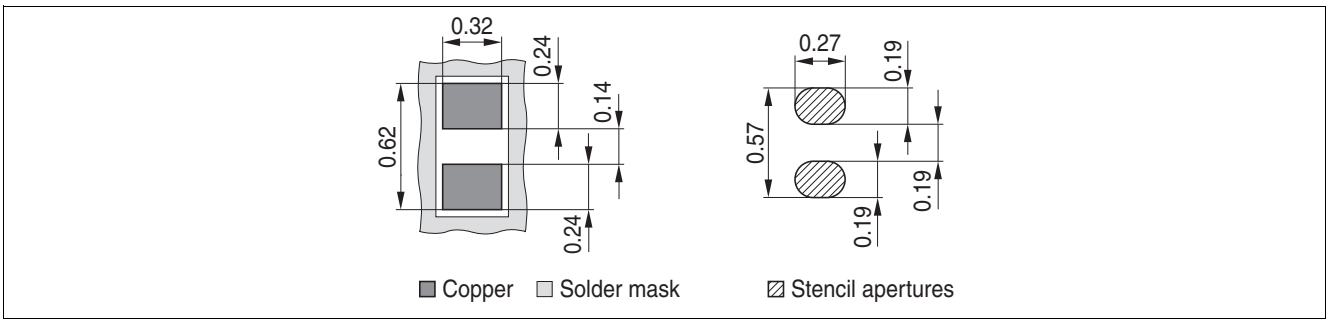

Figure 5-2 WLL-2-1 Footprint (dimension in mm)Recommendation for Printed Circuit Board Assembly[2]

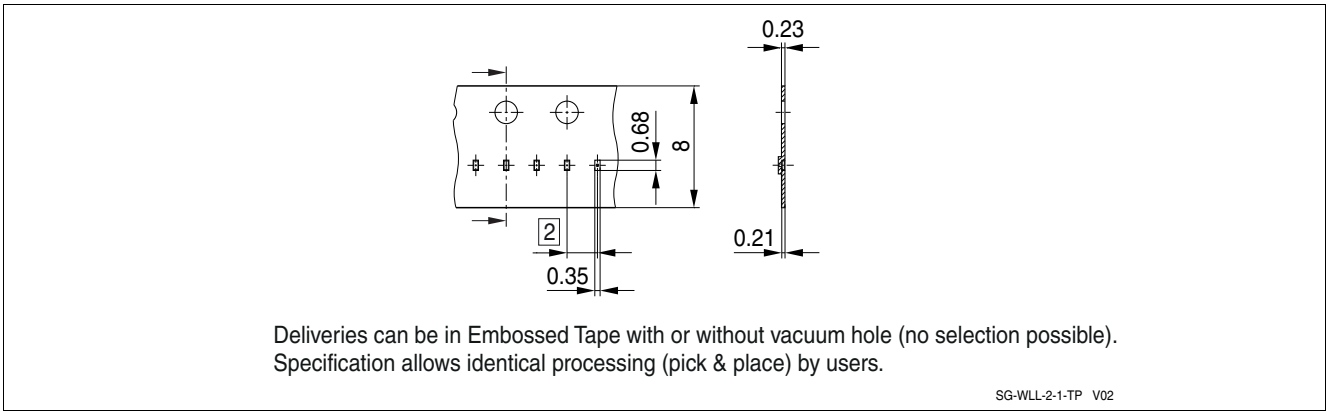

Figure 5-3 WLL-2-1 Packing (dimension in mm)

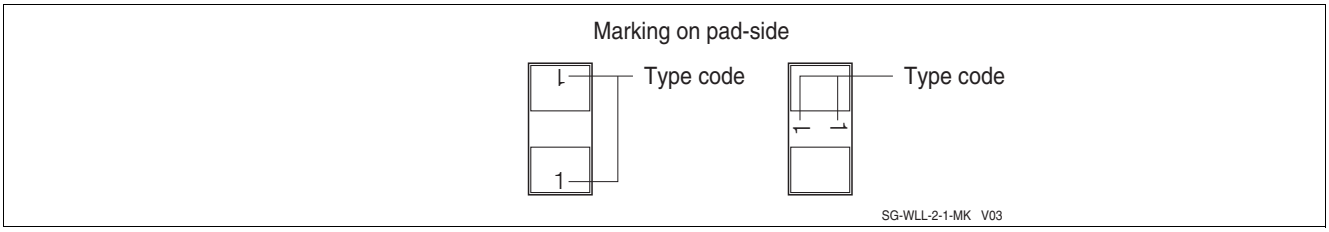

Figure 5-4 WLL-2-1 Marking example, Type code see: Table 1-1 “Part Information” on Page 3