



6-BIT D REGISTER

SY10E151
SY100E151

FEATURES

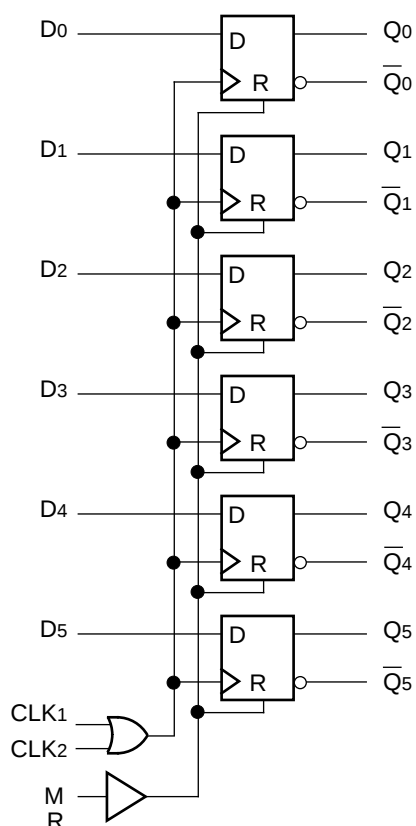
- 1100MHz toggle frequency
- Extended 100E VEE range of -4.2V to -5.46V
- Differential outputs
- Asynchronous Master Reset
- Dual clocks
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E151
- Available in 28-pin PLCC package

DESCRIPTION

The SY10/100E151 offer 6 edge-triggered, high-speed, master-slave D-type flip-flops with differential outputs, designed for use in new, high-performance ECL systems. The two external clock signals (CLK1, CLK2) are gated through a logical OR operation before use as clocking control for the flip-flops. Data is clocked into the flip-flops on the rising edge of either CLK1 or CLK2 (or both). When both CLK1 and CLK2 are at a logic LOW, data enters the master and is transferred to the slave when either CLK1 or CLK2 (or both) go HIGH.

The MR (Master Reset) signal operates asynchronously to make all Q outputs go to a logic LOW.

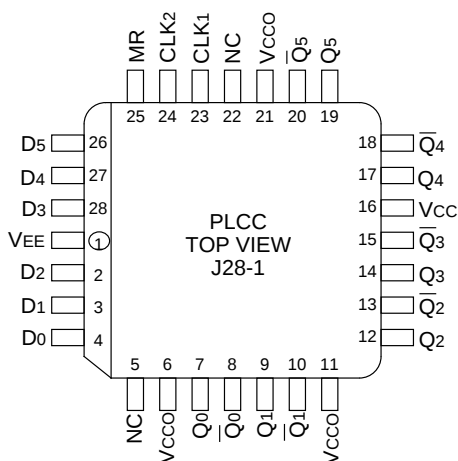
BLOCK DIAGRAM



PIN NAMES

Pin	Function
D0-D5	Data Inputs
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q0-Q5	True Outputs
$\bar{Q}0-\bar{Q}5$	Inverting Outputs
Vcco	Vcc to Output

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E151JI	J28-1	Industrial	SY10E151JI	Sn-Pb
SY10E151JITR ⁽²⁾	J28-1	Industrial	SY10E151JI	Sn-Pb
SY10E151JC	J28-1	Commercial	SY10E151JC	Sn-Pb
SY10E151JCTR ⁽²⁾	J28-1	Commercial	SY10E151JC	Sn-Pb
SY100E151JC	J28-1	Commercial	SY100E151JC	Sn-Pb
SY100E151JCTR ⁽²⁾	J28-1	Commercial	SY100E151JC	Sn-Pb
SY10E151JY ⁽³⁾	J28-1	Industrial	SY10E151JY with Pb-Free bar-line indicator	Matte-Sn
SY10E151JYTR ^(2, 3)	J28-1	Industrial	SY10E151JY with Pb-Free bar-line indicator	Matte-Sn
SY100E151JZ ⁽³⁾	J28-1	Commercial	SY100E151JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E151JZTR ^(2, 3)	J28-1	Commercial	SY100E151JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

TRUTH TABLES⁽¹⁾**Asynchronous Operation**

Inputs				Output
D _n	CLK ₁	CLK ₂	MR	Q _n (t + 1)
X	X	X	H	L

Note:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
t = Time before positive CLK transition
t+1 = Time after positive CLK transition
u = LOW-to-HIGH transition

Synchronous Operation

Inputs				Output
D _n	CLK ₁	CLK ₂	MR	Q _n (t + 1)
L	u	L	L	L
H	u	L	L	H
L	L	u	L	L
H	L	u	L	H
X	H	u	L	Q _n (t)
X	u	H	L	Q _n (t)
X	L	L	L	Q _n (t)

DC ELECTRICAL CHARACTERISTICS⁽¹⁾V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current										mA	—
	10E	—	65	78	—	65	78	—	65	78		
	100E	—	65	78	—	65	78	—	75	90		

Note:

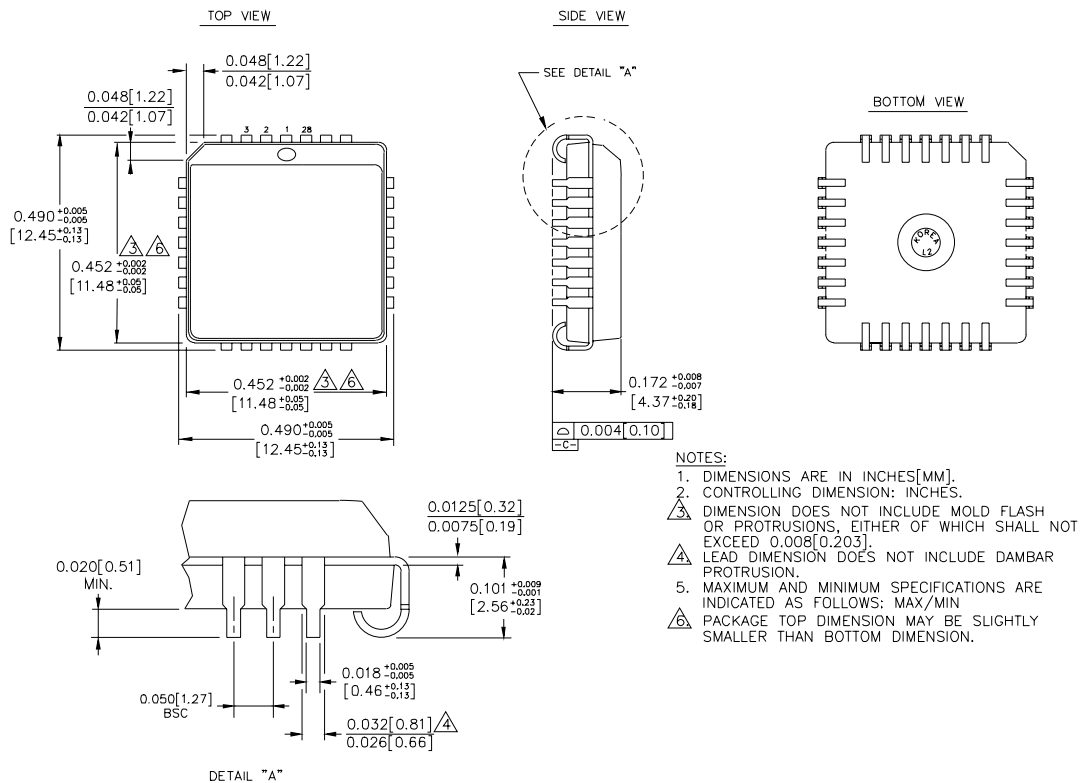
1. Specification for packaged product only.

AC ELECTRICAL CHARACTERISTICS⁽²⁾V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f _{MAX}	Max. Toggle Frequency	1100	1400	—	1100	1400	—	1100	1400	—	MHz	—
t _{PD}	Propagation Delay to Output CLK MR	475 475	650 650	800 850	475 475	650 650	800 850	475 475	650 650	800 850	ps	—
t _S	Set-up Time, D	0	–175	—	0	–175	—	0	–175	—	ps	—
t _H	Hold Time, D	350	175	—	350	175	—	350	175	—	ps	—
t _{RR}	Reset Recovery Time	750	550	—	750	550	—	750	550	—	ps	—
t _{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t _{skew}	Within-Device Skew	—	65	—	—	65	—	—	65	—	ps	1
t _r t _f	Rise/Fall Time 20% to 80%	300	450	700	300	450	700	300	450	700	ps	—

Note:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Specification for packaged product only.

28-PIN PLCC (J28-1)

Rev. 03

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