

**SY10EL34/L  
SY100EL34/L****5V/3.3V ÷2, ÷4, ÷8 Clock Generation Chip****Precision Edge®****Precision Edge®****General Description**

The SY10/100EL34/L are low-skew ÷2, ÷4, ÷8 clock generation chips designed explicitly for low-skew clock generation applications. The internal dividers are synchronous to each other; therefore, the common output edges are all precisely aligned. The devices can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the  $V_{BB}$  output, a sinusoidal source can be AC-coupled into the device. If a single-ended input is to be used, the  $V_{BB}$  output should be connected to the  $\overline{CLK}$  input and bypassed to ground via a 0.01µF capacitor. The  $V_{BB}$  output is designed to act as the switching reference for the input of the EL34/L under single-ended input conditions. As a result, this pin can only source/ sink up to 0.5mA of current.

The common enable ( $\overline{EN}$ ) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as for multiple EL34/Ls in a system.

Data sheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

**Features**

- 3.3V and 5V power supply options
- 50ps output-to-output skew
- Synchronous enable/disable
- Master Reset for synchronization
- Internal 75KΩ input pull-down resistors
- Available in 16-pin SOIC package

**Pin Description**

Pin Name	Pin Function
CLK	Differential clock inputs.
$\overline{EN}$	Synchronous enable.
MR	Master reset.
$V_{BB}$	Reference output.
$Q_0$	Differential ÷2 outputs.
$Q_1$	Differential ÷4 outputs.
$Q_2$	Differential ÷8 outputs.

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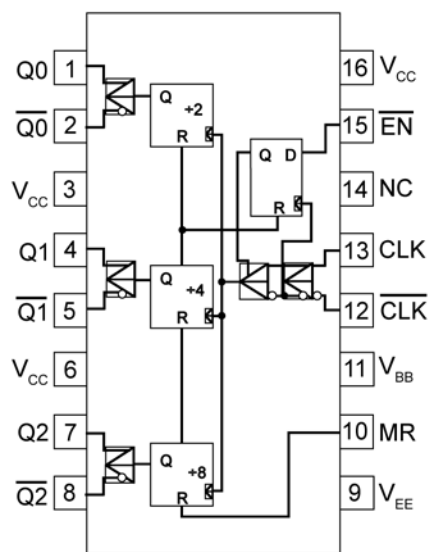
## Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10EL34LZG	Z16-2	Industrial	SY10EL34LZG with Pb-Free Bar Line Indicator	Pb-Free NiPdAu
SY10EL34LZGTR <sup>(2)</sup>	Z16-2	Industrial	SY10EL34LZG with Pb-Free Bar Line Indicator	Pb-Free NiPdAu
SY100EL34LZG	Z16-2	Industrial	SY100EL34LZG with Pb-Free Bar Line Indicator	Pb-Free NiPdAu
SY100EL34LZGTR <sup>(2)</sup>	Z16-2	Industrial	SY100EL34LZG with Pb-Free Bar Line Indicator	Pb-Free NiPdAu
SY10EL34ZG	Z16-2	Industrial	SY10EL34ZG with Pb-Free Bar Line Indicator	Pb-Free NiPdAu
SY10EL34ZGTR <sup>(2)</sup>	Z16-2	Industrial	SY10EL34ZG with Pb-Free Bar Line Indicator	Pb-Free NiPdAu
SY100EL34ZG	Z16-2	Industrial	SY100EL34ZG with Pb-Free Bar Line Indicator	Pb-Free NiPdAu
SY100EL34ZGTR <sup>(2)</sup>	Z16-2	Industrial	SY100EL34ZG with Pb-Free Bar Line Indicator	Pb-Free NiPdAu

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC electricals only.
2. Tape and reel.

## Pin Configuration



16-Pin Narrow SOIC (Z16-2)

**DC Electrical Characteristics<sup>(1)</sup>** $V_{EE} = V_{EE}$  (minimum) to  $V_{EE}$  (maximum);  $V_{CC} = \text{GND}$ .

Symbol	Parameter	Min.	Typ.	Max.	Units	
<b>T<sub>A</sub> = -40°C</b>						
I <sub>EE</sub>	Power Supply Current	10EL	-	-	49	mA
		100EL	-	-	49	
V <sub>BB</sub>	Output Reference Voltage	10EL	-1.43	-	-1.30	V
		100EL	-1.38	-	-1.26	
I <sub>IH</sub>	Input High Current	-	-	150	μA	
<b>T<sub>A</sub> = 0°C</b>						
I <sub>EE</sub>	Power Supply Current	10EL	-	-	49	mA
		100EL	-	-	49	
V <sub>BB</sub>	Output Reference Voltage	10EL	-1.38	-	-1.27	V
		100EL	-1.38	-	-1.26	
I <sub>IH</sub>	Input High Current	-	-	150	μA	
<b>T<sub>A</sub> = +25°C</b>						
I <sub>EE</sub>	Power Supply Current	10EL	-	-	49	mA
		100EL	-	-	49	
V <sub>BB</sub>	Output Reference Voltage	10EL	-1.35	-	-1.25	V
		100EL	-1.38	-	-1.26	
I <sub>IH</sub>	Input High Current	-	-	150	μA	
<b>T<sub>A</sub> = +85°C</b>						
I <sub>EE</sub>	Power Supply Current	10EL	-	-	49	mA
		100EL	-	-	54	
V <sub>BB</sub>	Output Reference Voltage	10EL	-1.31	-	-1.19	V
		100EL	-1.38	-	-1.26	
I <sub>IH</sub>	Input High Current	-	-	150	μA	

**Note:**

- Parametric values specified at:
  - 5V Power Supply Range:
    - 100EL34 Series: -4.2V to -5.5V
    - 10EL34 Series: -4.75V to -5.5V
  - 3V Power Supply Range:
    - 10/100EL34L Series: -3.0V to -3.8V

**AC Electrical Characteristics<sup>(1)</sup>** $V_{EE} = V_{EE}$  (minimum) to  $V_{EE}$  (maximum);  $V_{CC} = GND$ .

Symbol	Parameter	Min.	Typ.	Max.	Units
<b>T<sub>A</sub> = -40°C</b>					
t <sub>PD</sub>	Propagation Delay to Output CLK MR	960	1100	1200	ps
		650	800	1010	
t <sub>SKREW</sub>	Within-Device Skew <sup>(2)</sup>	–	–	50	ps
t <sub>S</sub>	Set-Up Time ( $\overline{EN}$ )	400	–	–	ps
t <sub>H</sub>	Hold Time ( $\overline{EN}$ )	200	–	–	ps
V <sub>PP</sub>	Minimum Input Swing <sup>(3)</sup>	250	–	–	mV
V <sub>CMR</sub>	Common-Mode Range <sup>(4)</sup>	–1.3	–	–0.4	V
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times Q (20% – 80%)	275	400	525	ps
<b>T<sub>A</sub> = 0°C</b>					
t <sub>PD</sub>	Propagation Delay to Output CLK MR	960	1100	1200	ps
		650	800	1010	
t <sub>SKREW</sub>	Within-Device Skew <sup>(2)</sup>	–	–	50	ps
t <sub>S</sub>	Set-Up Time ( $\overline{EN}$ )	400	–	–	ps
t <sub>H</sub>	Hold Time ( $\overline{EN}$ )	200	–	–	ps
V <sub>PP</sub>	Minimum Input Swing <sup>(3)</sup>	250	–	–	mV
V <sub>CMR</sub>	Common-Mode Range <sup>(4)</sup>	–1.4	–	–0.4	V
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times Q (20% – 80%)	275	400	525	ps
<b>T<sub>A</sub> = +25°C</b>					
t <sub>PD</sub>	Propagation Delay to Output CLK MR	960	1100	1200	ps
		650	800	1010	
t <sub>SKREW</sub>	Within-Device Skew <sup>(2)</sup>	–	–	50	ps
t <sub>S</sub>	Set-Up Time ( $\overline{EN}$ )	400	–	–	ps
t <sub>H</sub>	Hold Time ( $\overline{EN}$ )	200	–	–	ps
V <sub>PP</sub>	Minimum Input Swing <sup>(3)</sup>	250	–	–	mV
V <sub>CMR</sub>	Common-Mode Range <sup>(4)</sup>	–1.4	–	–0.4	V
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times Q (20% – 80%)	275	400	525	ps

**AC Electrical Characteristics<sup>(1)</sup> (Continued)** $V_{EE} = V_{EE}$  (minimum) to  $V_{EE}$  (maximum);  $V_{CC} = \text{GND}$ .

Symbol	Parameter	Min.	Typ.	Max.	Units
$T_A = +85^\circ\text{C}$					
$t_{PD}$	Propagation Delay to Output CLK MR	960	1100	1200	ps
		650	800	1010	
$t_{SKEW}$	Within-Device Skew	–	–	50	ps
$t_S$	Set-Up Time ( $\overline{\text{EN}}$ )	400	–	–	ps
$t_H$	Hold Time ( $\overline{\text{EN}}$ )	200	–	–	ps
$V_{PP}$	Minimum Input Swing <sup>(3)</sup>	250	–	–	mV
$V_{CMR}$	Common-Mode Range <sup>(4)</sup>	–1.4	–	–0.4	V
$t_r$ $t_f$	Output Rise/Fall Times Q (20% – 80%)	275	400	525	ps

**Notes:**

- Parametric values specified at:
  - 5V Power Supply Range:
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    - 10EL34 Series: –4.75V to –5.5V
  - 3V Power Supply Range:
    - 10/100EL34L Series: –3.0V to –3.8V
- Skew is measured between outputs under identical transitions.
- Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.
- The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PP}$  minimum and 1V. The lower end of the CMR range varies 1:1 with  $V_{EE}$ . The numbers in the specification table assume a nominal  $V_{EE} = -3.3\text{V}$ . Note for PECL operation, the  $V_{CMR(MIN)}$  will be fixed at  $3.3\text{V} - |V_{CMR(MIN)}|$ .

**Truth Table**

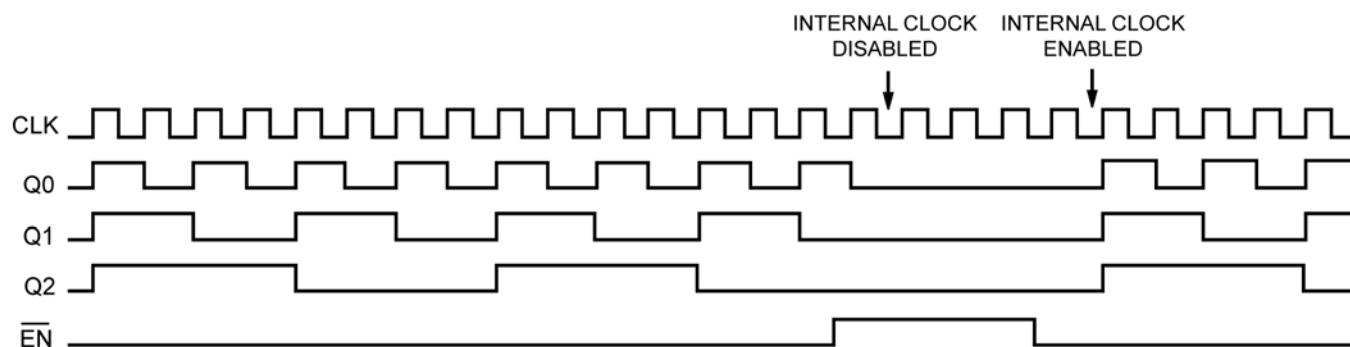
CLK	$\overline{\text{EN}}$	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold $Q_{0-2}$
X	X	H	Reset $Q_{0-2}$

**Notes:**

Z = LOW-to-HIGH transition

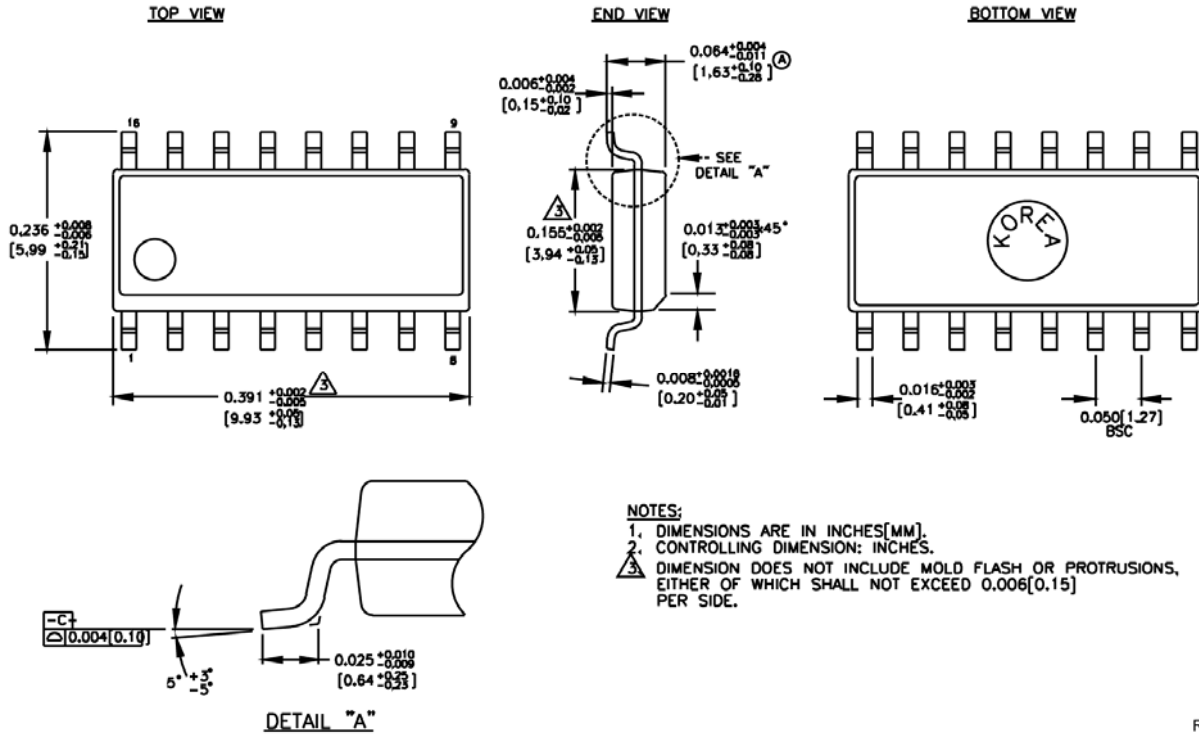
ZZ = HIGH-to-LOW transition

## Timing Diagram



The  $\overline{EN}$  signal will freeze the internal clocks to the flip-flops on the first falling edge of CLK after its assertion. The internal dividers will maintain their state during the internal clock freeze and will return to clocking once the internal clocks are unfrozen. The outputs will transition to their next states in the same manner, time and relationship as they would have had the  $\overline{EN}$  signal not been asserted.

Package Information



Rev. 02

16-Pin .150" Wide SOIC (Z16-2)

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