

FEATURES

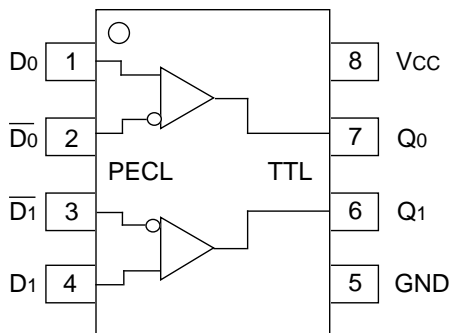
- 3.0ns typical propagation delay
- <500ps typical output-to-output skew
- Differential PECL outputs
- 24mA TTL outputs
- Flow-through pinouts
- ESD protection of 2000V
- Available in 8-pin SOIC package

DESCRIPTION

The SY10/100ELT23 are dual differential PECL-to-TTL translators. Because PECL (Positive ECL) levels are used, only +5V and ground are required. The small outline 8-lead SOIC package and the low skew, dual gate design of the ELT23 makes it ideal for applications which require the translation of a clock and a data signal.

The ELT23 is available in both ECL standards: the 10ELT is compatible with positive ECL 10H logic levels, while the 100ELT is compatible with positive ECL 100K logic levels.

PIN CONFIGURATION/BLOCK DIAGRAM



**SOIC
TOP VIEW**

PIN NAMES

Pin	Function
Q _n	TTL Outputs
D _n	Differential PECL Inputs
V _{cc}	+5.0V Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{CC}	Power Supply Voltage	-0.5 to +7.0	V
V _I	PECL Input Voltage	0V to V _{CC} +0.5	V
V _O	Voltage Applied to Output at HIGH State	-0.5 to +5.5	V
I _O	Current Applied to Output at LOW State	Twice the Rated I _{OL}	mA
T _{store}	Storage Temperature	-65 to +150	°C
T _{amb}	Operating Temperature	-40 to +85	°C

TRUTH TABLE

D	\bar{D}	Q
L	H	L
H	L	H
Open	Open	L

NOTES:

- Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

V_{CC} = V_{CC} (Min.) to V_{CC} (Max.)

Symbol	Parameter	T _A = -40°C		T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
I _{CC}	Power Supply Current	—	30	—	30	—	30	—	30	mA	—

NOTE:

- Parametric values specified at: 5 volt Power Supply Range 100ELT23 Series: +4.2V to +5.5V.
10ELT23 Series +4.75V to +5.5V.

AC ELECTRICAL CHARACTERISTICS⁽¹⁾

V_{CC} = V_{CC} (Min.) to V_{CC} (Max.)

Symbol	Parameter	T _A = -40°C		T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay D to Output Q	2.5	3.5	2.5	3.5	2.5	3.5	2.5	3.5	ns	CL = 50pF
t _{skpp}	Part-to-Part Skew ^(2,5)	—	0.5	—	0.5	—	0.5	—	0.5	ns	CL = 50pF
t _{skew++}	Within-Device Skew ^(3,5)	—	0.3	—	0.3	—	0.3	—	0.3	ns	CL = 50pF
t _{skew--}	Within-Device Skew ^(4,5)	—	0.3	—	0.3	—	0.3	—	0.3	ns	CL = 50pF
t _r t _f	Output Rise/Fall Time 1.0V to 2.0V	—	1.5	—	1.5	—	1.5	—	1.5	ns	CL = 50pF
f _{MAX}	Maximum Input Frequency ⁽⁵⁾	160	—	160	—	160	—	160	—	MHz	CL = 50pF

NOTES:

- Parametric values specified at: 5 volt Power Supply Range 100ELT23 Series: +4.2V to +5.5V.
10ELT23 Series +4.75V to +5.5V.
- Device-to-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
- Within-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
- Within-Device Skew considering LOW-to-LOW transitions at common V_{CC} level.
- All skew parameters are guaranteed but not tested.

8 LEAD PLASTIC SOIC (Z8-1)

FILE/REV #: PD0032A03

PD/0032/ASCORP

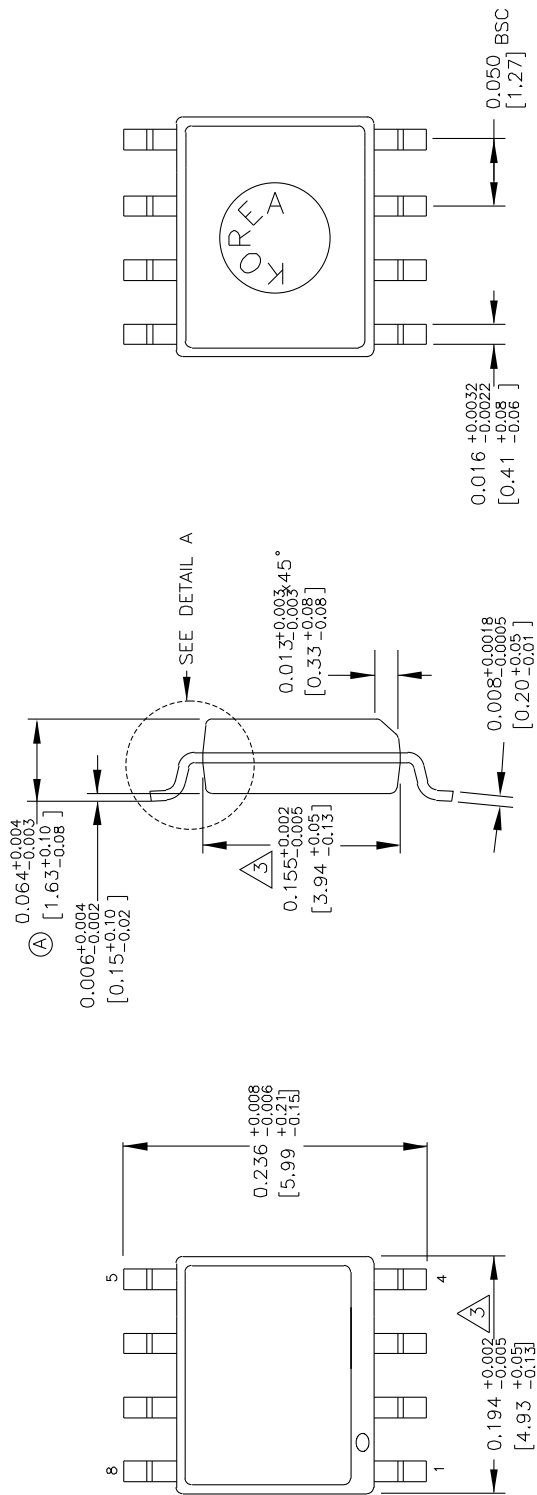
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REV.	REVISION DESCRIPTION	DATE
00	NEW OUTLINE DRAWING.	01/20/94
01	CONVERT TO AUTOCAD. REFERENCE AMKOR DWG. NO. 00019	12/14/95
	REV.05. MAKE (A) SAME AS JEDEC.	
02	ADDED LEAD WIDTH AND PITCH DIMENSIONS. CORRECTED TYPOS.	03/12/97
03	CONVERT DWG TO REL.13 AND ONE PAGE DOCUMENT.	02/20/98

TOP VIEW

END VIEW

BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.



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APPROVALS	DATE	APPROVALS	DATE	SIZE	8 LEAD PLASTIC SOIC (.150" WIDE)
ORIGINATOR: ERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	PACKAGE OUTLINE
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					

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SCALE: N/A
REVISION: 03

