

### FEATURES

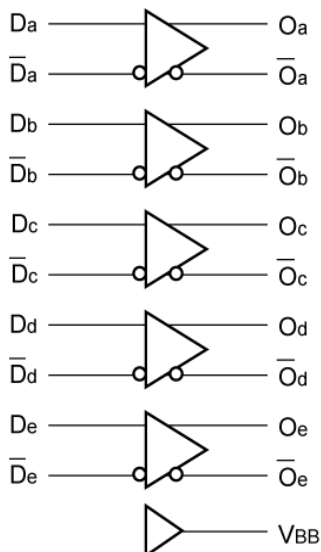
- Max. propagation delay of 900ps
- Differential outputs
- IEE min. of -60mA
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- VBB output for single-ended use
- More than twice as fast as Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

### DESCRIPTION

The SY100S314 offers five differential line receivers with emitter follower outputs, designed for use in high-performance ECL systems. For single-ended operation, the VBB reference voltage is available. In the single-ended mode, the apparent input threshold of the true inputs is 30mV higher than the threshold of the complementary inputs.

Common mode rejection of +1.0V is achieved through the use of active current sources. If both the true and complement inputs are at the same potential between VEE and VCC, then the complementary outputs will take on a logic HIGH state. Unlike the other members of the Micrel 300K family, the inputs on this device do not have pull-down resistors.

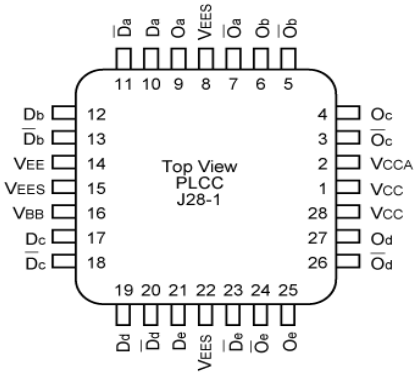
### BLOCK DIAGRAM



### PIN NAMES

Pin	Function
Da – De	Data Inputs
$\bar{D}a - \bar{D}e$	Inverting Data Inputs
Oa – Oe	Data Outputs
$\bar{O}a - \bar{O}e$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S314JC	J28-1	Commercial	SY100S314JC	Sn-Pb
SY100S314JCTR <sup>(1)</sup>	J28-1	Commercial	SY100S314JC	Sn-Pb
SY100S314JZ <sup>(2)</sup>	J28-1	Commercial	SY100S314JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S314JZTR <sup>(1, 2)</sup>	J28-1	Commercial	SY100S314JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S314JY <sup>(2)</sup>	J28-1	Industrial	SY100S314JY with Pb-Free bar-line indicator	Matte-Sn
SY100S314JYTR <sup>(1, 2)</sup>	J28-1	Industrial	SY100S314JY with Pb-Free bar-line indicator	Matte-Sn

Notes:

- 1. Tape and Reel.
- 2. Pb-Free package is recommended for new designs.

## LOGIC EQUATION

$O = D$

## DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

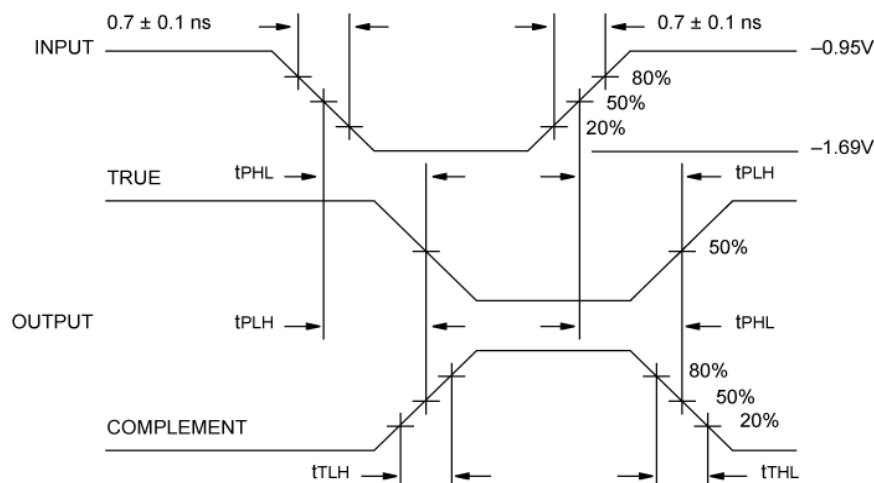
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$V_{DIFF}$	Input Voltage Differential	150	—	—	mV	Required for Full Output Swing
$V_{CM}$	Common Mode Voltage	—	—	1.0	V	Permissible $\pm V_{CM}$ with Respect to $V_{BB}$
$I_{IH}$	Input HIGH Current	—	—	50	$\mu A$	$V_{IN} = V_{IH} (Max.)$ , $D_a - D_e = V_{BB}$ , $\bar{D}_a - \bar{D}_e = V_{IL} (Min.)$
$I_{CBO}$	Input Leakage Current	-10	—	—	$\mu A$	$V_{IN} = V_{EE}$ , $D_a - D_e = V_{BB}$ , $\bar{D}_a - \bar{D}_e = V_{IL} (Min.)$
$I_{EE}$	Power Supply Current	-60	-45	-30	mA	$D_a - D_e = V_{BB}$ , $\bar{D}_a - \bar{D}_e = V_{IL} (Min.)$

## AC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = -40^\circ C$		$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	300	900	300	900	300	900	300	900	ps	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	300	900	ps	

## TIMING DIAGRAM

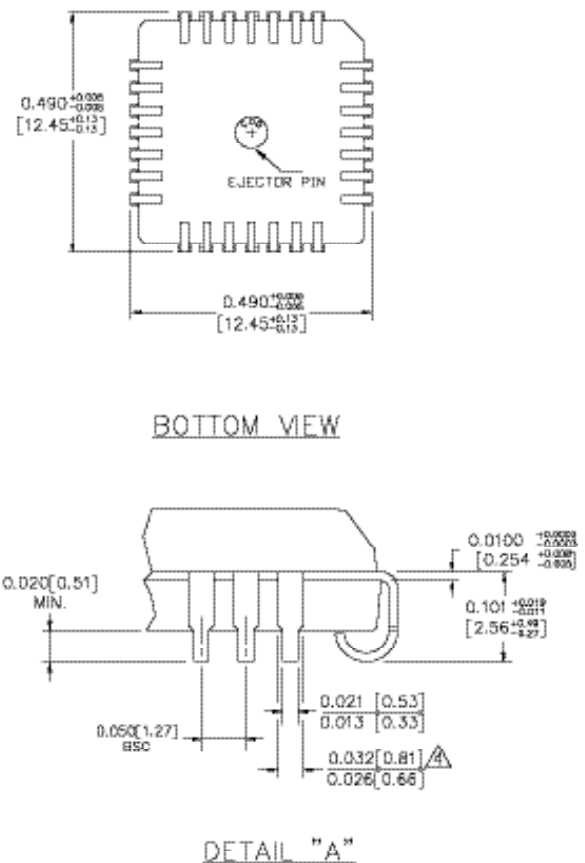
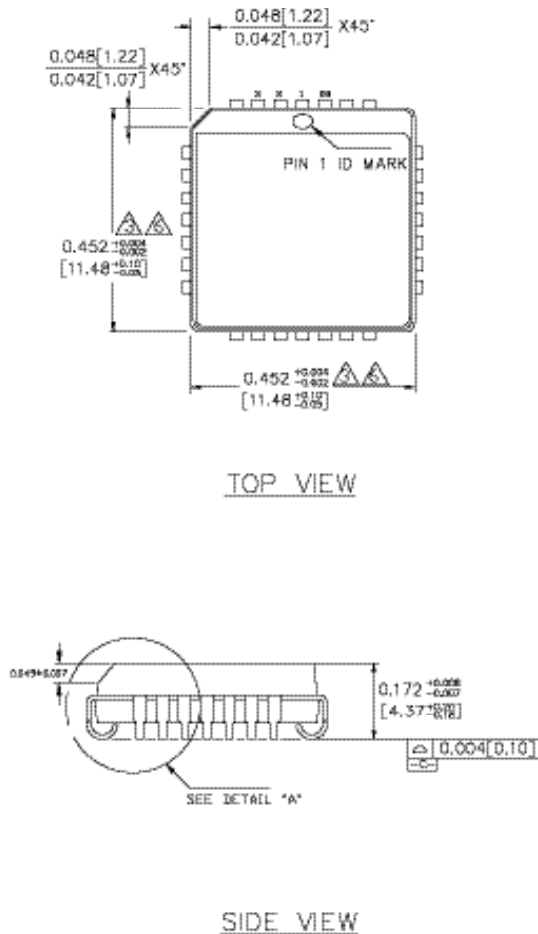


Propagation Delay and Transition Times

### Note:

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

## 28-PIN PLCC (J28-1)



### NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

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