

FEATURES

- 25 Ω cut-off bus outputs
- 50 Ω receiver outputs
- Transmit and receive registers with separate clocks
- 1500ps max. delay from CLK1 to Bus Outputs (BUS)
- 1500ps max. delay from CLK2 to Receiver Outputs (Q)
- Individual bus enable pins
- Internal 75K Ω input pull-down resistors
- Voltage and temperature compensation for improved noise immunity
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Available in 28-pin PLCC package

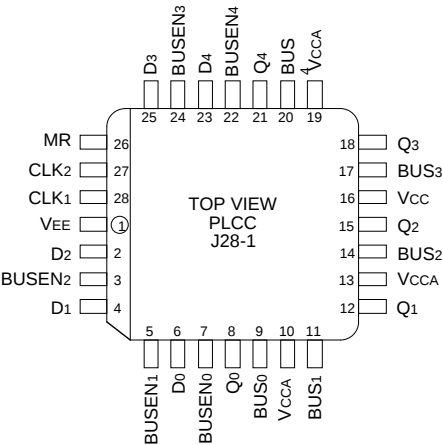
DESCRIPTION

The SY100S891 is a 5-bit registered transceiver containing five bus transceivers with both transmit and receive registers. The bus outputs (BUS0 – BUS4) are specified for driving a 25 ohm bus and the receive outputs (Q0 – Q4) are specified for driving a 50 ohm line. The bus outputs have a normal high level output voltage and a normal low level output voltage when the bus enable (BUSEN0 – BUSEN4) is high. However, the output is switched to a cut-off level when a bus-enable is low. This cut-off level is sufficiently low that a relatively high impedance is presented to the bus in order to minimize reflections. There is one bus-enable for each bus driver; a clock (CLK1) which is common to all five bus driver registers; and a separate clock (CLK2) which is common to all five receive registers. Data at the D inputs is clocked to the Bus register by a positive transition of CLK1 and data on the bus is clocked into the Receiver register by a positive transition of CLK2. A high on the Master Reset clears all registers.

PIN NAMES

Pin	Function
BUSEN0–4	Bus Enable Inputs
D0 – D4	Data Inputs
CLK1	Bus Driver Clock Input
CLK2	Receive Register Clock
MR	Master Reset
Q0 – Q4	Bus Receive Outputs
BUS0–4	Bus Outputs

PACKAGE/ORDERING INFORMATION

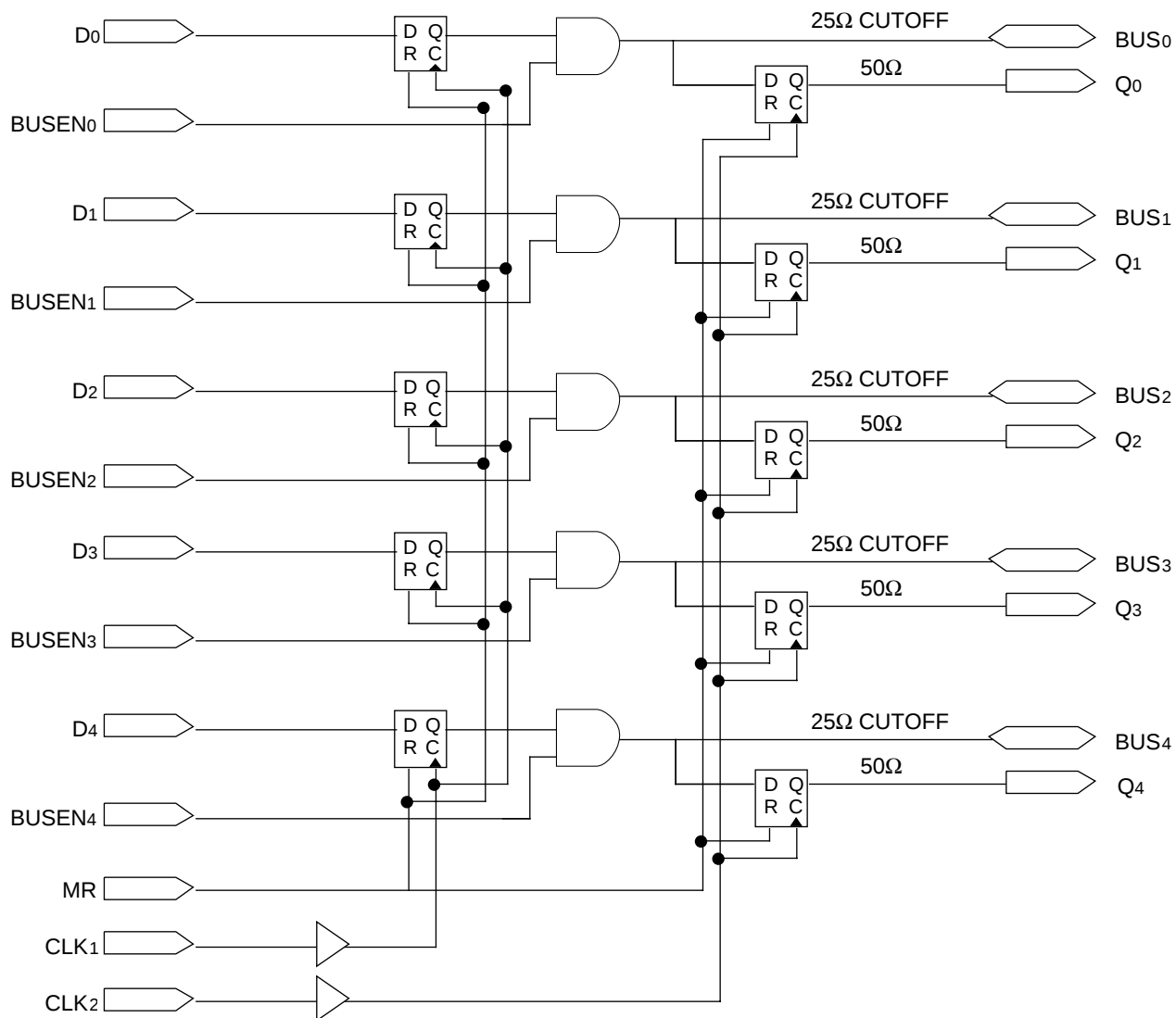


28-Pin PLCC (J28-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S891JC	J28-1	Commercial	SY100S891JC	Sn-Pb
SY100S891JCTR ⁽¹⁾	J28-1	Commercial	SY100S891JC	Sn-Pb
SY100S891JZ ⁽²⁾	J28-1	Commercial	SY100S891JC with Pb-Free bar-line indicator	Matte-Sn
SY100S891JZTR ^(1, 2)	J28-1	Commercial	SY100S891JC with Pb-Free bar-line indicator	Matte-Sn

- Notes:
- 1. Tape and Reel.
 - 2. Pb-Free package is recommended for new designs.

BLOCK DIAGRAM

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V _{CUT}	Cut-off Bus Output Voltage	−2200	−2160	−2100	mV	V _{IN} = V _{IH} (Max.) or V _{IL} (Min.)	Loading with 25Ω to −2.20V
V _{OH}	Output HIGH Voltage Bus	−1025	−955	−880	mV	V _{IN} = V _{IH} (Max.) or V _{IL} (Min.)	Loading with 25Ω to −2.0V
V _{OL}	Output LOW Voltage Bus	−1810	−1705	−1620	mV		
V _{OHA}	Output HIGH Voltage Bus	−1035	—	—	mV	V _{IN} = V _{IH} (Min.) or V _{IL} (Max.)	
V _{OLA}	Output LOW Voltage Bus	—	—	−1610	mV		
V _{OH}	Output HIGH Voltage Receiver	−1025	−955	−880	mV	V _{IN} = V _{IH} (Max.) or V _{IL} (Min.)	Loading with 50Ω to −2.0V
V _{OL}	Output LOW Voltage Receiver	−1810	−1705	−1620	mV		
V _{OHA}	Output HIGH Voltage Receiver	−1035	—	—	mV	V _{IN} = V _{IH} (Min.) or V _{IL} (Max.)	
V _{OLA}	Output LOW Voltage Receiver	—	—	−1610	mV		
V _{IH}	Input HIGH Voltage	−1165	—	−880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	−1810	—	−1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.5	—	—	μA	V _{IN} = V _{IL} (Min.)	
I _{IH}	Input High Current	—	—	150	μA	V _{IN} = V _{IH} (Max.)	
I _{EE}	Power Supply Current	−216	—	—	mA	Inputs Open	
C _{IN}	Input Pin Capacitance	—	4	—	pF		
C _{OUT}	Output Pin Capacitance	—	5	—	pF		

AC ELECTRICAL CHARACTERISTICS

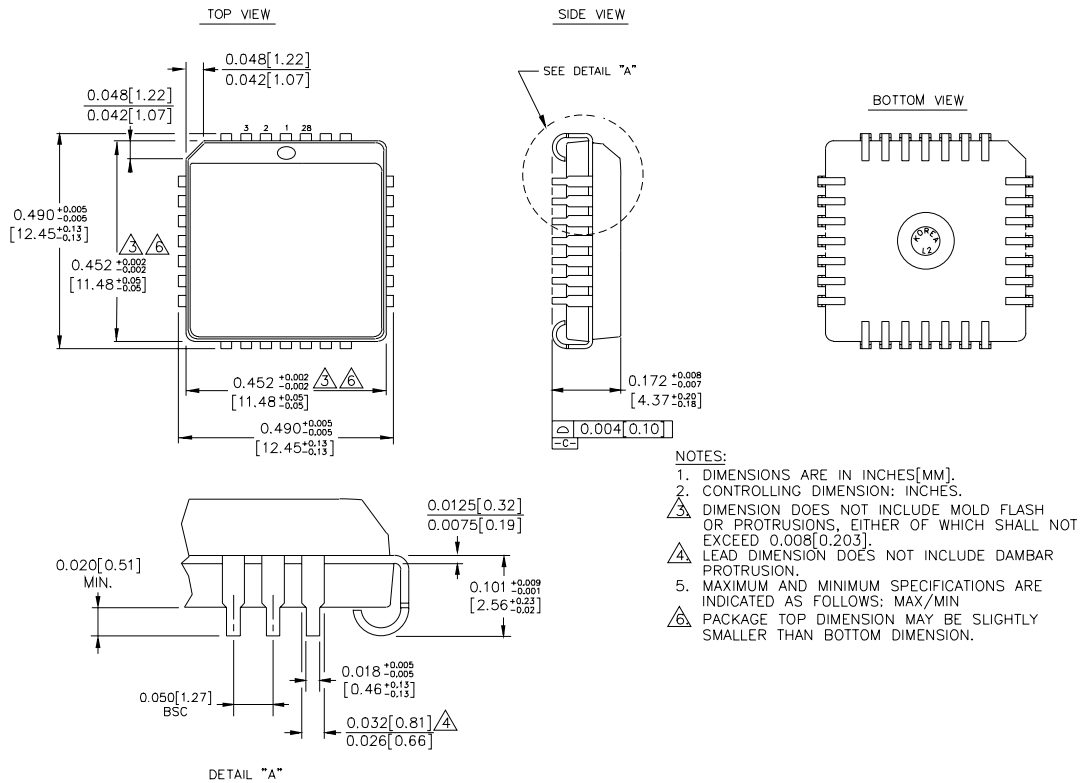
$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$			$T_A = +25^{\circ}C$			$T_A = +85^{\circ}C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{PLH} t _{PHL}	Propagation Delay ⁽¹⁾ CLK1 to Bus	600	1000	1500	600	1000	1500	600	1000	1500	ps	
t _{PLH} t _{PHL}	Propagation Delay ⁽²⁾ CLK2 to Q	500	800	1200	500	800	1200	500	800	1200	ps	
t _{PLH} t _{PHL}	Propagation Delay ⁽¹⁾ BUSEN to Bus	500	800	1200	500	800	1200	500	800	1200	ps	
t _{PLH} t _{PHL}	Propagation Delay ⁽¹⁾ Master Reset to Bus	600	1000	1500	600	1000	1500	600	1000	1500	ps	
t _{PLH} t _{PHL}	Propagation Delay ⁽²⁾ Master Reset to Q	500	800	1200	500	800	1200	500	800	1200	ps	
t _s	Set-up Time Bus Wrt CLK2 D Wrt CLK1	—	—	400	—	—	400	—	—	400	ps	
		—	—	400	—	—	400	—	—	400		
t _{REL}	Master Reset Release Time	—	—	1000	—	—	1000	—	—	1000	ps	
t _H	Hold Time Bus Wrt CLK2 D Wrt CLK1	—	—	400	—	—	400	—	—	400	ps	
		—	—	400	—	—	400	—	—	400		
t _r	Output Rise Time Bus ⁽³⁾ Q ⁽⁴⁾	500	—	1000	500	—	1000	500	—	1000	ps	
		300	—	900	300	—	900	300	—	900		
t _f	Output Fall Time Bus ⁽³⁾ Q ⁽⁴⁾	500	—	1000	500	—	1000	500	—	1000	ps	
		300	—	900	300	—	900	300	—	900		
t _{skew}	Skew (Maximum difference between slowest and fastest path)	—	100	—	—	100	—	—	100	—	ps	

Notes:

1. Loaded with 25Ω to $-2.0V$
2. Loaded with 50Ω to $-2.0V$
3. 25Ω Load
4. 50Ω Load

28-PIN PLCC (J28-1)



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