5V/3.3V ÷ 2 DIVIDER

FEATURES

- Guaranteed maximum frequency > 4GHz
- 3.3V and 5V power supply options
- Guaranteed propagation delay <440ps over temperature
- Internal 75KΩ input pull-down resistors
- Wide operating temperature range: –40°C to +85°C
- Available in 8-pin MSOP and SOIC packages

ECL Pro™

DESCRIPTION

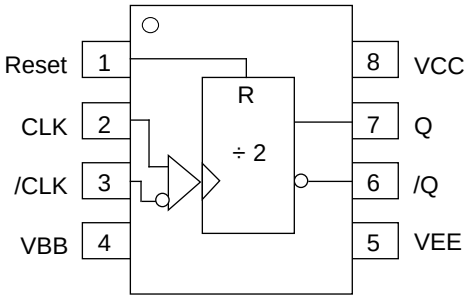
The SY10/100EP32V is an integrated ÷2 divider with differential clock inputs.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC-coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01µF capacitor and limit current sourcing or sinking to 0.5mA. When not used, V_{BB} should be left open.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronous use of multiple EP32's in a system.

The 100k series includes internal temperature compensation circuitry.

PIN CONFIGURATION/BLOCK DIAGRAM



TOP VIEW
(Available in MSOP or SOIC package)

PIN NAMES

Pin	Function
CLK, /CLK	ECL Clock Inputs
Reset	ECL Asynchronous Reset
V_{BB}	Reference Voltage Output
Q, /Q	ECL Data Outputs

TRUTH TABLE(1)

CLK	/CLK	RESET	Q	/Q
X	X	Z	L	H
Z	/Z	L	F	F

Note 1: Z = LOW-to-HIGH Transition
/Z = HIGH-to-LOW Transition
F = Divide by 2 function.

(10EP) LVPECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 3.3V ±10%; V_{EE} = 0V[2]

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	—	30	37	—	30	37	—	30	37	mA
V_{OH}	Output HIGH Voltage[3]	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage[3]	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2090	—	2415	2155	—	2480	2215	—	2540	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1365	—	1690	1430	—	1755	1490	—	1815	mV
V_{BB}	Output Voltage	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage[4] Common Mode Range (Differential)	2.0	—	V_{CC}	2.0	—	V_{CC}	2.0	—	V_{CC}	V
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current CLK /CLK	0.5 –150	— —	— —	0.5 –150	— —	— —	0.5 –150	— —	— —	µA

Note 1. 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

Note 2. Input and output parameters vary 1:1 with V_{CC}.

Note 3. All loading with 50Ω to V_{CC} –2.0V.

Note 4. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(10EP) PECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 5.0V ±10%; V_{EE} = 0V[2]

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	—	—	37	—	30	37	—	—	37	mA
V_{OH}	Output HIGH Voltage[3]	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage[3]	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3790	—	4115	3855	—	4180	3915	—	4240	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3065	—	3390	3130	—	3455	3190	—	3515	mV
V_{BB}	Output Voltage	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
V_{IHCMR}	Input HIGH Voltage[4] Common Mode Range (Differential)	2.0	—	V_{CC}	2.0	—	V_{CC}	2.0	—	V_{CC}	V
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current CLK /CLK	0.5 –150	— —	— —	0.5 –150	— —	— —	0.5 –150	— —	— —	µA

Note 1. 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

Note 2. Input and output parameters vary 1:1 with V_{CC}.

Note 3. All loading with 50Ω to V_{CC} –2.0V.

Note 4. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(10EP) ECL/LVECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 0V; V_{EE} = –3.3V to 5.0V ±10%[2]

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	—	—	37	—	30	37	—	—	37	mA
V_{OH}	Output HIGH Voltage[3]	–1135	–1010	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage[3]	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	–1210	—	–885	–1145	—	–820	–1085	—	–760	mV
V_{IL}	Input LOW Voltage (Single-Ended)	–1935	—	–1610	–1870	—	–1545	–1810	—	–1485	mV
V_{BB}	Output Voltage	–1510	–1410	–1310	–1445	–1345	–1245	–1385	–1285	–1185	mV
V_{IHCMR}	Input HIGH Voltage[4] Common Mode Range (Differential)	V_{EE} +2.0		0.0	V_{EE} +2.0		0.0	V_{EE} +2.0		0.0	V
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current CLK	0.5	—	—	0.5	—	—	0.5	—	—	µA
	/CLK	–150	—	—	–150	—	—	–150	—	—	

Note 1. 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

Note 2. Input and output parameters vary 1:1 with V_{CC}.

Note 3. All loading with 50Ω to V_{CC} – 2.0V.

Note 4. V_{IHCMR} (min) varies 1:1 with V_{EE}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(100EP) LVPECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = +3.3V ±10%; V_{EE} = 0V[2]

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	—	—	37	—	30	37	—	—	42	mA
V_{OH}	Output HIGH Voltage[3]	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage[3]	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2075	—	2420	2075	—	2420	2075	—	2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355	—	1675	1355	—	1675	1355	—	1675	mV
V_{BB}	Output Voltage	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage[4] Common Mode Range (Differential)	2.0	—	V_{CC}	2.0	—	V_{CC}	2.0	—	V_{CC}	V
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current CLK /CLK	0.5 –150	— —	— —	0.5 –150	— —	— —	0.5 –150	— —	— —	µA

Note 1. 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

Note 2. Input and output parameters vary 1:1 with V_{CC}.

Note 3. All loading with 50Ω to V_{CC} –2.0V.

Note 4. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(100EP) PECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = +5.0V ±10%; V_{EE} = 0V[2]

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	—	—	37	—	30	37	—	—	42	mA
V_{OH}	Output HIGH Voltage[3]	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage[3]	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3775	—	4120	3775	—	4120	3775	—	4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3055	—	3375	3055	—	3375	3055	—	3375	mV
V_{BB}	Output Voltage	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV
V_{IHCMR}	Input HIGH Voltage[4] Common Mode Range (Differential)	2.0	—	V_{CC}	2.0	—	V_{CC}	2.0	—	V_{CC}	V
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current CLK /CLK	0.5 –150	— —	— —	0.5 –150	— —	— —	0.5 –150	— —	— —	µA

Note 1. 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

Note 2. Input and output parameters vary 1:1 with V_{CC}.

Note 3. All loading with 50Ω to V_{CC} –2.0V.

Note 4. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(100EP) ECL/LVECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 0V; V_{EE} = –3.3V to –5.0V ±10%[2]

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	—	—	37	—	30	37	—	—	42	mA
V_{OH}	Output HIGH Voltage[3]	–1145	–1020	–895	–1145	–1020	–895	–1145	–1020	–895	mV
V_{OL}	Output LOW Voltage[3]	–1945	–1820	–1695	–1945	–1820	–1695	–1945	–1820	–1695	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	–1225	—	–880	–1225	—	–880	–1225	—	–880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	–1945	—	–1625	–1945	—	–1625	–1945	—	–1625	mV
V_{BB}	Output Voltage	–1525	–1425	–1325	–1525	–1425	–1325	–1525	–1425	–1325	mV
V_{IHCMR}	Input HIGH Voltage[4] Common Mode Range (Differential)	V_{EE} +2.0		0.0	V_{EE} +2.0		0.0	V_{EE} +2.0		0.0	V
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current CLK	0.5	—	—	0.5	—	—	0.5	—	—	µA
	/CLK	–150	—	—	–150	—	—	–150	—	—	

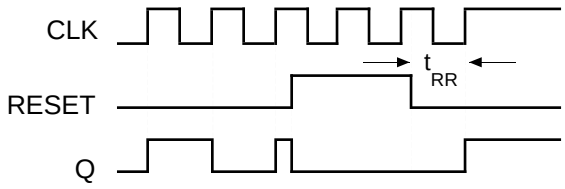
Note 1. 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

Note 2. Input and output parameters vary 1:1 with V_{CC}.

Note 3. All loading with 50Ω to V_{CC} –2.0V.

Note 4. V_{IHCMR} (min) varies 1:1 with V_{EE}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

TIMING DIAGRAM



AC ELECTRICAL CHARACTERISTICS[1]

NECL: V_{CC} = 0V, V_{EE} = –3.3V to –5.0V ±10%; PECL: V_{EE} = 0V, V_{CC} = +3.3V to +5.0V ±10%

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Maximum Frequency[3]	4	—	—	4	—	—	4	—	—	GHz
t_{PLH} t_{PHL}	Propagation Delay to Output Differential RESET, CLK → Q, /Q	250	330	420	260	275	430	280	400	440	ps
t_{RR}	Set/Reset Recovery	200	—	—	200	100	—	200	—	—	ps
t_{PW}	Minimum Pulse Width RESET	550	—	—	550	200	—	550	—	—	ps
t_{JITTER}	Cycle-to-Cycle RMS Jitter[2]	—	0.2	< 1	—	0.2	< 1	—	0.2	< 1	ps(rms)
V_{PP}	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q, /Q (20% to 80%)	50	100	150	50	100	160	50	100	160	ps

Note 1. Measured using a 750mV source, 50% duty cycle clock source. All loading with 50Ω to V_{CC} –2.0V.

Note 2. See Figure 1. f_{MAX} Jitter below.

Note 3. f_{MAX} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.

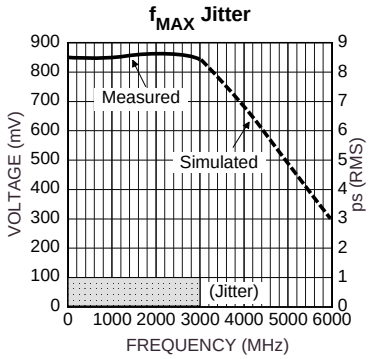


Figure 1. f_{MAX} and RMS Jitter

PRODUCT ORDERING CODE

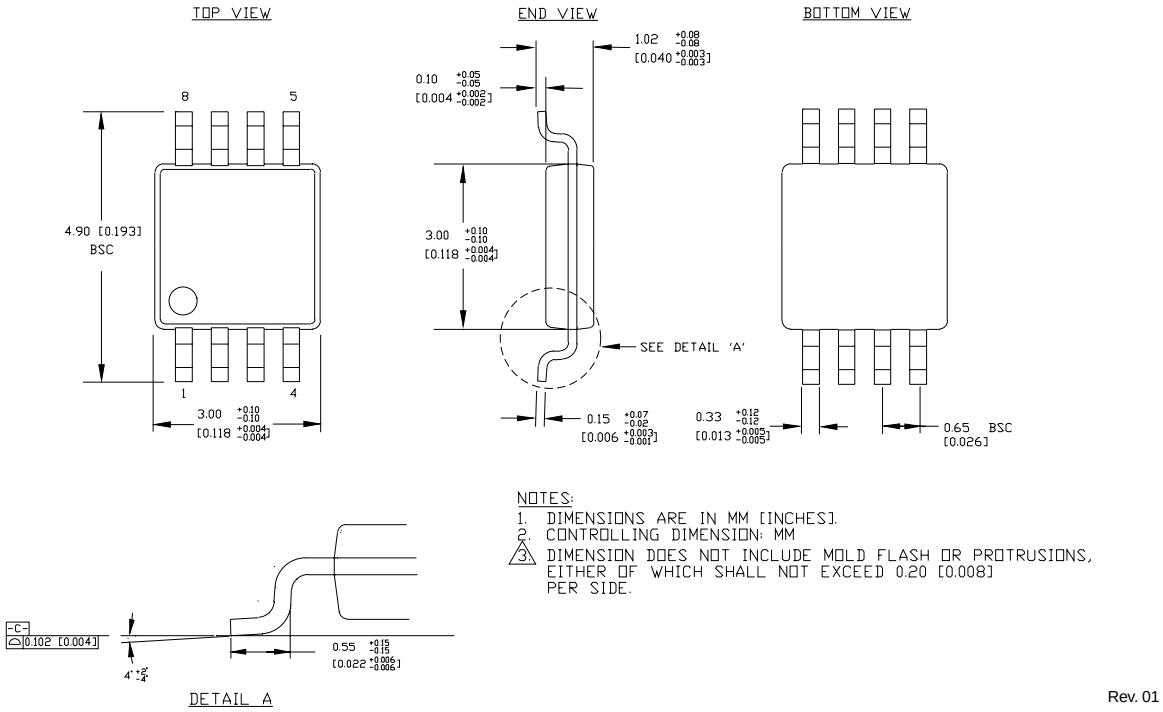
Ordering Code	Package Type	Operating Range	Package Marking
SY10EP32VZC	Z8-1	Commercial	HEP32V
SY10EP32VZCTR[1]	Z8-1	Commercial	HEP32V
SY100EP32VZC	Z8-1	Commercial	XEP32V
SY100EP32VZCTR[1]	Z8-1	Commercial	XEP32V
SY10EP32VKC	K8-1	Commercial	HP32
SY10EP32VKCTR[1]	K8-1	Commercial	HP32
SY100EP32VKC	K8-1	Commercial	XP32
SY100EP32VKCTR[1]	K8-1	Commercial	XP32

Ordering Code	Package Type	Operating Range	Package Marking
SY10EP32VZI[2]	Z8-1	Industrial	HEP32V
SY10EP32VZITR[1,2]	Z8-1	Industrial	HEP32V
SY100EP32VZI[2]	Z8-1	Industrial	XEP32V
SY100EP32VZITR[1,2]	Z8-1	Industrial	XEP32V
SY10EP32VKI[2]	K8-1	Industrial	HP32
SY10EP32VKITR[1,2]	K8-1	Industrial	HP32
SY100EP32VKI[2]	K8-1	Industrial	XP32
SY100EP32VKITR[1,2]	K8-1	Industrial	XP32

Note 1. Tape and Reel.

Note 2. Recommended for new designs.

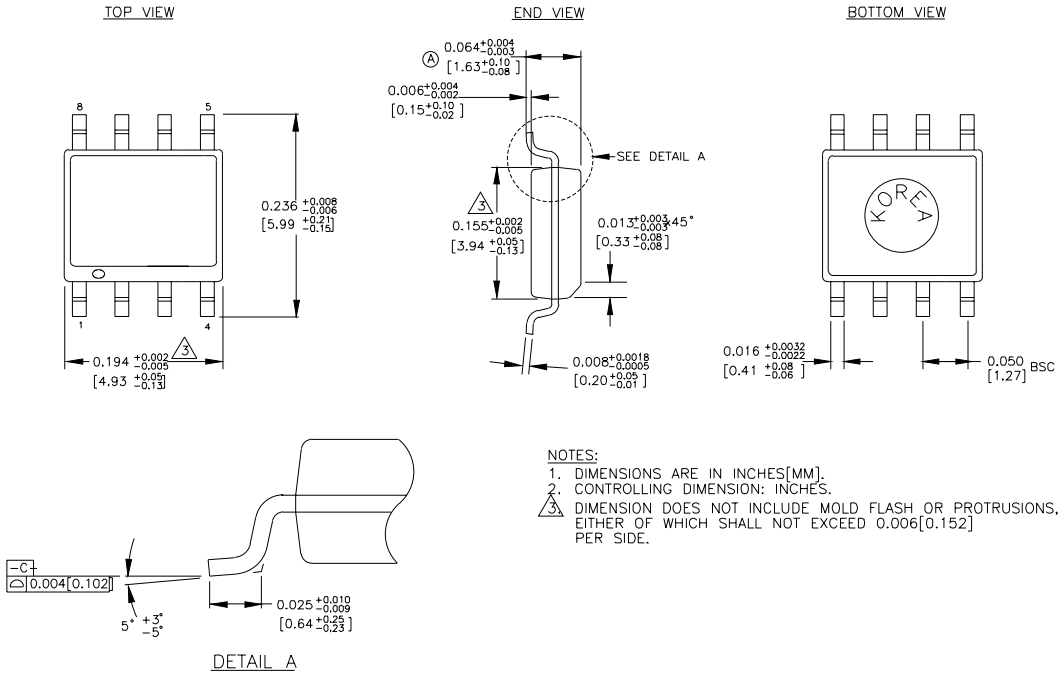
8 LEAD MSOP (K8-1)



NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

Rev. 01

8 LEAD SOIC .150" WIDE (Z8-1)



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