

FEATURES

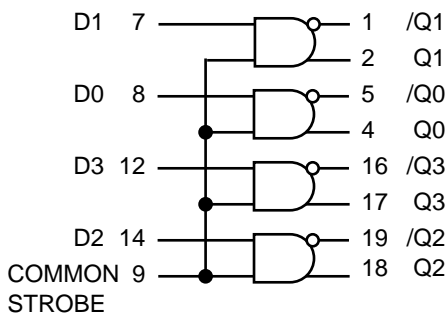
- Single 5V power supply
- All V_{CC} pins isolated on chip
- Differentially drive balanced lines
- t_{pd} 1.3ns typical
- Fully compatible with MC10H352
- Available in 20-pin PLCC package

DESCRIPTION

The SY10H352 is a quad translator for interfacing data between a CMOS logic section and the PECL section of digital systems when only a +5.0V VDC power supply is available. The SY10H352 has CMOS compatible inputs and PECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at a low logic level, it forces all true outputs to the PECL low logic state ($\approx +3.2V$) and all inverting outputs to the PECL high logic state ($\approx +4.1V$).

The SY10H352 can also be used with the SY10H350 to transmit and receive CMOS information differentially via balanced twisted pair lines.

BLOCK DIAGRAM

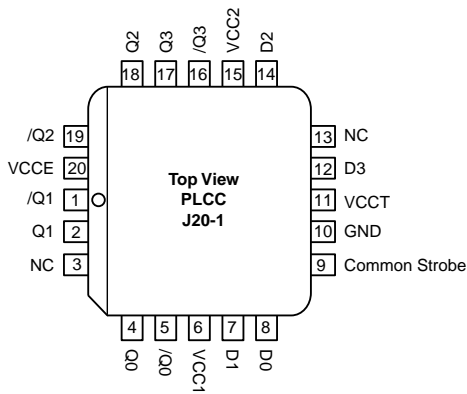


V_{CC} (+5 V_{DC}) = Pins 6, 11, 15, 20;
GND = Pin 10

PIN NAMES

| Pin | Function |
|---------------|----------------------|
| D0 – D3 | Inputs |
| Q0 – Q3 | Outputs |
| /Q0 – /Q3 | Inverted outputs |
| VCC1 | PECL V_{CC} (5.0V) |
| VCCE | PECL V_{CC} (5.0V) |
| VCCT | CMOS V_{CC} (5.0V) |
| VCC2 | PECL V_{CC} (5.0V) |
| Common Strobe | Common Strobe |
| GND | Ground |

PACKAGE/ORDERING INFORMATION



20-Pin PLCC (J20-1)

Ordering Information⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|--------------------------------|--------------|-----------------|--|-------------|
| SY10H352JC | J20-1 | Commercial | SY10H352JC | Sn-Pb |
| SY10H352JCTR ⁽²⁾ | J20-1 | Commercial | SY10H352JC | Sn-Pb |
| SY10H352JZ ⁽³⁾ | J20-1 | Commercial | SY10H352JZ with Pb-Free bar-line indicator | Matte-Sn |
| SY10H352JZTR ^(2, 3) | J20-1 | Commercial | SY10H352JZ with Pb-Free bar-line indicator | Matte-Sn |

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|--------------------|---|--------------|------|
| V _{CC} | Power Supply Voltage | -0.5 to +7.0 | V |
| I _{OUT} | Output Current –Continuous –Surge | 50 100 | mA |
| T _{LEAD} | Lead Temperature (soldering, 20sec.) | +260 | °C |
| T _{store} | Storage Temperature | -65 to +150 | °C |
| T _A | Operating Temperature | 0 to +85 | °C |

TRUTH TABLE

| CS | D | Q | /Q |
|------|------|---|----|
| H | L | L | H |
| H | H | H | L |
| H | Open | H | L |
| L | X | L | H |
| Open | L | L | H |
| Open | H | H | L |
| Open | Open | H | L |

Note:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICSV_{CC1} = V_{CC2} = V_{CC} = V_{CE} = V_{CT} = 4.75V to 5.25V

| Symbol | Parameter | T _A = 0°C | | T _A = +25°C | | | T _A = +85°C | | Unit | Condition |
|---------------------|---|----------------------|----------|------------------------|------|----------|------------------------|----------|------|-------------------------|
| | | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | | |
| I _{CC} | Power Supply Current ECL ⁽¹⁾ TTL ⁽²⁾ | — | 45 15 | — | — | 45 15 | — | 45 15 | mA | No output loads |
| I _R | Reverse Current (Pins 7, 8, 12, 14) | — | 20 | — | — | 20 | — | 20 | μA | |
| I _{INH} | Reverse Current, (Pin 9) | — | 80 | — | — | 80 | — | 80 | μA | |
| I _F | Forward Current (Pins 7, 8, 12, 14) | — | -0.6 | — | — | -0.6 | — | -0.6 | mA | |
| I _{INL} | Forward Current, (Pin 9) | — | -2.4 | — | — | -2.4 | — | -2.4 | mA | |
| V _{BR(in)} | Input Breakdown Voltage | 5.5 | — | 5.5 | — | — | 5.5 | — | V | |
| V _I | Input Clamp Voltage | — | -1.5 | — | — | -1.5 | — | -1.5 | V | I _{IN} = -18mA |
| V _{OH} | Output HIGH Voltage ⁽³⁾ | 3.98 | 4.16 | 4.02 | — | 4.19 | 4.09 | 4.28 | V | |
| V _{OL} | Output LOW Voltage ⁽³⁾ | 3.05 | 3.37 | 3.05 | — | 3.37 | 3.05 | 3.37 | V | |
| V _{IH} | Input HIGH Voltage | 3.15 | — | 3.15 | — | — | 3.15 | — | V | |
| V _{IL} | Input LOW Voltage | — | 1.5 | — | — | 1.5 | — | 1.5 | V | |

Notes:

1. Total I_{CC} at V_{CC1}, V_{CC2} and V_{CE}.
2. I_{CC} at I_{CT}.
3. These values are for V_{CC} = 5.0V. Level Specifications will vary 1:1 V_{CC}.

AC ELECTRICAL CHARACTERISTICS

VCC1 = VCC2 = VCCE = VCCT = 4.75V to 5.25V

| Symbol | Parameter | TA = 0°C | | TA = +25°C | | | TA = +85°C | | Unit | Condition |
|----------------------------------|--|----------|------|------------|------|------|------------|------|------|---------------|
| | | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | | |
| t _{PD} | Propagation Delay ⁽¹⁾ | 0.4 | 1.9 | 0.4 | — | 2.0 | 0.4 | 2.1 | ns | 50Ω to VCC-2V |
| t _r t _f | Output Rise/Fall Time (20% to 80%) | 0.4 | 1.9 | 0.4 | — | 2.0 | 0.4 | 2.1 | ns | 50Ω to VCC-2V |
| f _{MAX} | Maximum Input Frequency ⁽²⁾ | 150 | — | 150 | — | — | 150 | — | MHz | 50Ω to VCC-2V |

Notes:

1. Propagation delay is measured on this circuit from V_{CC2} on the input waveform to the 50% point on the output waveform.
2. These parameters are guaranteed but not tested.

SWITCHING WAVEFORM

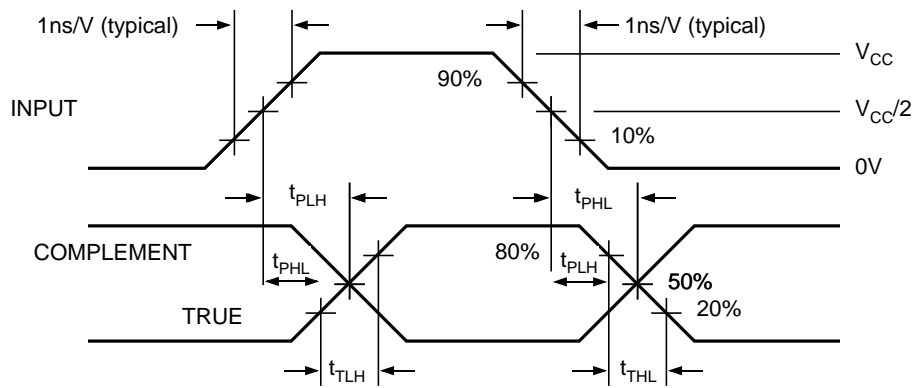
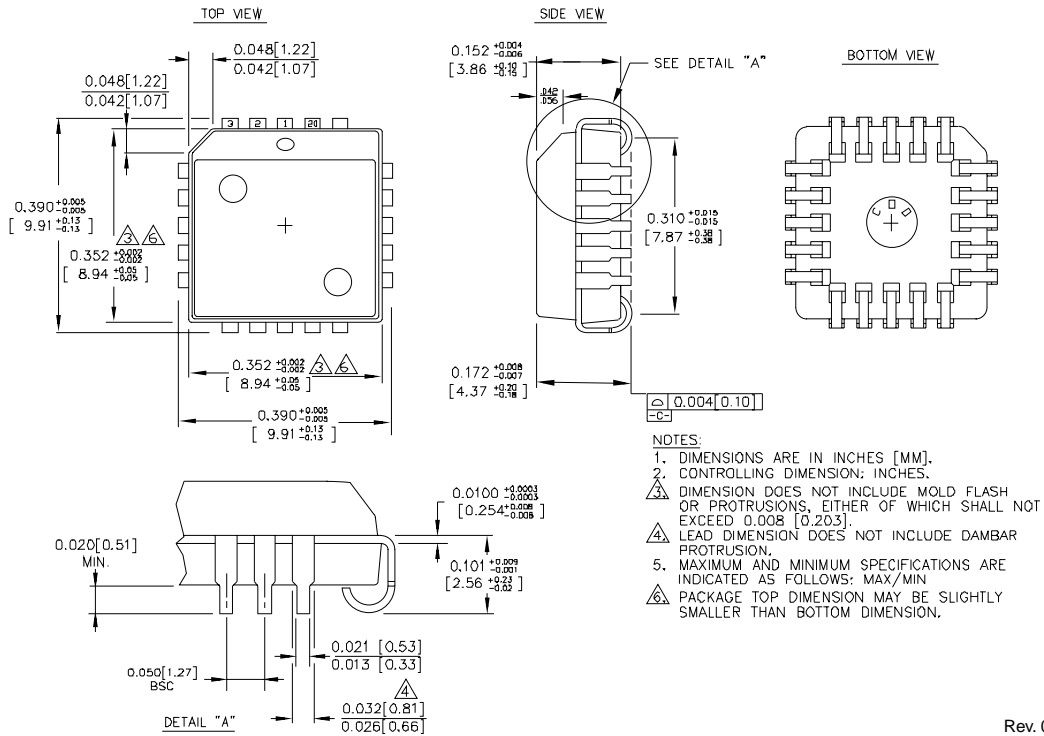


Figure 1. Propagation Delay and Transition Times

20-PIN PLASTIC LEADED CHIP CARRIER (J20-1)



Rev. 00

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