

FEATURES

- Input frequencies up to 135MHz
- PECL-to-TTL version of popular ECLinPS E111
- Guaranteed low skew specification
- Latched input
- Differential internal design
- VBB output VECL for single-ended operation
- Single +5V supply
- Reset/enable
- Extra TTL and ECL power/ground pins
- Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)
- Available in 28-pin PLCC package

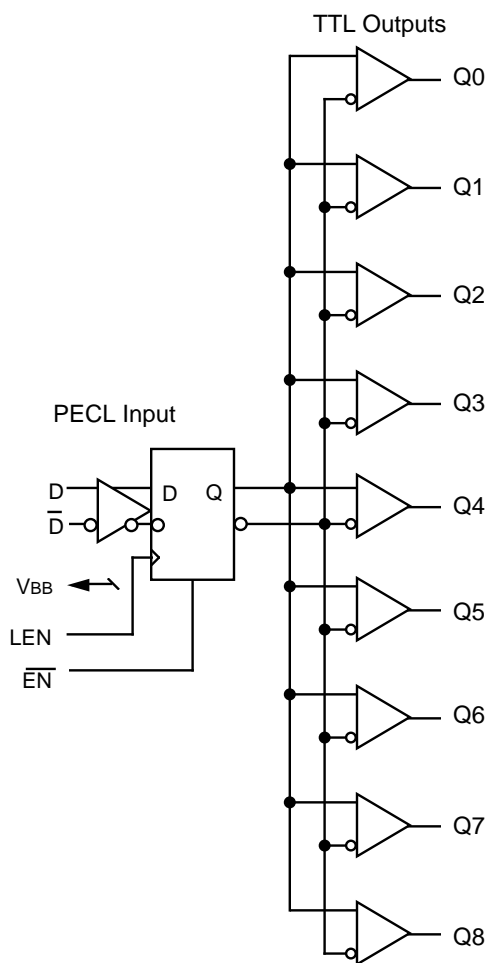
DESCRIPTION

The SY10/100H641 are single supply, low skew translating 1:9 clock drivers. Devices in the Micrel-Synergy H600 translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

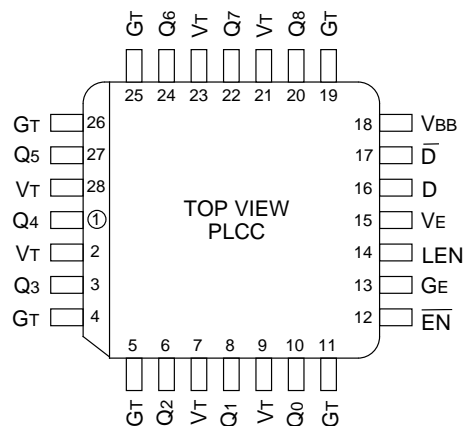
The devices feature a 24mA TTL output stage with AC performance specified into a 50pF load capacitance. A latch is provided on-chip. When LEN is LOW (or left open, in which case it is pulled LOW by the internal pull-downs), the latch is transparent. A HIGH on the enable pin (\overline{EN}) forces all outputs LOW.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
GT	TTL Ground (0V)
VT	TTL Vcc (+5.0V)
VE	ECL Vcc (+5.0V)
GE	ECL Ground (0V)
D, \overline{D}	Signal Input (PECL)
VBB	VBB Reference Output (PECL)
Q0 - Q8	Signal Outputs (TTL)
\overline{EN}	Enable Input (PECL)
LEN	Latch Enable Input (PECL)

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
VE (ECL) VT (TTL)	Power Supply Voltage	-0.5 to +7.0 -0.5 to +7.0	V
VI (ECL)	Input Voltage	0.0 to VEE	V
VOUT (TTL)	Disabled 3-State Output	0.0 to VCCT	V
IOUT (ECL)	Output Current - Continuous - Surge	50 100	mA
Tstore	Storage Temperature	-65 to +150	°C
TA	Operating Temperature	0 to +85	°C

TRUTH TABLE

D	LEN	EN	Q
L	L	L	L
H	L	L	H
X	H	L	Q0
X	X	H	L

NOTE:

- Do not exceed.

VCC AND CLOAD

Ranges to meet duty cycle requirement: $0^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. Output duty cycle measured relative to 1.5V.

Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
PW1	Ranges of Vcc and CL to meet min. pulse width (HIGH or LOW) at $f_{OUT} \leq 40\text{MHz}$	Vcc	4.75	5.0	5.25	V	All Outputs
		CL	10	—	50	pF	
		Pw	11	—	—	ns	
PW2	Ranges of Vcc and CL to meet min. pulse width (HIGH or LOW) at $f_{OUT} \leq 50\text{MHz}$	Vcc	4.875	5.0	5.125	V	All Outputs
		CL	15	—	27	pF	
		Pw	9.0	—	—	ns	

DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0\text{V} \pm 5\%$

Symbol	Parameter		TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
IEE	Power Supply Current	ECL	—	30	—	30	—	30	mA	VE Pin
ICCH		TTL	—	30	—	30	—	30		Total all VT pins
ICCL			—	35	—	35	—	35		

TTL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0\text{V} \pm 5\%$

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
VOH	Output HIGH Voltage	2.0	—	2.0	—	2.0	—	V	IOH = -15mA
VOL	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	IOL = 24mA
Ios	Output Short Circuit Current	-100	-225	-100	-225	-100	-225	mA	VOUT = 0V

10H ECL DC ELECTRICAL CHARACTERISTICS

VT = VE = 5.0V ± 5%

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I _{IH}	Input HIGH Current	—	225	—	175	—	175	μA	—
I _{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	μA	—
V _{IH}	Input HIGH Voltage ⁽¹⁾	3.830	4.160	3.870	4.190	3.940	4.280	V	VE = 5.0V
V _{IL}	Input LOW Voltage ⁽¹⁾	3.050	3.520	3.050	3.520	3.050	3.555	V	VE = 5.0V
V _{BB}	Output Reference Voltage ⁽¹⁾	3.620	3.730	3.650	3.750	3.690	3.810	V	VE = 5.0V

NOTE:1. V_{IH}, V_{IL} and V_{BB} are referenced to V_E and will vary 1:1 with the power supply. The levels shown are for V_E = +5.0V.**100H ECL DC ELECTRICAL CHARACTERISTICS**

VT = VE = 5.0V ± 5%

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I _{IH}	Input HIGH Current	—	225	—	175	—	175	μA	—
I _{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	μA	—
V _{IH}	Input HIGH Voltage ⁽¹⁾	3.835	4.120	3.835	4.120	3.835	4.120	V	VE = 5.0V
V _{IL}	Input LOW Voltage ⁽¹⁾	3.190	3.525	3.190	3.525	3.190	3.525	V	VE = 5.0V
V _{BB}	Output Reference Voltage ⁽¹⁾	3.620	3.740	3.620	3.740	3.620	3.740	V	VE = 5.0V

NOTE:1. V_{IH}, V_{IL} and V_{BB} are referenced to V_E and will vary 1:1 with the power supply. The levels shown are for V_E = +5.0V.**AC ELECTRICAL CHARACTERISTICS**

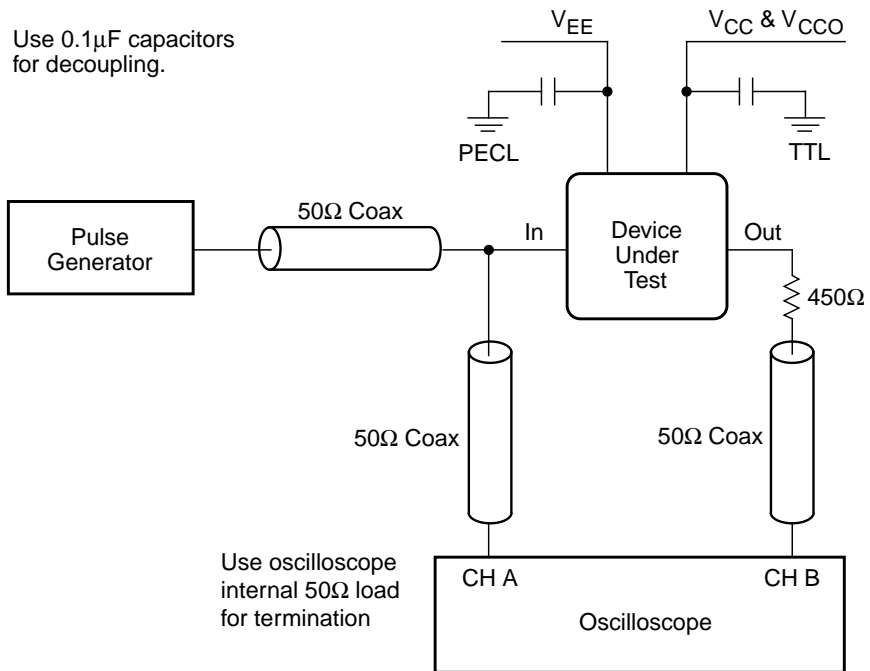
VT = VE = 5.0V ± 5%

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay D to Output	5.0	6.0	4.8	5.8	5.3	6.3	ns	CL = 50pF
t _{skpp}	Part-to-Part Skew ^(1,4)	—	1.0	—	1.0	—	1.0	ns	CL = 50pF
t _{skew++}	Within-Device Skew ^(2,4)	—	0.5	—	0.5	—	0.5	ns	CL = 50pF
t _{skew--}	Within-Device Skew ^(3,4)	—	0.5	—	0.5	—	0.5	ns	CL = 50pF
t _{PLH} t _{PHL}	Propagation Delay LEN to Output	4.9	6.9	4.9	6.9	5.0	7.0	ns	CL = 50pF
t _{PLH} t _{PHL}	Propagation Delay EN to Output	5.0	7.0	4.9	6.9	5.0	7.0	ns	CL = 50pF
t _r t _f	Output Rise/Fall Time 0.8V to 2.0V	—	1.7	—	1.7	—	1.7	ns	CL = 50pF
f _{MAX}	Maximum Input Frequency ^(5,6)	135	—	135	—	135	—	MHz	CL = 50pF
—	Pulse Width	1.5	—	1.5	—	1.5	—	ns	—
—	Recovery Time	1.25	—	1.25	—	1.25	—	ns	—
t _S	Set-up Time	0.5 (typ.)		0.5 (typ.)		0.5 (typ.)		ns	—
t _H	Hold Time	0.5 (typ.)		0.5 (typ.)		0.5 (typ.)		ns	—

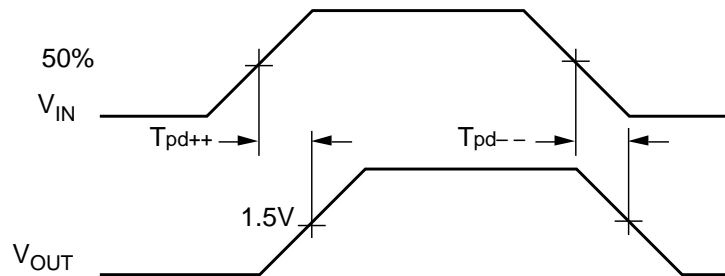
NOTES:

1. Device-to-Device Skew considering HIGH-to-HIGH transitions at common power supply voltage.
2. Within-Device Skew considering HIGH-to-HIGH transitions at common power supply voltage.
3. Within-Device Skew considering LOW-to-LOW transitions at common power supply voltage.
4. All skew parameters are guaranteed but not tested.
5. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
6. The f_{MAX} value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.

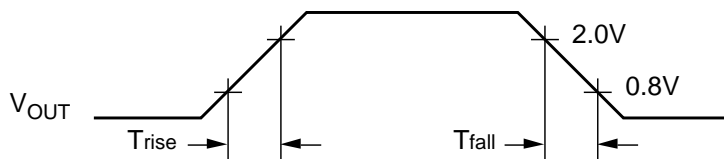
TTL SWITCHING CIRCUIT



ECL/TTL PROPAGATION DELAY — SINGLE ENDED



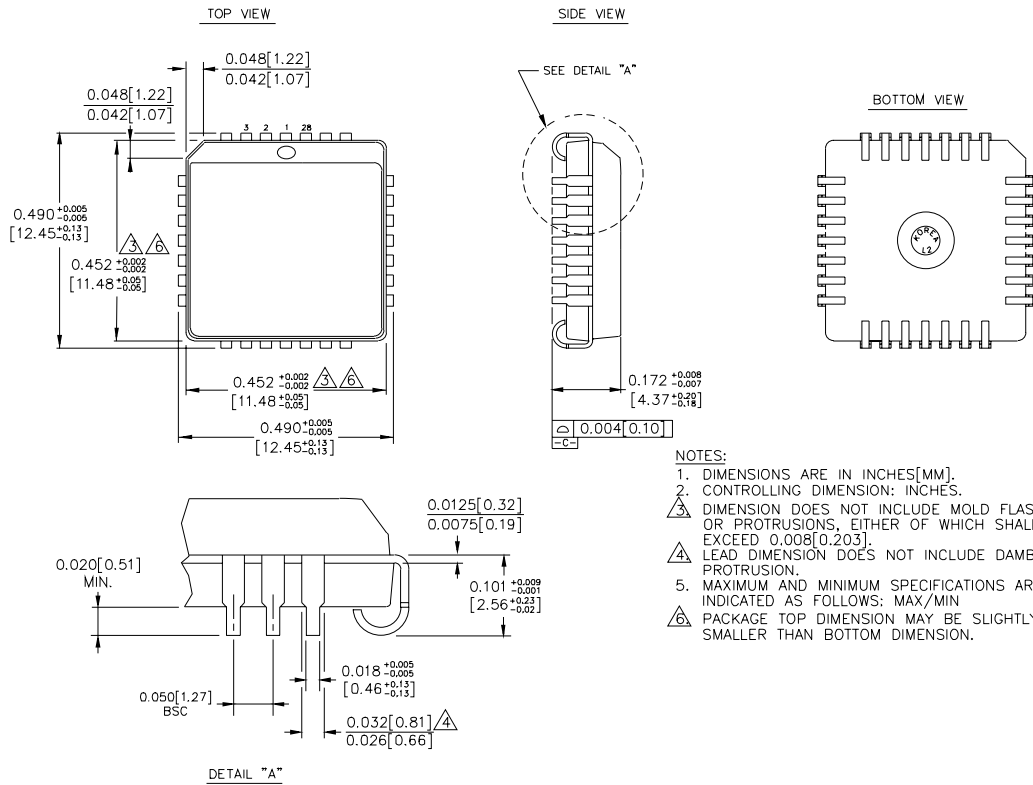
ECL/TTL WAVEFORMS: RISE AND FALL TIMES



PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H641JC	J28-1	Commercial
SY10H641JCTR	J28-1	Commercial
SY100H641JC	J28-1	Commercial
SY100H641JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



- NOTES:**
1. DIMENSIONS ARE IN INCHES[MM].
 2. CONTROLLING DIMENSION: INCHES.
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
 4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
 5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
 6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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