SY20018I

High-Efficiency, 1.5MHz,1A Synchronous Step-Down Regulator

General Description

The SY20018I high-efficiency 1.5MHz synchronous step-down DC/DC regulator operates over a wide input voltage range of 2.5V to 5.5V, and can deliver an output current up to 1A with a low quiescent current of 50μA. It integrates a main switch and a synchronous switch with very low $R_{DS(ON)}$ to minimize conduction loss. The 1.5MHz switching frequency allows for low output-voltage ripple, as well as small external inductor and capacitor values.

The SY20018I is highly integrated, so only the input and output capacitors, inductor, and feedback resistors need to be selected for the targeted application specifications.

The SY20018I is available in a compact SOT23-5 package.

Features

- 2.5V to 5.5V Input Voltage Range
- Up to 1A Output Current
- Low $R_{DS(ON)}$ for Internal Switches: 260mΩ Top, 160mΩ Bottom
- Low 50μA Quiescent Current
- High 1.5MHz Switching Frequency Minimizes Required External Components
- Constant-Off-Time and Peak-Current-Mode Control
- Internal Soft-Start Limits the Inrush Current
- 100% Dropout Operation
- Power-Good Indicator
- Hiccup Mode for Short-Circuit Protection
- Output Auto-Discharge Function
- RoHS-Compliant and Halogen-Free
- Compact Package: SOT23-5

Applications

- Set-Top Box
- USB Dongle
- Media Player
- Smartphone

Typical Application

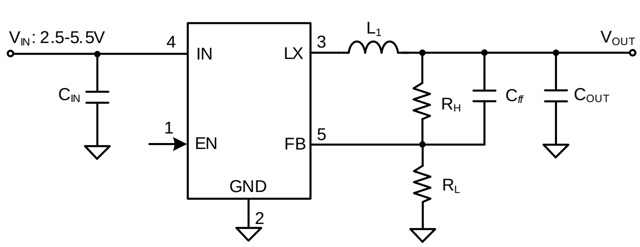


Figure 1.Typical Application Circuit

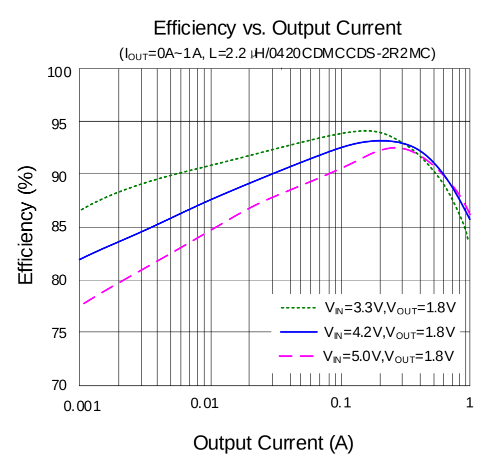


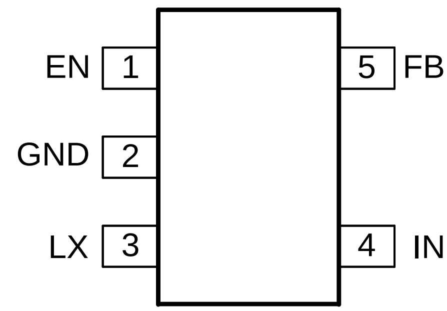
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY20018IAAC	SOT23-5 RoHS Compliant and Halogen Free	**bP*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	EN	Enable pin. Pull low to disable the device, pull high to enable. Do not leave this pin floating.
2	GND	Ground pin.
3	LX	Inductor pin. Connect this pin to the switching node of the inductor.
4	IN	Power input. Decouple this pin from the GND pin with at least a 10μF ceramic capacitor.
5	FB	Output feedback pin. Connect this pin to the center point of the output resistor-divider as shown in Figure 1. $V_{OUT} = 0.6 \times (1 + R_H/R_L)$

Block Diagram

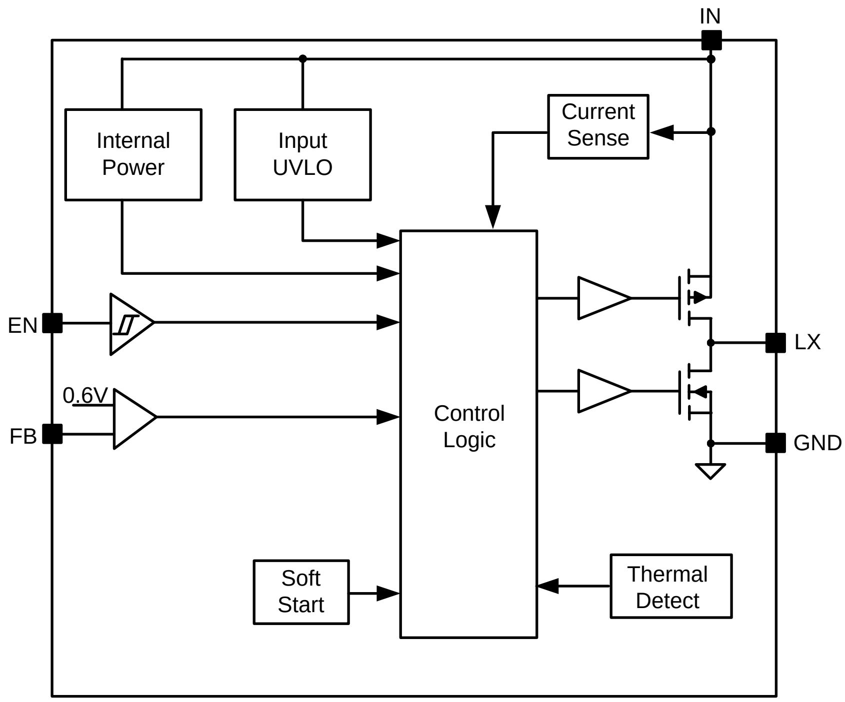


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	6	V
EN, FB	-0.3	IN + 0.6	
LX	-0.3	6	
LX, 40ns duration	-3	7	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	130	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	28	
P_D Power Dissipation T_A = 25°C	0.77	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	2.5	5.5	V
Output Voltage	0.6	5.5	
Output Current		1	A
Junction Temperature	-40	125	°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 1.8V, L = 2.2μH, C_{OUT} = 10μF, T_J = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage	V_{IN}		2.5		5.5	V
	UVLO, rising	$V_{IN,UVLO}$				2.5	V
	UVLO, hysteresis	$V_{IN,HYS}$			150		mV
	Shutdown current	I_{SHDN}	V_{EN} = 0V		0.1	1	μA
	Quiescent current	I_Q	V_{FB} = 105% × V_{REF}		50	60	μA
FB	Reference voltage	V_{REF}	I_{OUT} = 0.5A, CCM	0.591	0.6	0.609	V
	Input current	I_{FB}	V_{EN} = 2V, V_{FBS} = 1V	-50	0	50	nA
Power Switch	On resistance	$R_{DS(ON)HS}$		180	260	340	mΩ
	Current limit	$I_{LMT,HS}$		1.5		2.5	A
Synchronous Rectifier	On resistance	$R_{DS(ON)LS}$		100	160	220	mΩ
Discharge FET resistance		R_{DIS}			50		Ω
Enable(EN)	Input voltage high	$V_{EN,H}$		1.2			V
	Input voltage low	$V_{EN,L}$				0.4	V
Soft-Start (SS)	Turn-on delay time	$t_{ON,DLY}$	From EN high to LX start switching		300		μs
	Soft-start time	t_{SS}	V_{OUT} from 0% to 100%		700		μs
Switching Frequency		f_{SW}	I_{OUT} = 0.5A, CCM		1		MHz
Min ON Time		$t_{ON,MIN}$			60		ns
Maximum Duty Cycle		D_{MAX}		100			%
Thermal Shutdown Temperature		T_{SD}			160		°C
Thermal Shutdown Hysteresis		T_{HYS}			20		°C

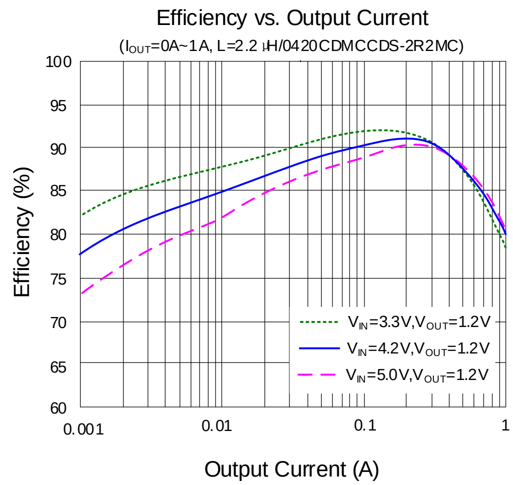
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

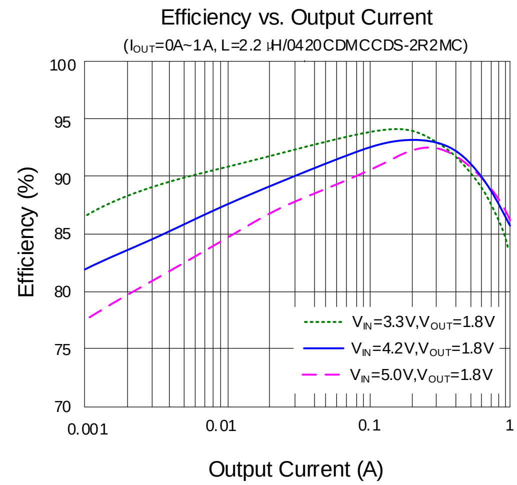
Note 2: θ_{JA} of SY20018I DFC is measured in the natural convection at T_A = 25ºC on a 2oz two-layer Silergy evaluation board. Pin 3 is the case position for θ_{JC} measurement.

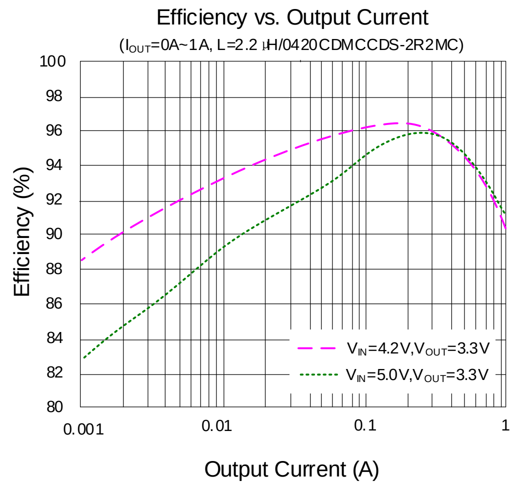
Note 3: The device is not guaranteed to function outside its operating conditions.

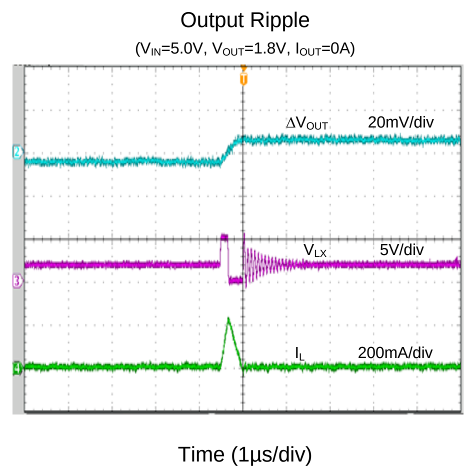
Typical Performance Characteristics

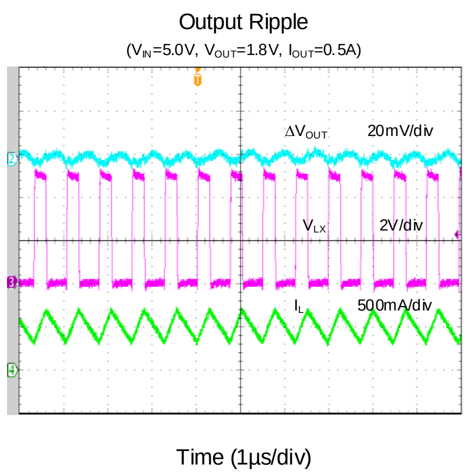
(T_A = 25°C, V_{IN} = 5V, V_{OUT} = 1.8V, L = 1.0μH, C_{OUT} = 22μF, unless otherwise noted)

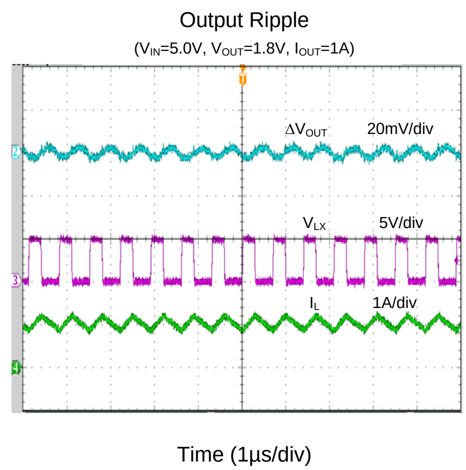






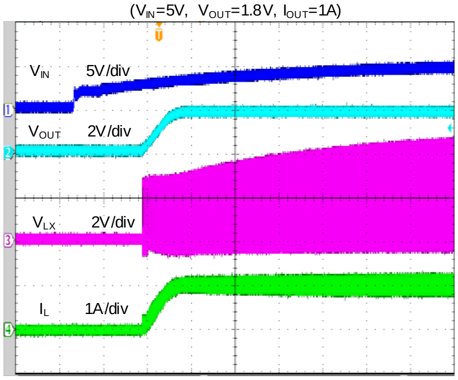






Startup from V_{IN}

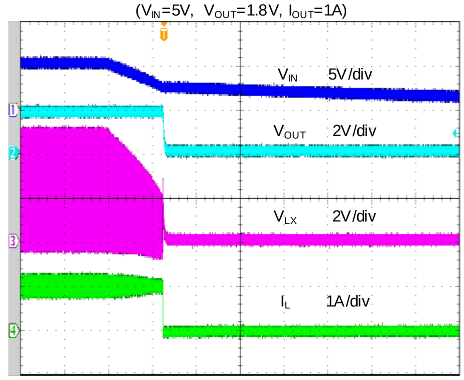
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=1A)



Time (800 µs/div)

Shutdown from V_{IN}

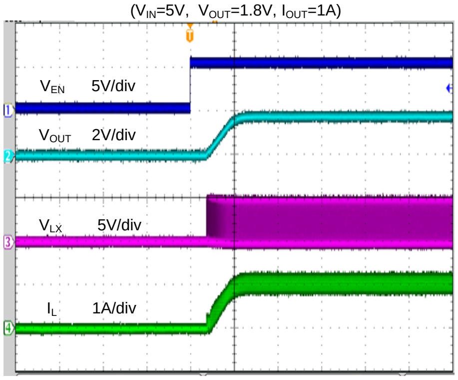
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=1A)



Time (800 µs/div)

Startup from Enable

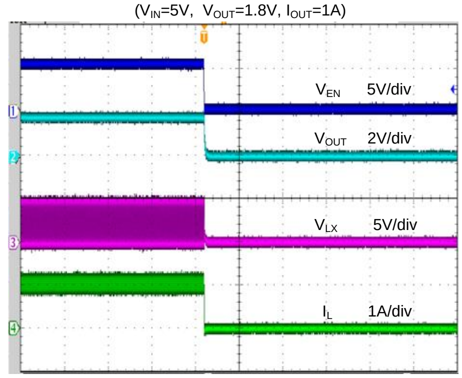
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=1A)



Time (800µs/div)

Shutdown from Enable

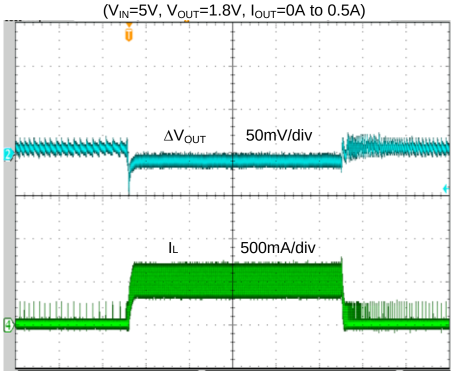
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=1A)



Time (800µs/div)

Load Transient

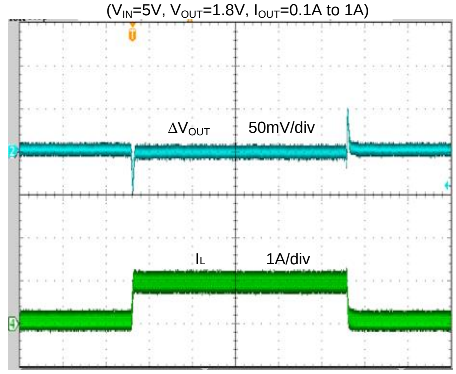
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A to 0.5A)



Time (200µs/div)

Load Transient

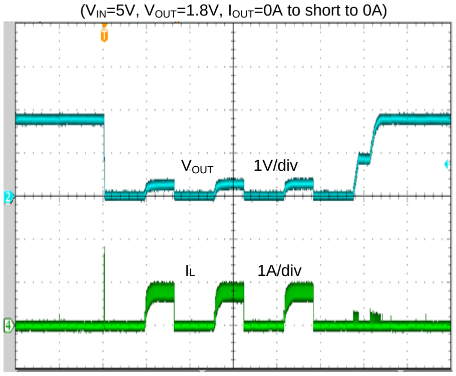
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0.1A to 1A)



Time (200µs/div)

Short Circuit Protection

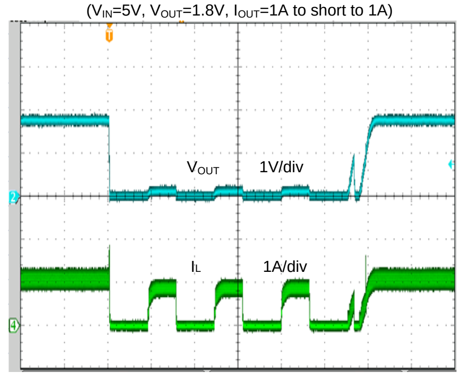
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A to short to 0A)



Time (2ms/div)

Short Circuit Protection

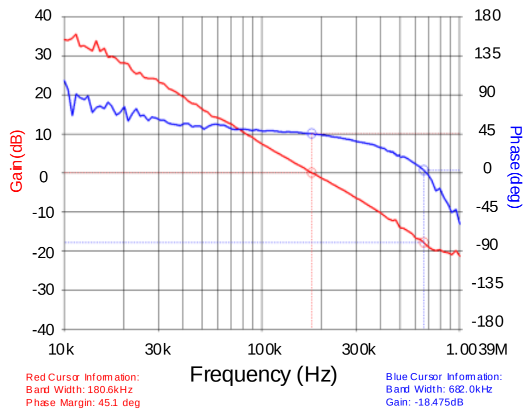
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=1A to short to 1A)



Time (2ms/div)

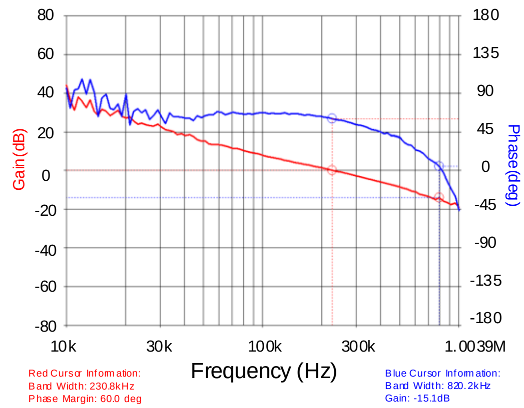
Bode Plot

(V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=1A)



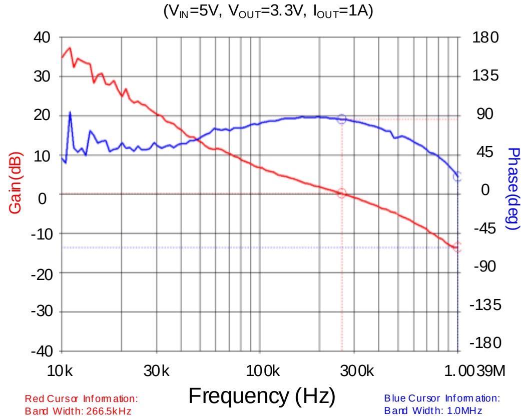
Bode Plot

(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=1A)



Bode Plot

(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1A)



Operation

The SY20018I high-efficiency 1.5MHz synchronous step-down DC/DC regulator operates over a wide input voltage range of 2.5V to 5.5V, and can deliver an output current up to 1A with a low quiescent current of 50μA. To minimize conduction loss, it integrates a main switch and a synchronous switch with very low $R_{DS(ON)}$. The 1.5MHz switching frequency allows for low output-voltage ripple, as well as small external inductor and capacitor values.

The SY20018I employs a constant-off-time and peak-current-mode control strategy. When the top FET's current-sense signal reaches internal V_{COMP}, the top FET turns off and the bottom FET turns on for a fixed period of time (constant t_{OFF}). t_{OFF} is internally calculated according to the input voltage, output voltage, and desired switching frequency (f_{SW}):

$$t_{OFF} = \frac{1 - V_{OUT}/V_{IN}}{f_{SW}}$$

The bottom FET turns off after a period of t_{OFF}.

Application Information

The SY20018I is highly integrated, so only the input capacitor C_{IN}, the output capacitor C_{OUT}, the output inductor L, and the feedback resistors R_H and R_L need to be selected for the targeted application specifications.

Feedback Resistor-Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. A value between 1kΩ and 1MΩ is recommended for both resistors. If R_L is chosen as 100kΩ, for example, then R_H can be calculated as follows:

$$R_H = \frac{(V_{OUT} - 0.6\,V) \times R_L}{0.6V}$$

Input Capacitor C_{IN}

For the best performance, select a typical X5R or better grade ceramic capacitor with a 6.3V rating, and at least 10μF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by C_{IN} and the IN/GND pins.

When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10μF X5R capacitor is sufficient in most applications.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use an X5R or better grade ceramic capacitor with a 6.3V rating, and capacitance of at least 10μF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed.

The output voltage ripple at the switching frequency is caused by the inductor-current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Output Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY20107A has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > \mathrm{I}_{\mathrm{OUT,MAX}} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor with DCR less than 50mΩ to achieve good overall efficiency.

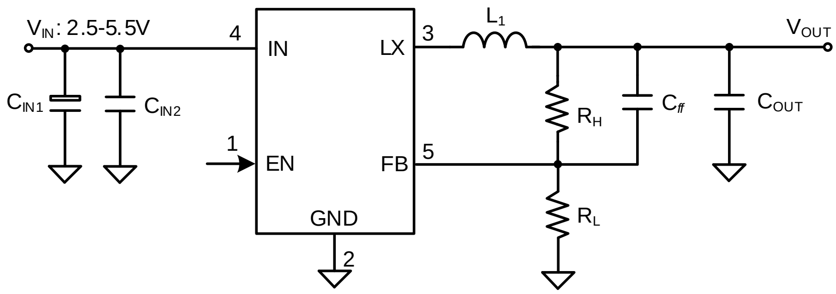
Short-Circuit Protection

The SY20018I integrates hiccup-mode short-circuit protection. If the output voltage falls below 50% of the regulation level, the internal soft-start node and the error amplifier output will be reset immediately, and the SY20018I will operate in hiccup mode. The hiccup frequency is approximately 300Hz and the hiccup duty cycle is approximately 45%. If the hard short is removed, the SY20018I will return to normal operation.

Load-Transient Considerations

The SY20018I integrates compensation components to achieve fast transient response and improved stability. In some applications, adding a ceramic capacitor (feed-forward capacitor C_{ff}) in parallel with R_H may further speed up the load-transient response, and is therefore recommended for applications with large load-transient step requirements.

Application Schematic (V_{OUT} = 1.8V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
L1	2.2µH Inductor	0420CDMCCDS-2R2MC	Sumida
C_{IN1}	100µF/25V(electrolytic capacitor)		
C_{IN2}	10µF/6.3V, 0603, X5R	C1608X5R0J106M	TDK
C_{OUT}	10µF/6.3V, 0603, X5R	C1608X5R0J106M	TDK
C_{ff}	22pF/50V, 0603, X5R	C1608C0G1H220J	TDK
R_H	100kΩ, 1%, 0603		
R_L	49.9kΩ, 1%, 0603		

Recommend Components for Typical Applications

V_{OUT} (V)	R_H (kΩ)	R_L (kΩ)	C_{FF} (pF)	L/(Rated/Saturating Current)	C_{OUT}
1.2	49.9	49.9	22	2.2µH/(12A/15A)	10µF/6.3V/X5R,0603
1.8	100	49.9	22	2.2µH/(12A/15A)	10µF/6.3V/X5R,0603
3.3	100	22.1	22	2.2µH/(12A/15A)	10µF/6.3V/X5R,0603

Layout Design

For optimal design, follow these PCB layout considerations:

- For minimum noise and maximum efficiency, place the following components close to the IC: C_{IN}, L, R_H and R_L.
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows.
- C_{IN} must be close to pins IN and GND. Minimize the loop area formed by C_{IN}, V_{IN}, and GND.
- To reduce potential noise:
  - Minimize the PCB copper area connected to the LX pin.
  - R_H, R_L, and the trace connected to the FB pin must **not** be adjacent to the LX net on the PCB layout.
  - If the system chip interfacing with the EN pin has a high impedance state during shutdown mode, and the IN pin is connected directly to a power source such as a Li-ion battery, add a 1MΩ pulldown resistor between the EN and GND pins to prevent noise from falsely triggering the regulator during shutdown mode.

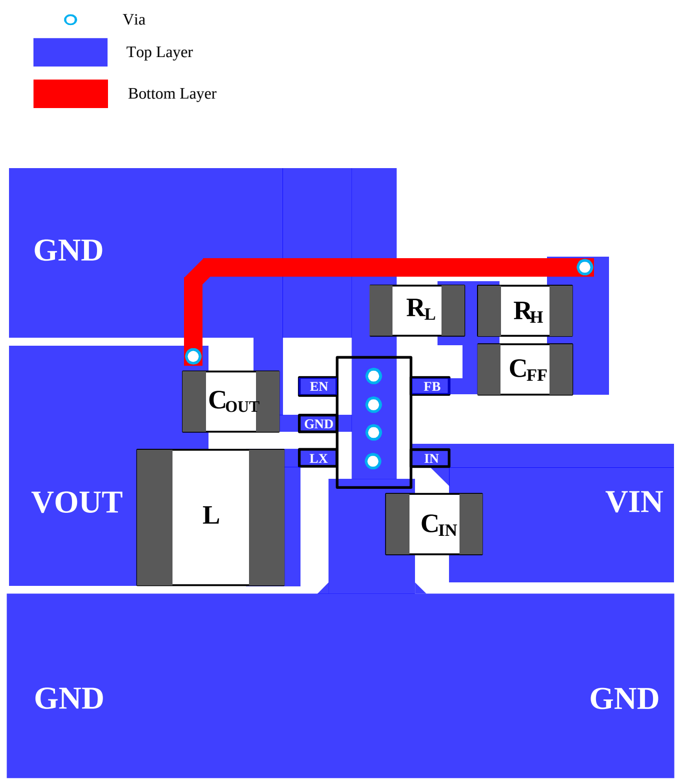
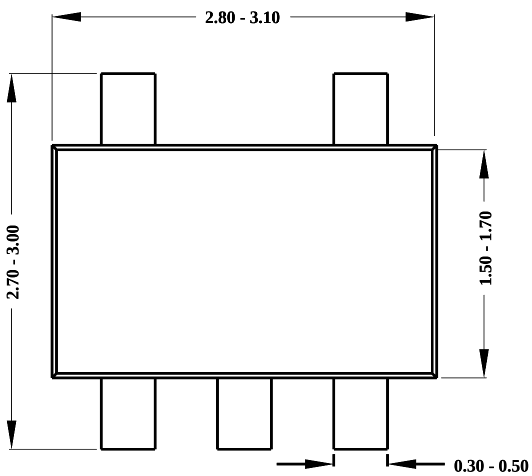
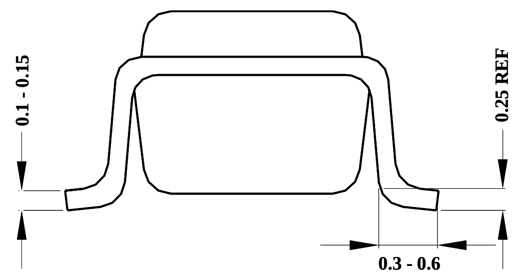
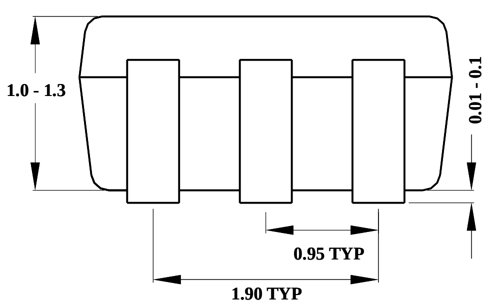


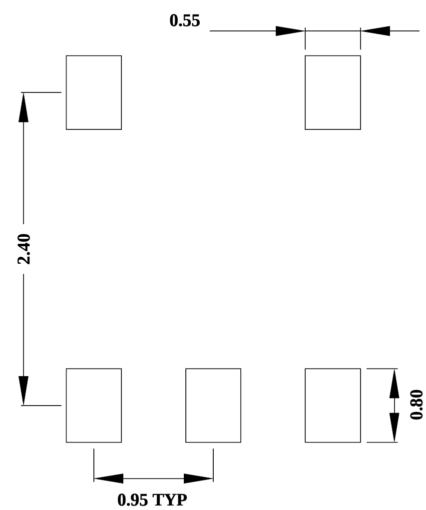
Figure 4. Recommended PCB Layout

SOT23-5 Package Outline and PCB Layout Design







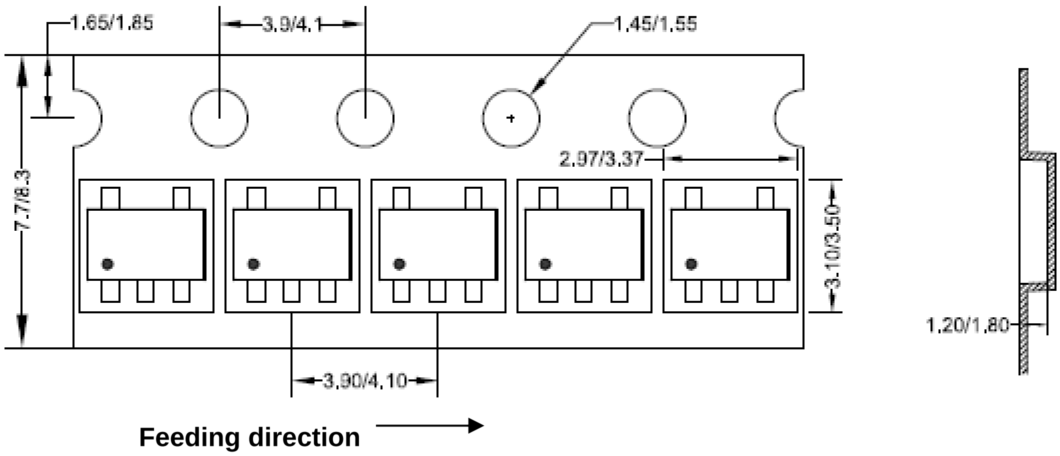


Recommended pad layout
(reference only)

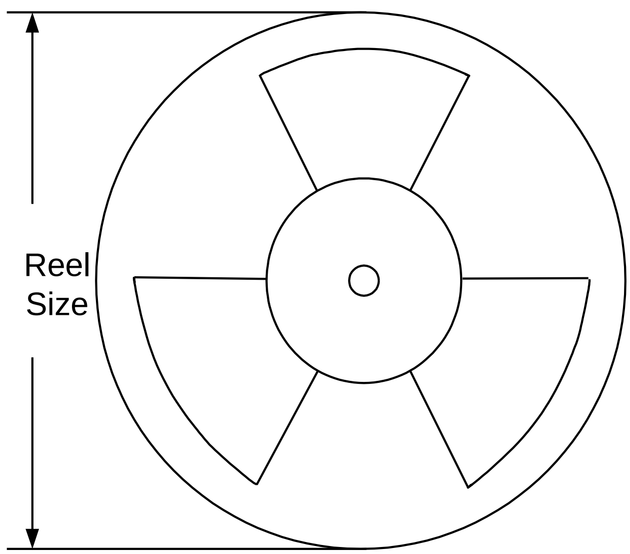
Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Taping and Reel Specification

SOT23-5 taping orientation



Carrier tape and reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-5	8	4	7"	280	160	3000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Feb.11, 2019	Revision 1.0	Product Release
Feb.11, 2018	Revision 0.9	Initial Release

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