SY20268

High Efficiency 1MHz, 6A Synchronous Step Down Regulator

General Description

The SY20268 is a high efficiency 1MHz synchronous step-down DC/DC regulator capable of delivering up to 6A output current.

The SY20268 operates over a wide input voltage range from 2.7V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Ordering Information

SY20268 □(□ □)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package Type	Note
SY20268QMC	QFN2×2-10	----

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 35/15mΩ
- 2.7-5.5V Input Voltage Range
- Pseudo-constant Frequency: 1MHz
- External Adjustable Soft-start Limits the Inrush Current
- Power Good Indicator
- Output Auto Discharge at Shutdown
- Latch-off Protection under Short-circuit and OVP Conditions
- RoHS Compliant and Halogen Free
- Compact Package: QFN2×2-10
- Built-in Over-temperature Protection.

Applications

- Notebook PC
- Server

Typical Applications

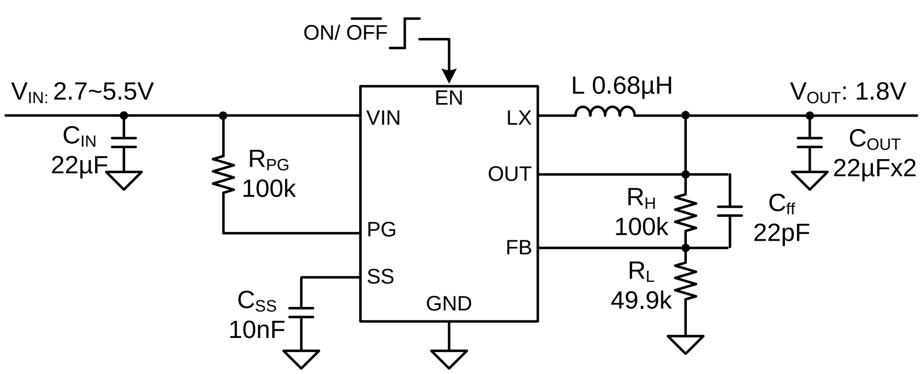
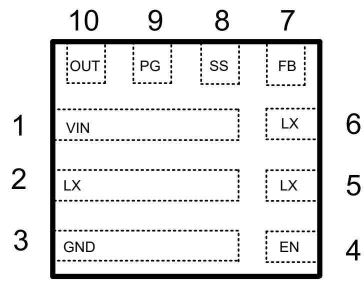


Figure1. Schematic Diagram

Pinout (top view)



(QFN2×2-10)

Top Mark: SY20268QMC: KT*xyz* **(**Device code: KT; ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
VIN	1	Power input pin. Decouple this pin to the GND pin with a 22μF ceramic capacitor.
LX	2,5,6	Inductor pin. Connect this pin to the switching node of the inductor.
GND	3	Ground pin.
EN	4	Enable control pin. Pulled high to turn on. Do not leave this pin floating.
FB	7	Feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure1) to program the output voltage: $V_{OUT}=0.6V\times(1+R_H/R_L)$
SS	8	Soft-start programming pin. Connect a capacitor from this pin to the ground to program the soft-start. $t_{SS}=C_{SS}\times10^5$ s. If the SS is floating, minimum soft-start time is 200μs.
PG	9	Power good indicator (Open-drain output). Low if the output < 90% of the regulation voltage; High otherwise. Connect a pull-up resistor to the input.
OUT	10	Output voltage sensing pin.

Block Diagram

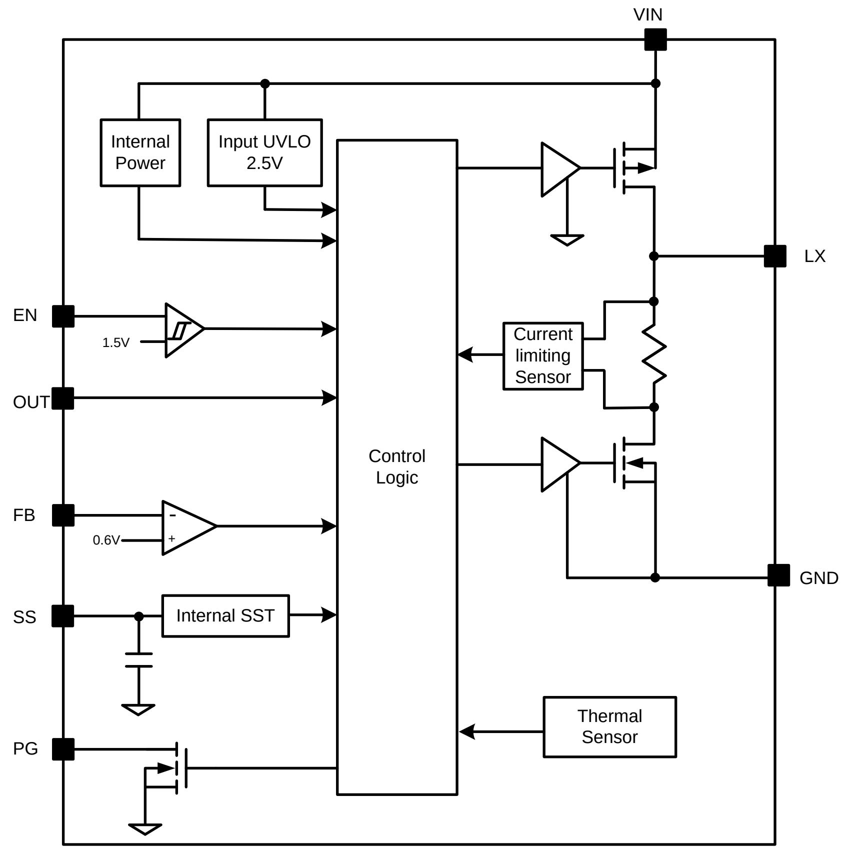


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage --- -0.3V to 6.0V
LX Voltage-- -0.3V (*1) to 6V (*2)
All other pins -- -0.3V to V_{IN} + 0.6V
Power Dissipation, P_D@ T_A=25°C QFN2×2-10--2.5W
Package Thermal Resistance (Note 2)
θ_{JA} --- 50°C/W
θ_{JC} --- 10°C/W
Junction Temperature Range -- 150°C
Lead Temperature (Soldering, 10 sec.) --- 260°C
Storage Temperature Range -- -65°C to 150°C
(*1) LX Voltage Tested Down to -5V<10ns
(*2) LX Voltage Tested Up to +7V<50ns

Recommended Operating Conditions (Note 3)

Supply Input Voltage -- 2.7V to 5.5V
Junction Temperature Range --- -40°C to 125°C
Ambient Temperature Range -- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 2.5V, L = 0.68µH, C_{OUT} = 22µF×2, T_A = 25°C, I_{MAX} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.7		5.5	V
Shutdown Current	I_{SHDN}	EN=0		0.1	1	µA
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%		50		µA
Feedback Reference Voltage	V_{REF}		0.594	0.6	0.606	V
PG Rising Threshold to Regulation Level Ratio				90		%
OVP Latch-off Protection Threshold	V_{OVP}			120		%
OVP Latch-off Protection Delay Time				40		µs
PFET R_{ON}	$R_{DS(ON),P}$			35		mΩ
NFET R_{ON}	$R_{DS(ON),N}$			15		mΩ
Valley Current Limit	I_{LIM}		6		7.5	A
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				2.65	V
UVLO Hysteresis	V_{HYS}			0.2		V
ON Time	t_{ON}	V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=1A		240		ns
Min OFF Time				130		ns
Max Duty	D_{MAX}			80		%
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis				15		°C
Output Discharge Resistor	R_{DSCH}			70		Ω

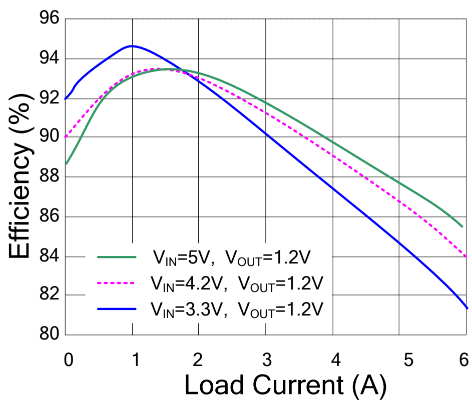
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy evaluation board.

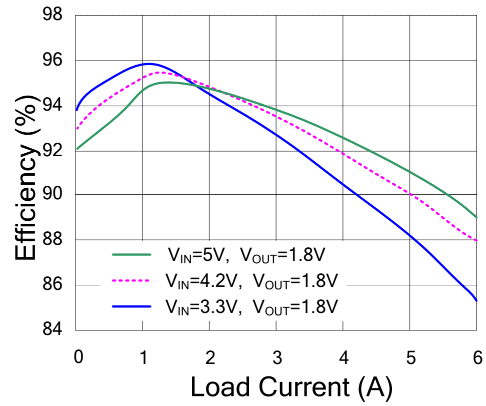
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

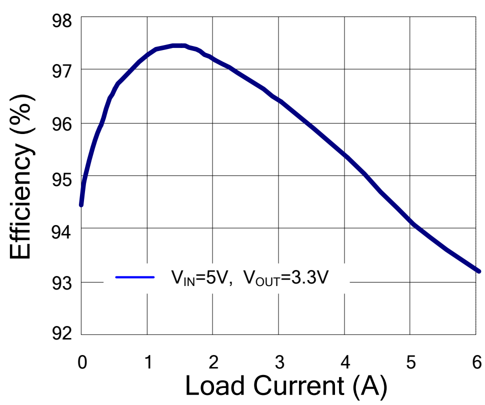
Efficiency vs. Load Current



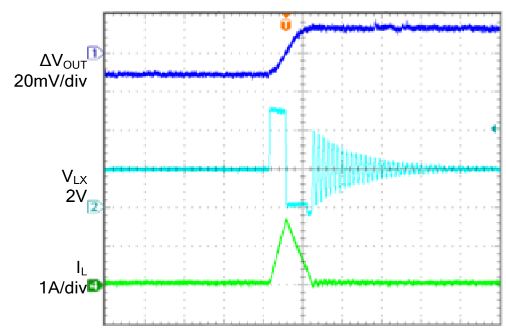
Efficiency vs. Load Current



Efficiency vs. Load Current

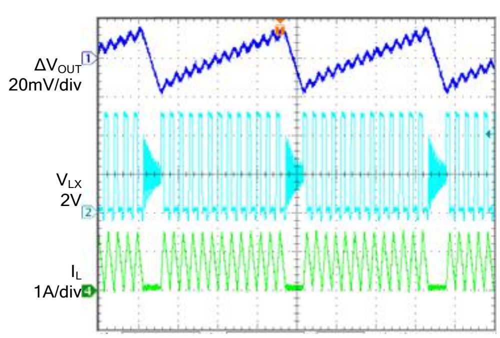


Output Ripple
(V_{IN}=5V, V_{OUT}=1.8V, Null Load)



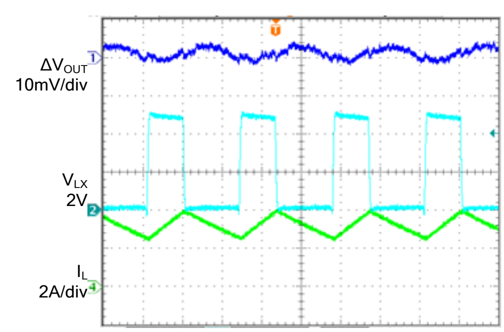
Time (1us/div)

Output Ripple
(V_{IN}=5V, V_{OUT}=1.8V,I_O=0.6A)



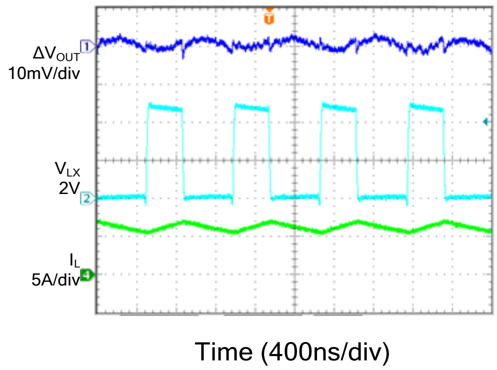
Time (4us/div)

Output Ripple
(V_{IN}=5V, V_{OUT}=1.8V, I_O=3A)

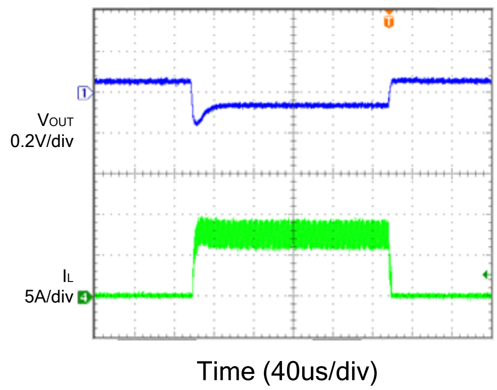


Time (400ns/div)

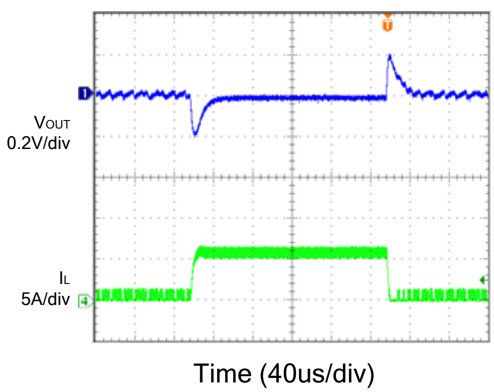
Output Ripple
(V_{IN}=5V, V_{OUT}=1.8V, I_O=6A)



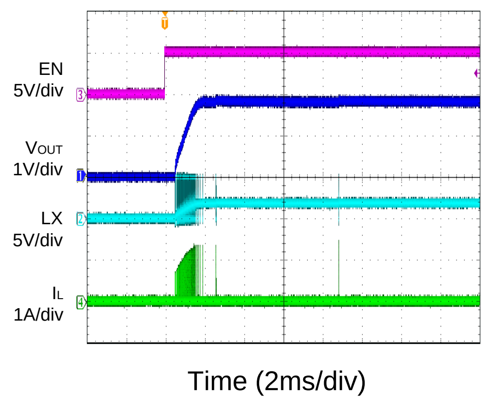
Load Transient
(V_{IN}=5V, V_{OUT}=1.8V, I_O=0-3A)



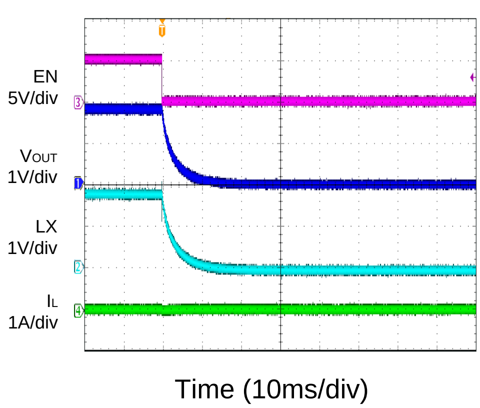
Load Transient
(V_{IN}=5V, V_{OUT}=1.8V, I_O=0.6-6A)



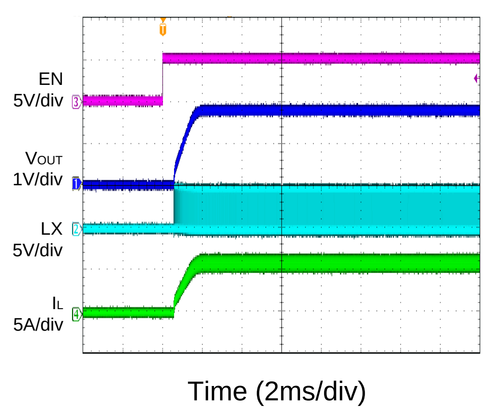
Startup from Enable
(V_{IN}=5V, V_{OUT}=1.8V,C_{SS}=10nF, Null Load)



Shutdown from Enable
(V_{IN}=5V, V_{OUT}=1.8V, Null Load)

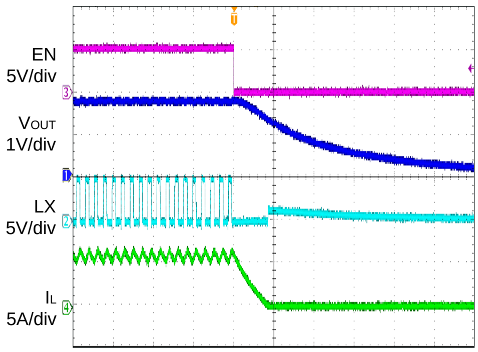


Startup from Enable
(V_{IN}=5V, V_{OUT}=1.8V, C_{SS}=10nF, I_O=6A)



Shutdown from Enable

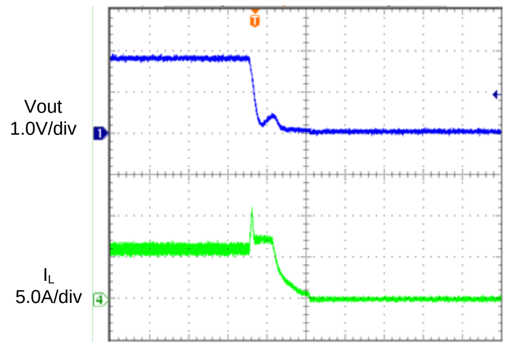
(V_{IN}=5V, V_{OUT}=1.8V, I_O=6A)



Time (4us/div)

Hard Short Protection

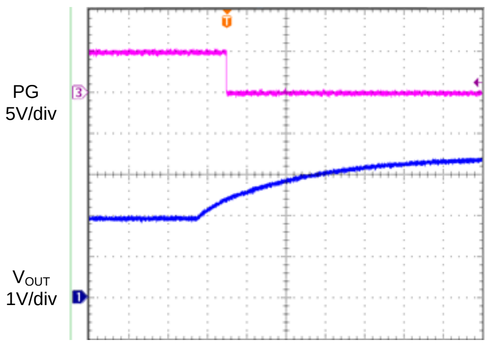
(V_{IN}=5V,V_{OUT}=1.8V,I_{Load}=6A To Short)



Time (1ms/div)

OVP Latch Off

(V_{IN}=5V,V_{OUT}=1.8V,Null Load)



Time (200us/div)

Operation

The SY20268 is a synchronous Buck regulator that integrates the PWM control, top and bottom switches on the same die to minimize the switching losses and conduction losses. With ultra low $R_{DS(ON)}$ power switches and proprietary PWM control, this regulator achieves a higher efficiency with high switching frequency to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

The SY20268 provides protection functions such as cycle-by-cycle current limit and thermal shutdown protection. The SY20268 will sense the output voltage conditions for the fault protection.

If the DC output voltage is about 3% over the regulation level, both switches will turn off and remain in this off state. If the DC voltage is about 20% over the regulation level, the IC will be latched-off after about 40μs delay time for the over voltage protection. If the DC voltage is below 33% of the regulation level, the IC will be latched-off after a short delay time for the short circuit protection.

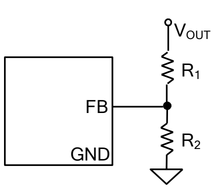
Applications Information

Because of the high integration in the SY20268, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the inductor L and the feedback resistors (R_1 and R_2) need to be selected for the targeted applications.

Feedback Resistor Divider R_1 and R_2

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is recommended for both resistors. If R_1=100kΩ is chosen, then R_2 can be calculated to be:

$$R_2 = \frac{0.6R_1}{V_{OUT} - 0.6} (\Omega)$$



Input Capacitor C_{IN}

This ripple current through the input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1\text{-}D)} \ (A)$$

This formula has a maximum at $V_{IN}=2\times V_{OUT}$ condition, where $I_{CIN\_RMS}=I_{OUT}/2$.

With the maximum load current at 6A, a typical X5R or better grade ceramic capacitor with 6.3V rating and greater than 22μF capacitance can handle this ripple current well. To minimize the potential noise problem, this ceramic capacitor should be placed really close to the VIN and the GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and the VIN/GND pins.

Output Capacitor C_{OUT}

Both steady state ripple and transient requirements must be taken into account when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor with 6.3V rating and greater than two 22μF capacitors.

Output Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN\_MAX})}{f_{SW} \times I_{OUT\_MAX} \times 40\%} (H)$$

Where f_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

The SY20268 is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1\text{-}V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<15mΩ to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During the shutdown, the SY20268 shutdown current drops to lower than 0.1µA. Driving the EN pin high (>1.5V) will turn on the IC again.

Power Good Indication

PG is an open-drain output pin. Connect an above 100k pull-up resistor to the VIN. The PG pin will output high immediately after the output voltage exceeds 90% of the normal output voltage.

Soft-start Programming

The SY20268 provides an external soft-start pin that gradually raises the output voltage. The soft-start time can be programmed by the external capacitor across the SS pin and the GND. The soft-start time is calculated as:

$$tss = MAX(200us, Css \times 10^5 s)$$

If a 10nF capacitor is used, the typical soft-start will be 1ms. If leaving the SS pin floating, the internal soft-start time will be 200µs.

Load Transient Considerations:

The SY20268 integrates the compensation components to achieve good stability and fast transient responses. Adding a 22pF~220pF ceramic capacitor in parallel with R_1 may further speed up the load transient responses.

Layout Design:

To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.

2) The decoupling capacitor of the VIN must be placed close enough to the pins. The loop area formed by the capacitors and the GND must be minimized.

3) The PCB copper area associated with the LX pin must be minimized to improve the noise immunity.

4) The components R_1, R_2 and the trace connecting to the FB/OUT pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to the FB/OUT pin.

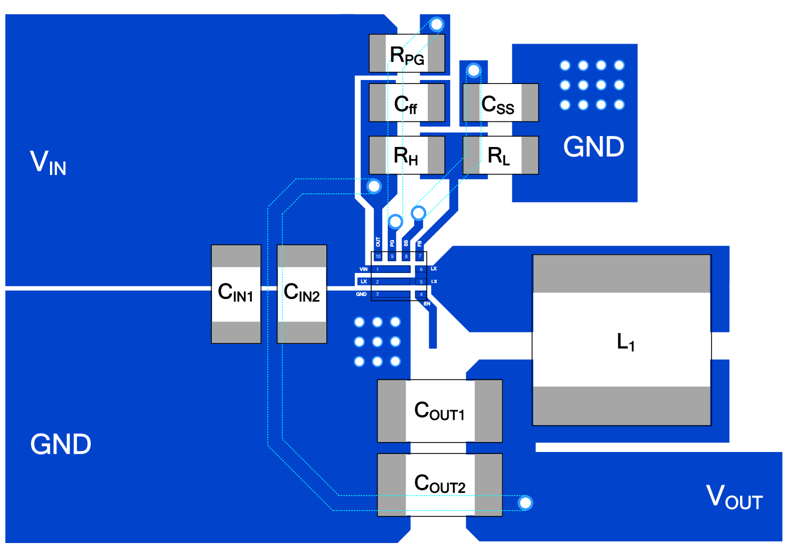
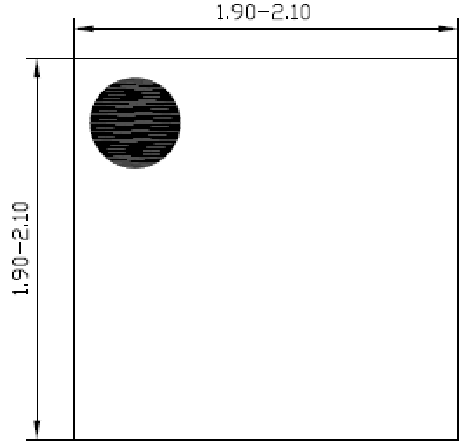
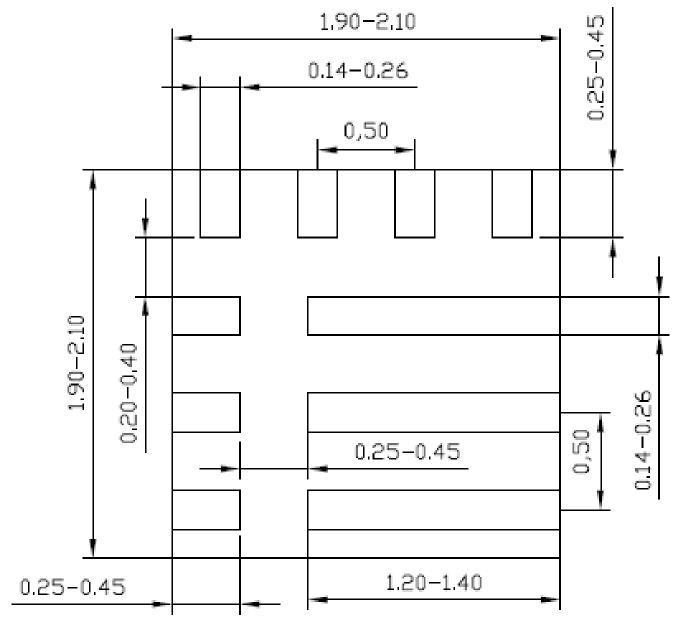


Figure3. PCB Layout Suggestion

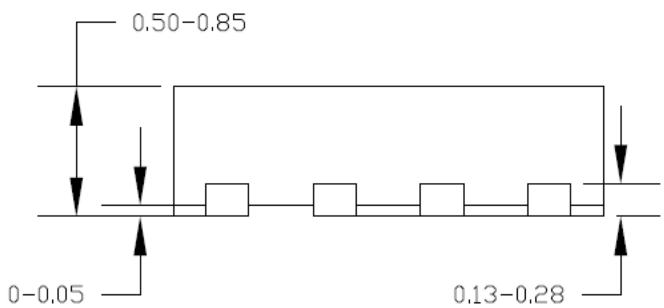
QFN2×2-10 Package Outline



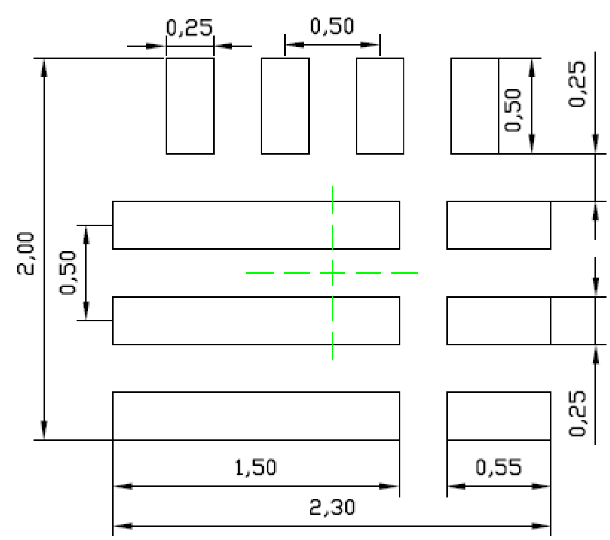
Top View



Bottom View



Side View

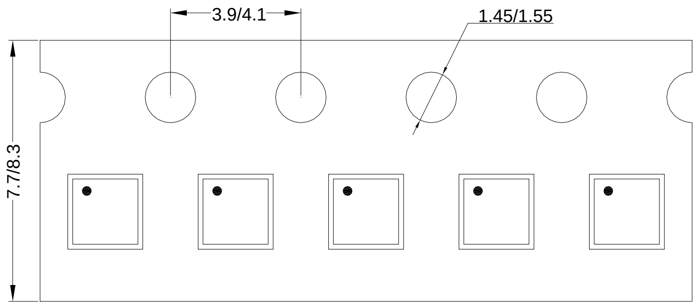


Recommended PCB Layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr**

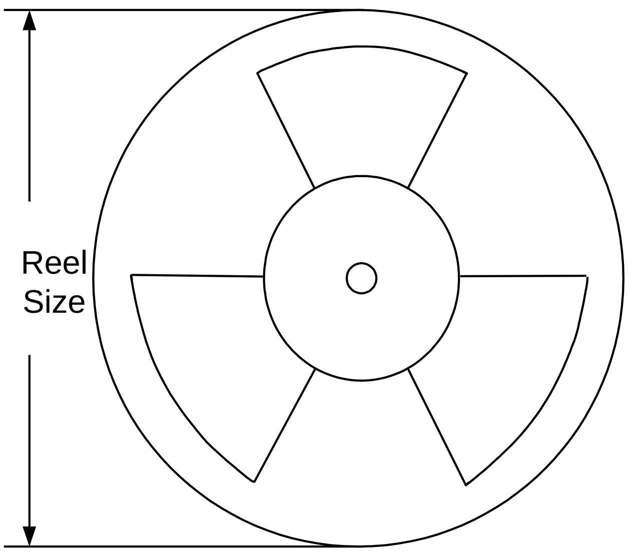
Taping & Reel Specification

1. QFN2×2-10 taping orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2×2	8	4	7"	400	160	3000

3. Others: NA

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