SY20516A

High Efficiency, 1MHz，1.2A Buck-Boost DC/DC Regulator

General Description

The SY20516A operates over an input voltage range from 2.6V to 5.5V, and can provide up to 1.2A to the load.

The device uses a 1MHz fixed frequency, pulse-width-modulation (PWM) architecture to obtain high efficiency, while enabling a small solution size. Under light load, the part switches automatically to PFM mode to maintain high efficiency.

The output voltage can be configured between 2.6V and 3.8V using a resistor divider. A soft-start circuit limits the power-up inrush current, and can be configured using an external capacitor. A simple RC series compensation network ensures stable operation across the range of loads and input voltages.

The device has an I_Q of 60 µA (typ.). During shutdown, the load is disconnected from the battery, and the quiescent current is reduced to 0.1 µA (typ.)

The SY20516A is designed to supply systems powered by either a two cell or three cell alkaline, Ni-Cd or Ni-MH battery, or a single cell Li-Ion or Li-polymer battery.

The device is available in a 3mm×3mm DFN package.

Features

- 2.6V to 5.5V Input Voltage Range
- 1.2A Output Current capability
- 1 MHz Fixed Frequency Operation
- 60 µA Quiescent Current (no load, typ.)
- 0.1 µA Shutdown Current (typ.)
- Seamless transition between operating modes
- Output disconnect during shutdown
- Application configurable soft-start
- Power Good Indicator
- Built in thermal, output short UVLO and OVP protections.
- Compact Package: DFN3×3-14

Applications

- Two cell and three cell alkaline, Ni-Cd or Ni-MH, or single cell Li batteries used in portable applications
- Handheld Instruments
- MP3/MP4 Players
- Digital Cameras/Camcorders
- IoT devices

Typical Application

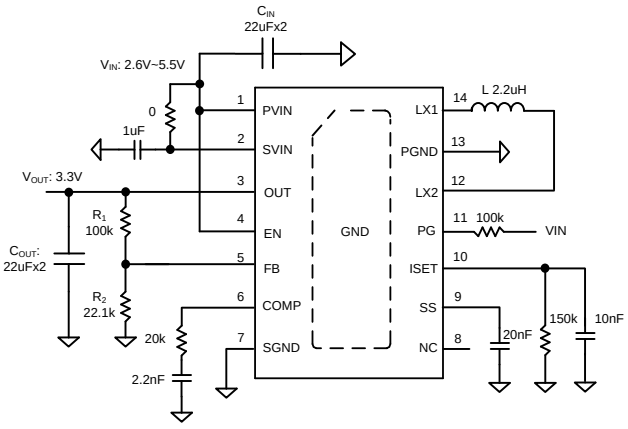


Figure 1. Schematic diagram

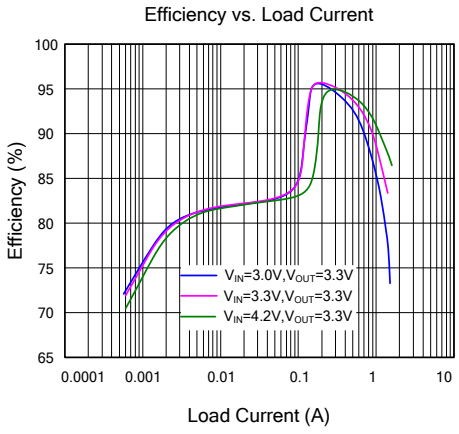
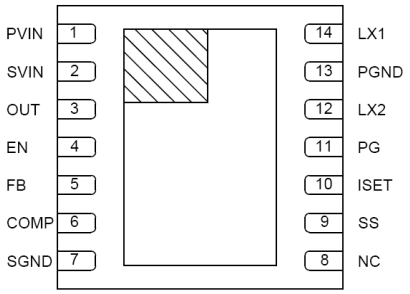


Figure 2. Efficiency

Ordering Information

Ordering Part Number	Package type	Top Mark
SY20516ADPC	DFN3×3-14 RoHS-Compliant and Halogen-Free	**WQ*xyz***

Pinout (top view)



Pin Description

Pin Name	Pin Number	Description
PVIN	I	Power input pin. Decouple this pin to GND with at least a 22μF ceramic cap. Minimize the loop area formed by input cap, PVIN pin and GND paddles.
SVIN	2	Signal power input pin. Decouple this pin to GND with at least a 1μF ceramic cap.
OUT	3	Output of the synchronous rectifier. Decouple this pin to GND with at least a 22μF ceramic cap. Minimize the loop area formed by output cap, OUT pin and GND paddles.
EN	4	Enable control. Pull high to turn on. Internal integrated with 1MΩ pull-down resistor.
FB	5	Output feedback pin. Connect this pin to the center point of the output resistor divider to program the output voltage.
COMP	6	External compensation for voltage loop.
SGND	7	Signal ground pin.
NC	8	Not connected.
SS	9	Connect this pin to a soft-start capacitor to program soft-start time.
ISET	10	Apply a resistor and capacitor parallel network to sense the output average current. If V_{ISET} is lower than 0.1V, IC will go into PFM mode. Do not let it floating. Tie to ground for forced PWM operation.
PG	11	Power good indicator.
LX2	12	Inductor connection 2. Connect this node to the switching node of the inductor.
PGND	13	Power ground pin.
LX1	14	Inductor connection 1 Connect this node to the switching node of the inductor.
GND	Paddle	Power ground.

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
OUT	-0.3	4	V
All Other Pins	-0.3	6	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	38	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	8	
P_D Power Dissipation T_A = 25°C	3.3	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Supply Input Voltage	2.6	5.5	V
Output Voltage	2.6	3.8	
Junction Temperature	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 4.2V, V_{OUT} = 3.3V, L =2.2μH, C_{OUT} = 22μF×2, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.6		5.5	V
Output Voltage Range	V_{OUT}		2.6		3.8	V
Quiescent Current	I_Q	I_{OUT}=0, EN=1, ISET=150kΩ, FB=105%×V_{REF}		60	100	μA
Shutdown Current	I_{SHDN}	EN=0		0.1	1	μA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
NFET $R_{DS(ON)}$	$R_{DS(ON)1}$			100		mΩ
PFET $R_{DS(ON)}$	$R_{DS(ON)2}$			100		mΩ
Input Peak Current Limit	I_{LIM}		3.5	4		A
Output Negative Current Limit	I_{NEG}			-1		A
Soft-start Current	I_{SS}	Soft-start time: $t_{ss} = \frac{0.7V}{I_{ss}} \times C_{ss}$		5		μA
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Rising Threshold	V_{UVLO}			2.45	2.55	V
UVLO Hysteresis	V_{HYS}			0.2		V
PG Under-voltage Threshold	$V_{FB,UV}$			0.48		V
PG Over-voltage Threshold	$V_{FB,OV}$			0.72		V
Output Current Sense	I_{SET}	I_{OUT}=1A		5		μA
Output Over Voltage Protection	V_{OVP}			125		%
OVP Protection Delay Time	t_{OVP_delay}			16		μs
ISET Pin Threshold for PFM Mode	V_{PFM}		0.08	0.1	0.12	V
Oscillator Frequency	f_{OSC}	I_{OUT}=1.0A	0.8	1.0	1.2	MHz
Min Duty Cycle		Boost & Buck		10		%
Max Duty Cycle		Boost & Buck		90		%
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

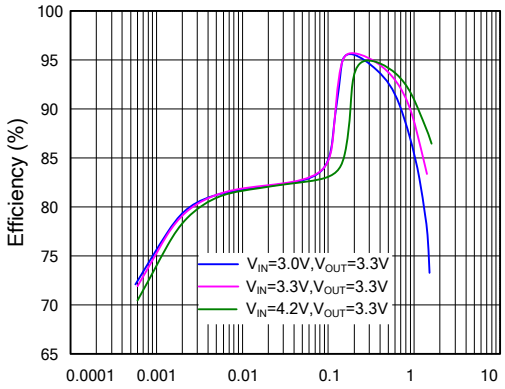
Note 2: θ_{JA} is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of DFN3X3-14 packages is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

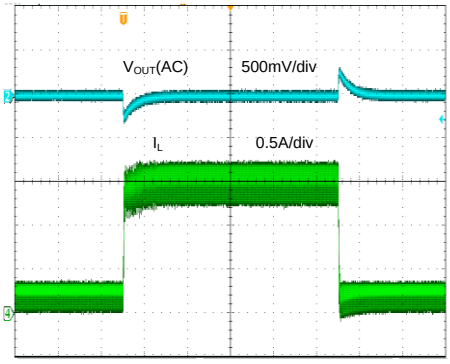
(T_A = 25°C, V_{OUT} = 3.3V, L =2.2μH, C_{OUT} =44μF, unless otherwise specified.)

Efficiency vs. Load Current



Load Transient

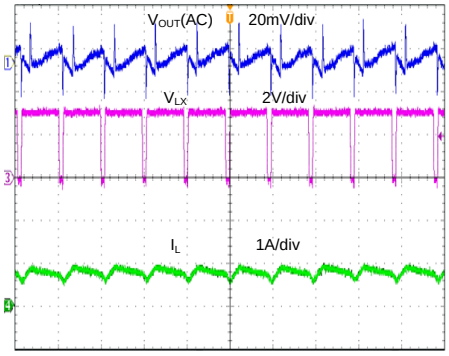
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{LOAD}=0.2~1.2A)



Time (200μs/div)

Output Ripple

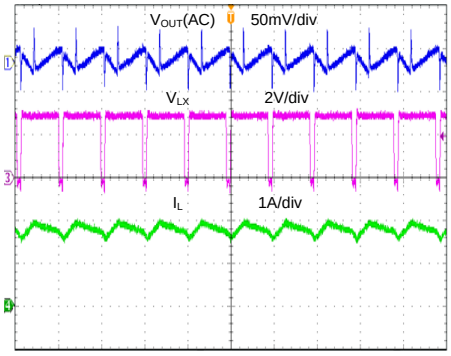
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{LOAD}=0.6A)



Time (1μs/div)

Output Ripple

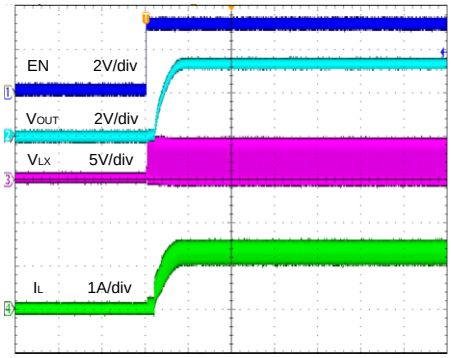
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{LOAD}=1.2A)



Time (1μs/div)

Startup From Enable

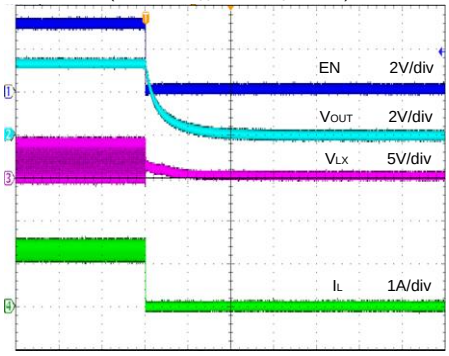
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{LOAD}=1.2A)



Time (2ms/div)

Shutdown From Enable

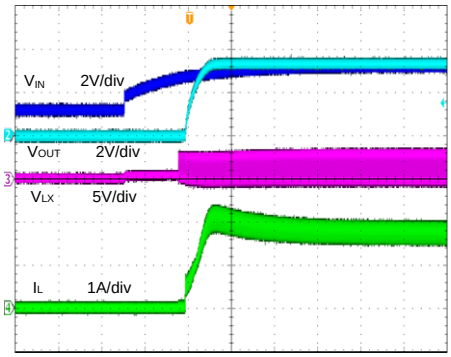
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{LOAD}=1.2A)



Time (200μs/div)

Startup From V_{IN}

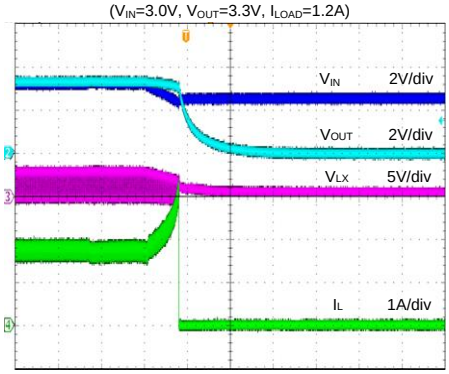
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{LOAD}=1.2A)



Time (2ms/div)

Shutdown From V_{IN}

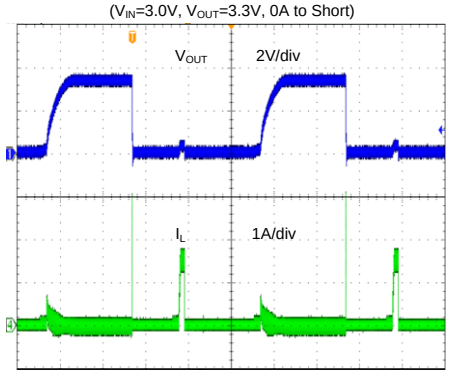
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{LOAD}=1.2A)



Time (200μs/div)

Short Circuit Protection

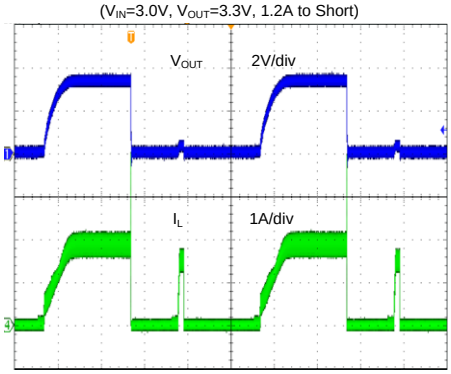
(V_{IN}=3.0V, V_{OUT}=3.3V, 0A to Short)



Time (2ms/div)

Short Circuit Protection

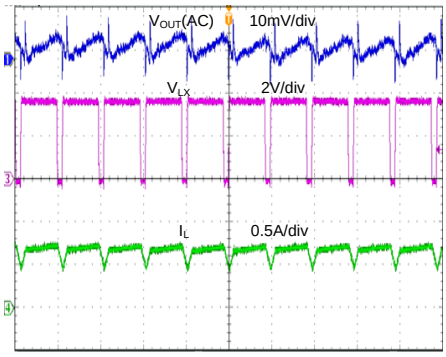
(V_{IN}=3.0V, V_{OUT}=3.3V, 1.2A to Short)



Time (2ms/div)

Output Ripple

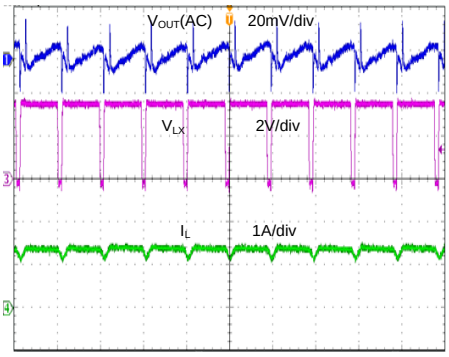
(V_{IN}=3.6V, V_{OUT}=3.3V, I_{LOAD}=0.6A)



Time (1μs/div)

Output Ripple

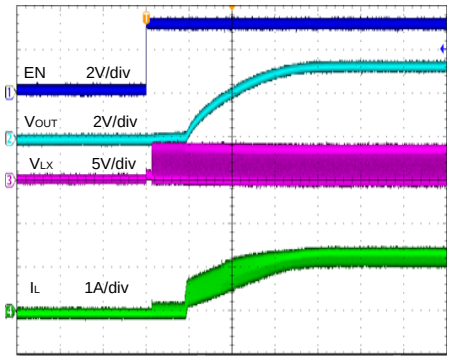
(V_{IN}=3.6V, V_{OUT}=3.3V, I_{LOAD}=1.2A)



Time (1μs/div)

Startup From Enable

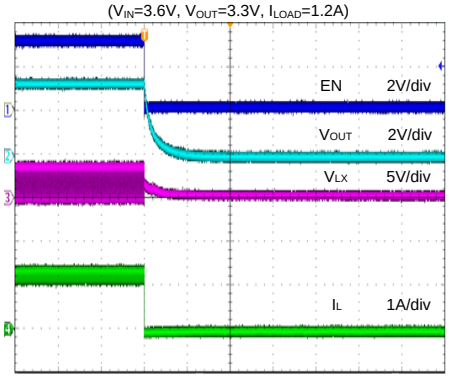
(V_{IN}=3.6V, V_{OUT}=3.3V, I_{LOAD}=1.2A)



Time (400μs/div)

Shutdown From Enable

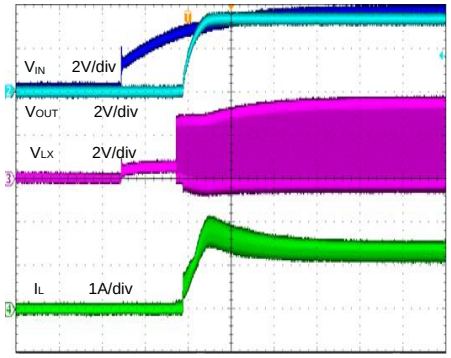
(V_{IN}=3.6V, V_{OUT}=3.3V, I_{LOAD}=1.2A)



Time (400μs/div)

Startup From V_{IN}

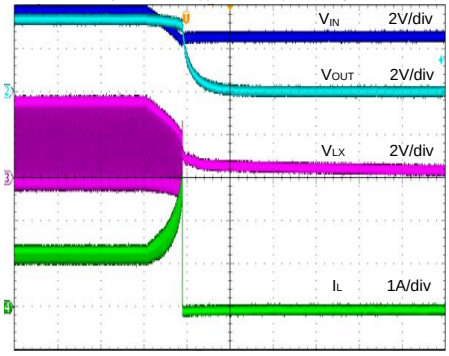
(V_{IN}=3.6V, V_{OUT}=3.3V, I_{LOAD}=1.2A)



Time (2ms/div)

Shutdown From V_{IN}

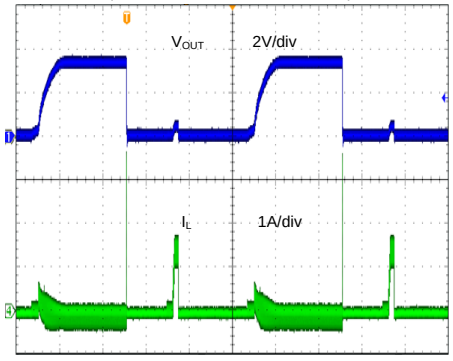
(V_{IN}=3.6V, V_{OUT}=3.3V, I_{LOAD}=1.2A)



Time (400μs/div)

Short Circuit Protection

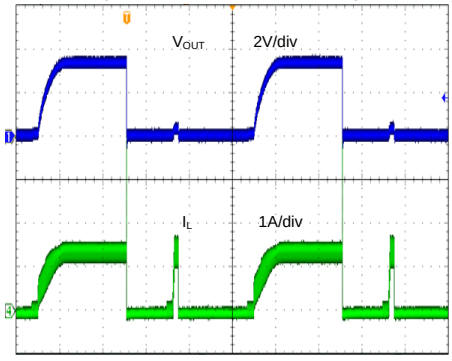
(V_{IN}=3.6V, V_{OUT}=3.3V, 0A to Short)



Time (2ms/div)

Short Circuit Protection

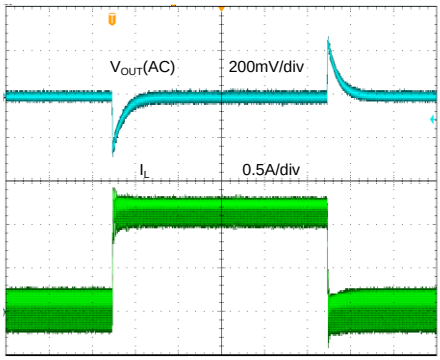
(V_{IN}=3.6V, V_{OUT}=3.3V, 1.2A to Short)



Time (2ms/div)

Load Transient

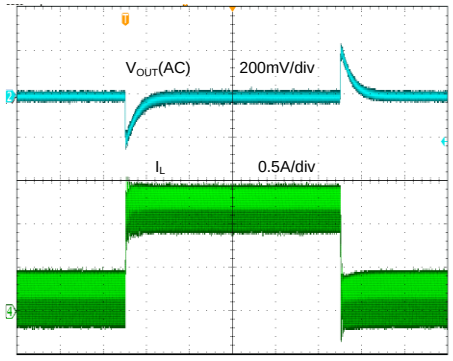
(V_{IN}=3.6V, V_{OUT}=3.3V, I_{LOAD}=0.2~1.2A)



Time (200μs/div)

Load Transient

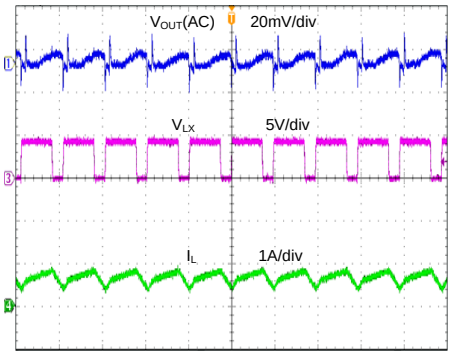
(V_{IN}=4.2V, V_{OUT}=3.3V, I_{LOAD}=0.2~1.2A)



Time (200μs/div)

Output Ripple

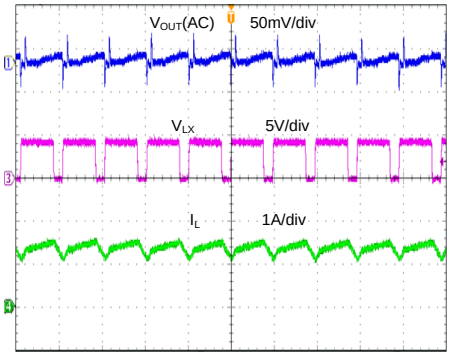
(V_{IN}=4.2V, V_{OUT}=3.3V, I_{LOAD}=0.6A)



Time (1μs/div)

Output Ripple

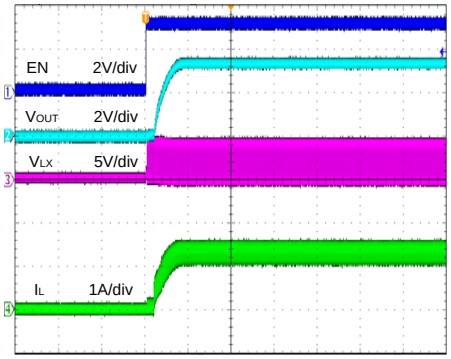
(V_{IN}=4.2V, V_{OUT}=3.3V, I_{LOAD}=1.2A)



Time (1μs/div)

Startup From Enable

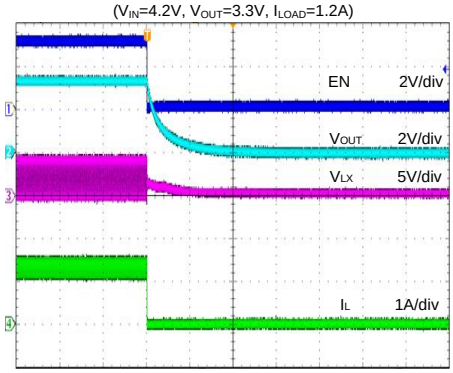
(V_{IN}=4.2V, V_{OUT}=3.3V, I_{LOAD}=1.2A)



Time (2ms/div)

Shutdown From Enable

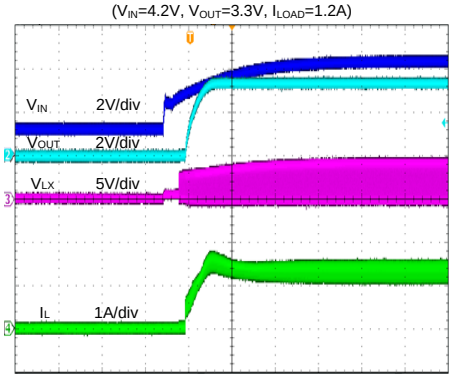
(V_{IN}=4.2V, V_{OUT}=3.3V, I_{LOAD}=1.2A)



Time (200μs/div)

Startup From V_{IN}

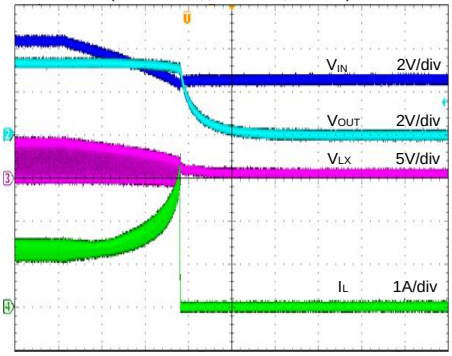
(V_{IN}=4.2V, V_{OUT}=3.3V, I_{LOAD}=1.2A)



Time (2ms/div)

Shutdown From V_{IN}

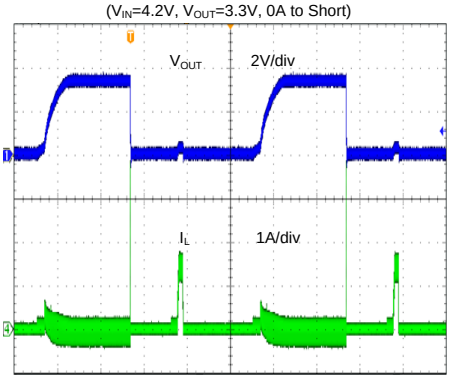
(V_{IN}=4.2V, V_{OUT}=3.3V, I_{LOAD}=1.2A)



Time (200μs/div)

Short Circuit Protection

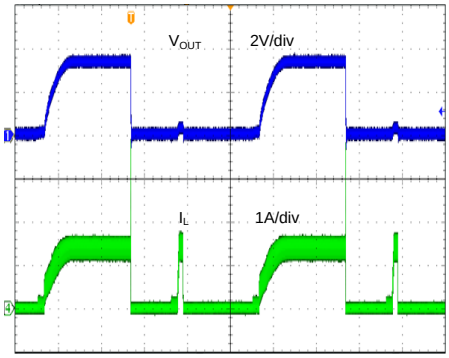
(V_{IN}=4.2V, V_{OUT}=3.3V, 0A to Short)



Time (2ms/div)

Short Circuit Protection

(V_{IN}=4.2V, V_{OUT}=3.3V, 1.2A to Short)



Time (2ms/div)

Operation

The device uses a 1MHz fixed frequency, pulse-width-modulation (PWM) architecture to obtain high efficiency, while enabling a small solution size. Under light load, the part switches automatically to PFM mode to maintain high efficiency.

The output voltage can be configured between 2.6V and 3.8V using a resistor divider. A soft-start circuit limits the power-up inrush current, and can be configured using an external capacitor. A simple RC series compensation network ensures stable operation across the range of loads and input voltages.

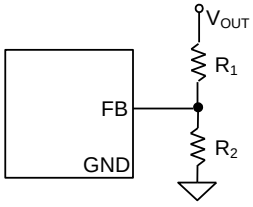
Selecting the passive components to meet the application requirements is described below.

Application Information

Feedback Resistor Divider R1 and R2

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_1 and R_2. A value between 10k and 1M is recommended for both resistors. If R_1=100k is chosen, then R_2 can be calculated to be:

$$R_2 = \frac{0.6R_1}{V_{OUT} - 0.6} (\Omega)$$



Input Capacitor C_{IN}

With the maximum load current of 1.2A, a typical X5R or better grade ceramic capacitor with 6.3V rating and greater than 22µF capacitance is recommended. Using low ESR ceramic capacitors able to handle the input current ripple is recommended. Using two low ESR capacitors in parallel is recommeneded for applications where lower input voltage ripple is beneficial. Place the ceramic capacitor(s) close to the V_{IN} and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and VIN/GND pins.

Output Capacitor C_{OUT}

Both steady state ripple and transient requirements must be taken into account when selecting this capacitor. Using two X5R or better grade ceramic capacitors in parallel, with a 6.3V voltage rating and a capacitance higher than 22µF is recommended for most applications.

Output Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be around 40% of the maximum average input current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN\_MAX})}{F_{SW} \times I_{OUT\_MAX} \times 40\%} (H)$$

where F_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

SY20516A is less sensitive to ripple current variations. Consequently, the final choice of inductance can be slightly different than the calculated value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.
The maximum peak current happens under minimum input voltage condition.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN\_MIN}}\right) \times I_{OUT,\,MAX} + \frac{V_{IN\_MIN}}{V_{OUT}} \frac{(V_{OUT} - V_{IN\_MIN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to meet the desired efficiency requirements. It is desirable to choose an inductor with DCR<15mΩ to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown, the SY20516A the current drops to lower than 0.1μA. Driving the EN pin high (>1.5V) will turn on the IC again.

Soft-start Programming

The SY20516A provides an external soft-start pin that gradually raises the output voltage. The soft-start time can be programmed by using an external capacitor between the SS pin and GND. The soft-start time can be calculated using the following formula:

$$t_{ss} = \frac{0.7}{I_{ss}} \times C_{ss}$$

As an example, using a 20nF capacitor will determine a typical soft-start time of 2.8ms. Don't leave SS pin floating.

Power Good Indicator

The PG pin is an open-drain output. The pins is actively driven low when the voltage measured at the FB pin is below 0.48V or above 0.72V. This translates to the output voltage being 20% below or above the target voltage set by the resistor divider.

The PG pin is also driven low during the start-up sequence, as soon as the voltage at the P_{VIN} pin reaches the V_{UVLO} level, and until the output voltage raises to 80% of the configured value.

For proper operation, the pin requires a pull-up resistor to a voltage rail within the operating voltage range.

During normal operation, when the output is within +/-20% of the target, the output is Hi-Z and the pull-up resistor ensures a high level for interfacing to the rest of the system.

Thermal protection

SY20516A includes over temperature protection circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the thermal protection threshold.

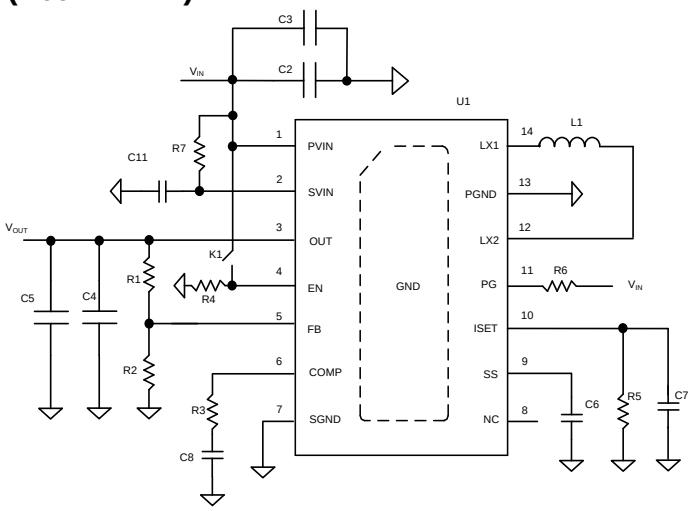
Short circuit protection

The SY20516A includes short circuit protection. If VOUT < ~50% of the set point and the device is in current limit, the short circuit protection mode will be initiated and the device will enter hic-cup protection mode. During hic-cup protection mode, the device will try to restart, and the cycle of hic-cup is approximately 4ms. If the output fault conditions are removed, the device will go back to normal operation on the nearest hic-cup on time with a complete soft start cycle.

Over Voltage Protection

The SY20516A includes output over voltage protection. If the feedback voltage rises above 125% of the feedback reference voltage the protection will be triggered after a 16μs delay. The device resumes operation once the overvoltage condition is removed.

Application Schematic (V_{OUT} = 3.3V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
U_1	Buck-Boost Converter	SY20516ADPC	Silergy
L_1	2.2μH/5.1A inductor	VLP6045LT-2R2N	TDK
C_1	100μF/16V (electrolytic capacitor)		
C_2, C_3	22μF/6.3V, 0805, X5R	C2012X5R0J226M	TDK
C_4, C_5	22μF/6.3V, 0805, X5R	C2012X5R0J226M	TDK
C_{11}	1μF, 0603		
R_1	100k,1%,0603		
R_2	22.1k,1%,0603		
R_3	20k, 0603		
C_8	2.2nF, 0603		
R_6	100k, 0603		
C_6	20nF, 0603		
R_5	150k, 0603		
C_7	10nF, 0603		
R_4	1MΩ, 0603		
R_7	0Ω		

Layout Design:

To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN}, C_{OUT}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.

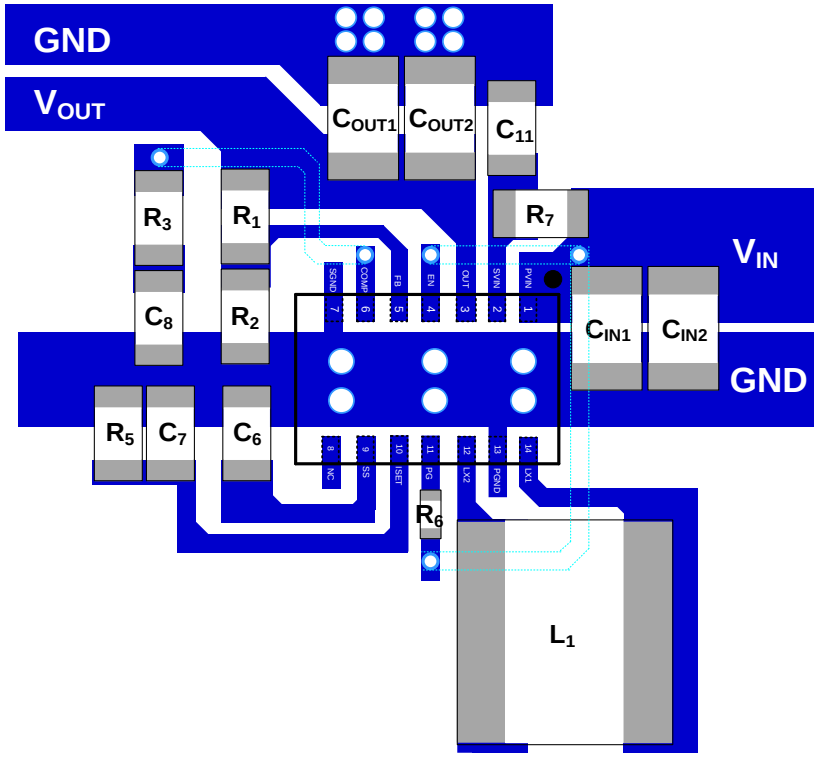
2) SVIN is the power supply pin for the internal control circuit. Don't connect SVIN pin to PVIN pin directly. A separated 1uF ceramic cap is strongly recommended to decouple SVIN pin to GND.

3) The decoupling capacitor of VIN must be placed close enough to the VIN pin and GND pins. The loop area formed by the input capacitors, VIN pin and GND pins must be minimized.

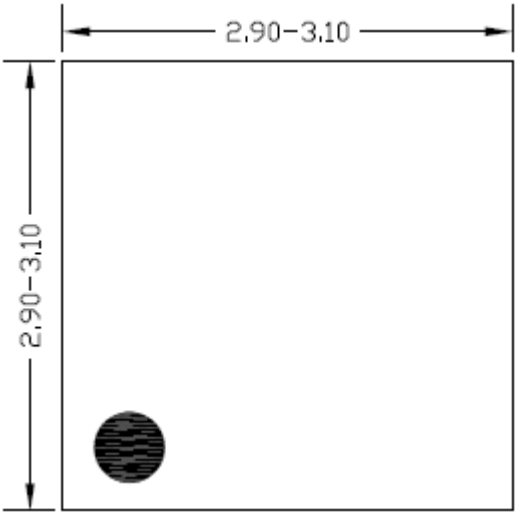
4) The PCB copper area associated with LX pin must be minimized to improve the noise immunity.

5) The components R_1, R_2 and the trace connecting to the FB/OUT pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to FB/OUT pin.

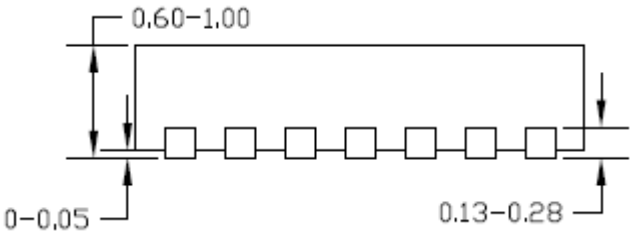
PCB layout Suggestion



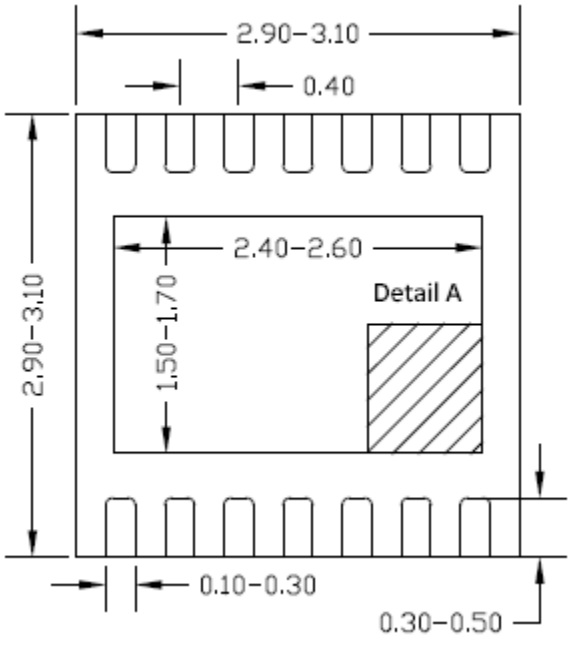
DFN3×3-14 Package Outline Drawing

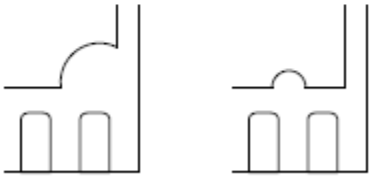


Top View



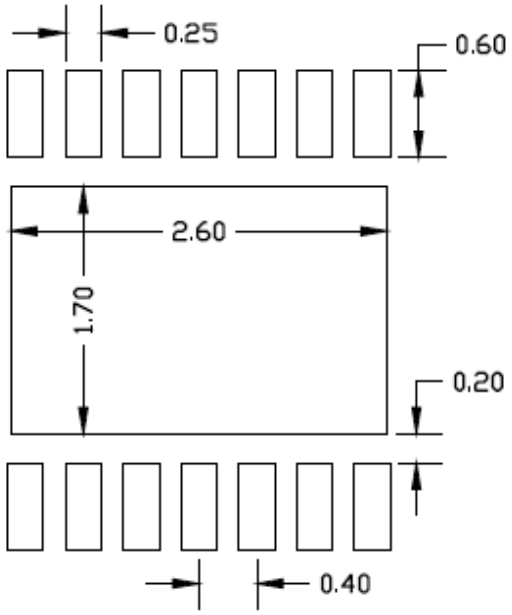
Side View





Detail A
Pin1 Identifier: two options

Bottom View

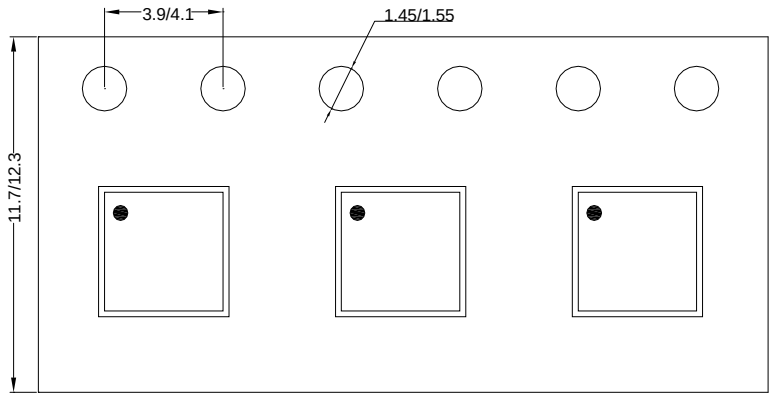


Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr**

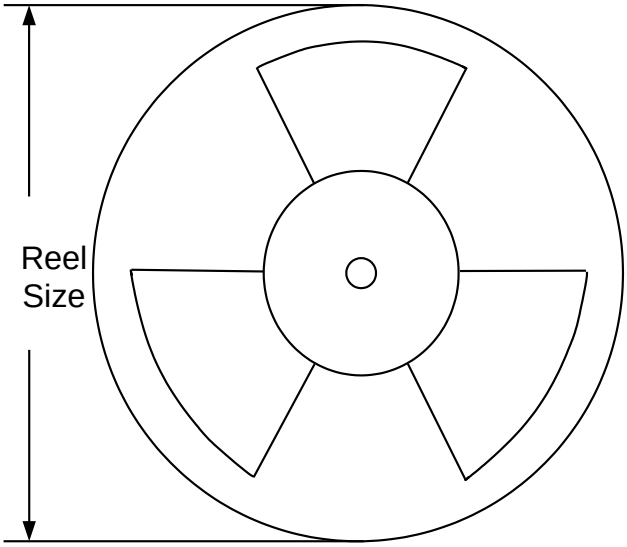
Taping & Reel Specification

1. DFN3×3-14 taping orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3×3	14	8	13"	400	400	5000

3. Others: NA

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