SY20733B

500mA Low Dropout Bias Rail LDO Regulator

General Description

The SY20733B is a low-voltage, low-dropout voltage regulator capable of sourcing 500mA with a built-in negative metal-oxide-semiconductor (NMOS). A separate bias rail is provided to enable an input voltage range of 0.8V to 5.5V. The output voltage can be configured using a resistor divider and provides a voltage accuracy of ±1%.

The SY20733B is available in a compact DFN1.2mm×1.2mm-6 pin package.

Features

- Input Voltage Range: 0.8V-5.5V
- Bias Voltage Range: 2.4V-5.5V
- Output Voltage Accuracy: ±1%
- Bias Input Quiescent Current: 110μA (typ.)
- Bias Shutdown current: 0.1μA (typ.)
- Up to 500mA Output Current
- Current Limit Protection
- Over Temperature Shutdown
- Output Auto-Discharge Resistor: 130Ω
- RoHS Compliant and Halogen Free
- Compact Package: DFN1.2×1.2-6

Applications

- Battery−Powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

Typical Applications

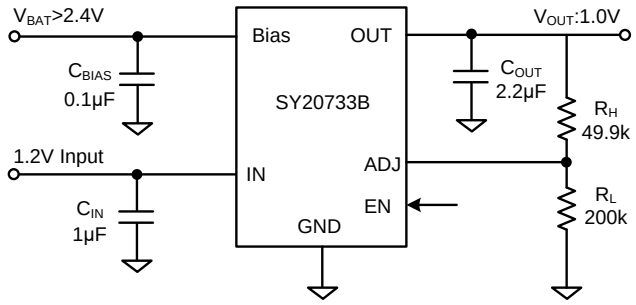


Figure 1. Schematic Diagram

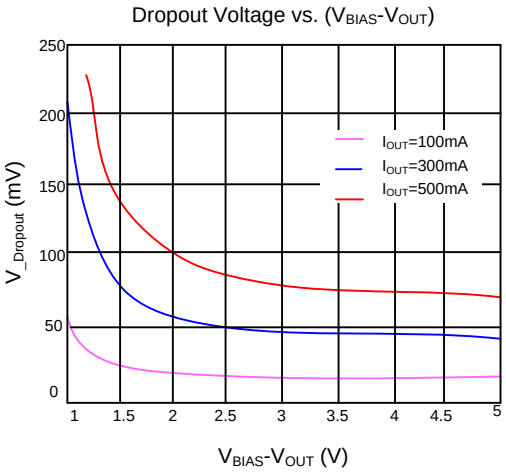


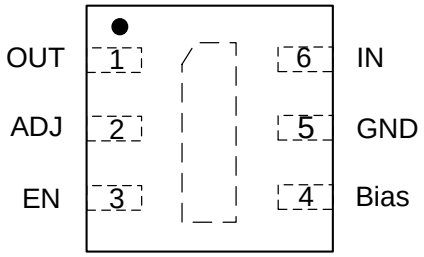
Figure 2. Dropout Curve

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY20733BSCC	DFN1.2x1.2-6 RoHS Compliant and Halogen Free	**Hxyz**

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Number	Symbol	Pin Description
1	OUT	Output pin. Decouple this pin to the GND with at least a 2.2μF ceramic capacitor.
2	ADJ	Output voltage programming pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: V_{OUT}=0.8V× (1+R_H/R_L).
3	EN	Enable control pin. Pull high to enable the regulator. Pull low to shut down the regulator. Do not leave it floating.
4	Bias	Bias voltage supply for internal control circuits. Decouple this pin to GND with at least a 0.1μF ceramic capacitor.
5	GND	Ground pin.
6	IN	Input voltage supply pin. Decouple this pin to GND with at least a 1μF ceramic capacitor.

Block Diagram

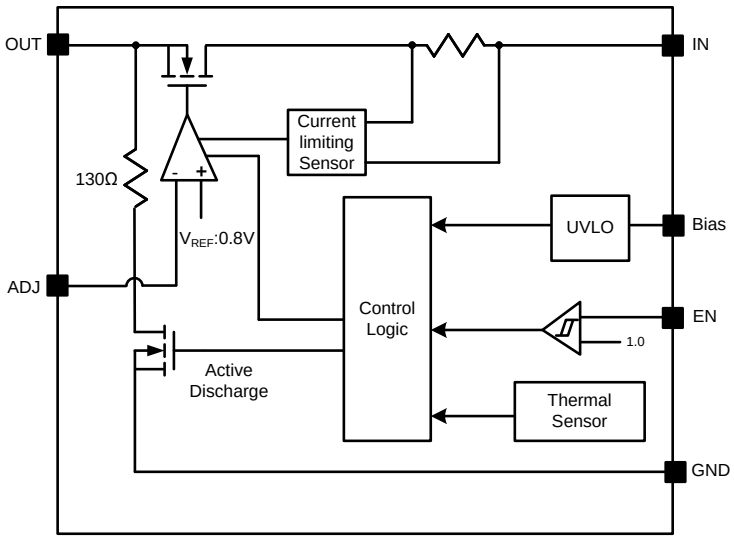


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
IN, OUT, Bias, EN, ADJ	-0.3	6	V
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	70	°C/W
θ_{JC} Junction-to-case Thermal Resistance	12	
P_D Power Dissipation T_A = 25°C	1.4	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Bias Input Voltage	2.4	5.5	V
IN	0.8	5.5	
OUT	0.8	V_{Bias}-1.4	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} =1.2V, V_{OUT}=1.0V, V_{Bias}=3.3V, I_{OUT}=1mA, C_{IN}=1.0uF, C_{OUT}=2.2μF, T_A = 25°C unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Input Voltage Range	V_{IN}		$V_{OUT}+V_{DO}$		5.5	V
Bias Input Voltage	V_{Bias}		2.4		5.5	V
Bias Supply Current	I_{Bias}			110		μA
Bias Shutdown Current	I_{SD}	V_{EN}=0		0.1	1	μA
Feedback Reference Voltage	V_{REF}		0.792	0.8	0.808	V
Current Limit	I_{LIM}		500			mA
Load Regulation	V_{LOAD}	I_{OUT}: 1mA~500mA		2		mV
V_{Bias} Line Regulation	$\triangle V_{OUT}/\triangle V_{Bias}$	2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{Bias} < 5.5 V		0.01		%/V
Dropout Voltage	V_{DO}	I_{OUT}=500mA		90		mV
Ripple Rejection	$PSRR_{(VIN)}$	V_{IN} to V_{OUT}, f = 1 kHz, I_{OUT} = 150mA, $V_{IN} \geq V_{OUT}$ +0.5 V		70		dB
	$PSRR_{(VBias)}$	V_{Bias} to V_{OUT}, f = 1 kHz, I_{OUT} = 150mA, $V_{IN} \geq V_{OUT}$ +0.5 V		70		dB
Output Voltage Temperature Coefficient	$\triangle V_{OUT}/\triangle T$	I_{OUT}=100mA -40°C≤T≤85°C		±100		ppm/°C
Output Noise Voltage	V_N	$V_{IN}=V_{OUT}$+0.5V, V_{OUT}=1V, f=10Hz to 100kHz		40		μV_{RMS}
Discharge Resistor	$R_{Discharge}$			130		Ω
EN Rising Threshold	V_{ENH}		1.0			V
EN Falling Threshold	V_{ENL}				0.4	V
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

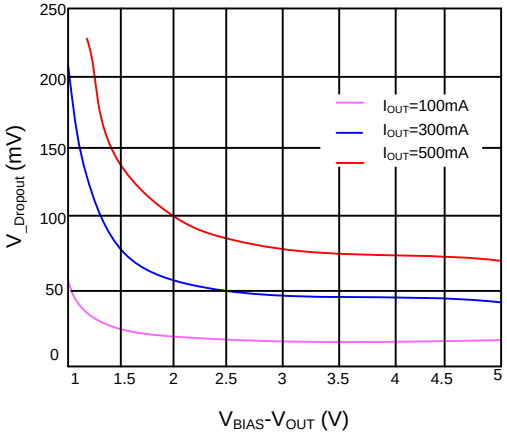
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} of SY20733BSCC is measured in the natural convection at T_A = 25°C on a two-layer Silergy evaluation board. θ_{JC} measurement. Paddle of DFN 1.2x1.2-6 package is the case position for SY20733BSCC.

Note 3: The device is not guaranteed to function outside its operating conditions.

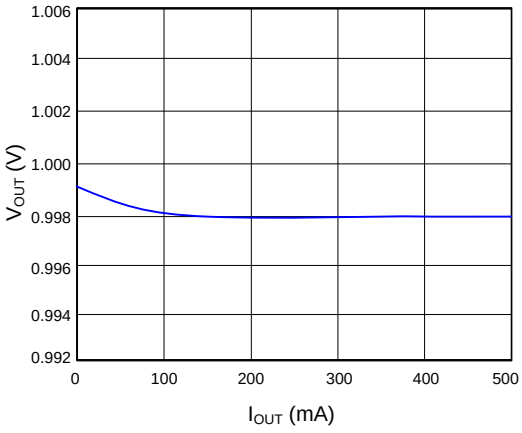
Typical Performance Characteristics

Dropout Voltage vs. (V_{BIAS}-V_{OUT})



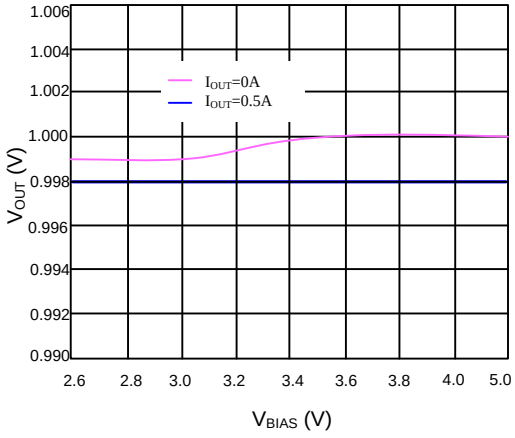
Load Regulation

(V_{IN}=1.2V, V_{BIAS}=3.3V)



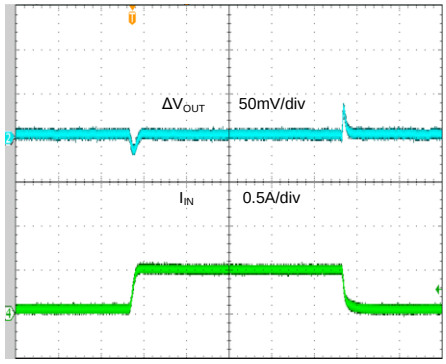
V_{BIAS} Line Regulation

(V_{IN}=1.2V, V_{BIAS}=3.3V)



Load Transient

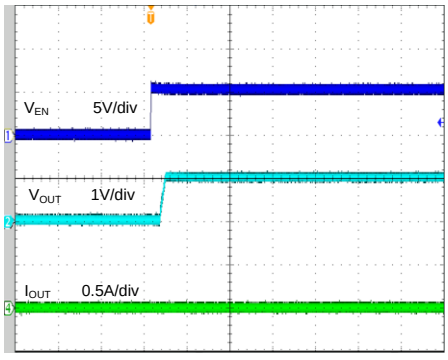
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V, I_{OUT}= 50mA~ 500mA)



Time (100μs/div)

Startup from Enable

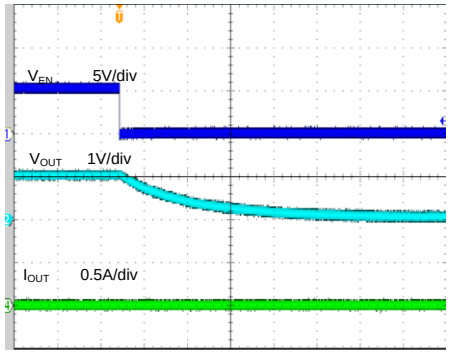
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=0A)



Time (200μs/div)

Shutdown from Enable

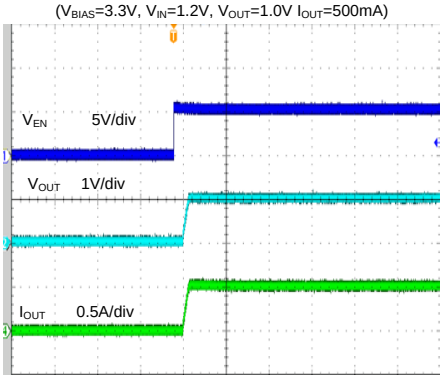
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=0A)



Time (200μs/div)

Startup from Enable

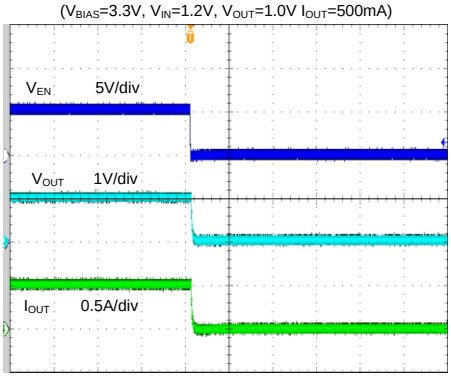
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=500mA)



Time (200μs/div)

Shutdown from Enable

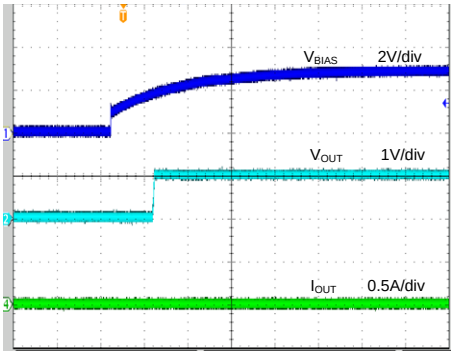
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=500mA)



Time (200μs/div)

Startup from V_{BIAS}

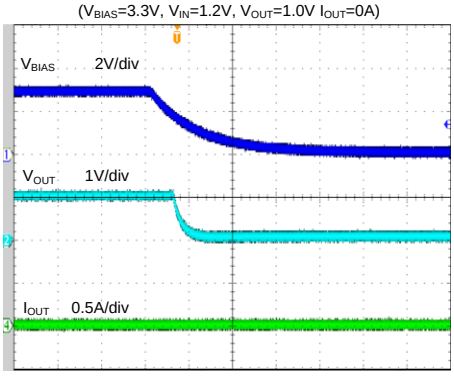
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=0A)



Time (2ms/div)

Shutdown from V_{BIAS}

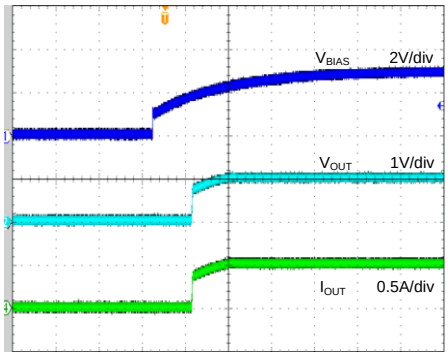
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=0A)



Time (2ms/div)

Startup from V_{BIAS}

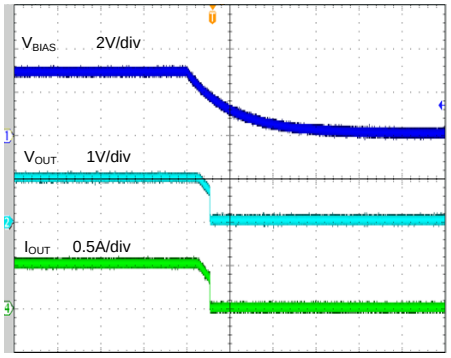
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=500mA)



Time (2ms/div)

Shutdown from V_{BIAS}

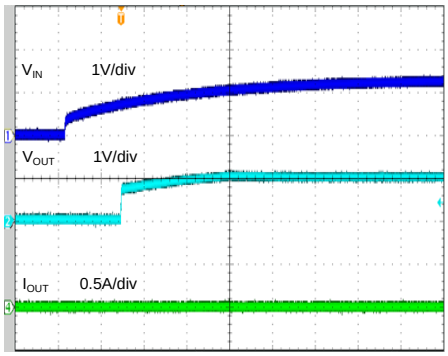
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=500mA)



Time (2ms/div)

Startup from V_{IN}

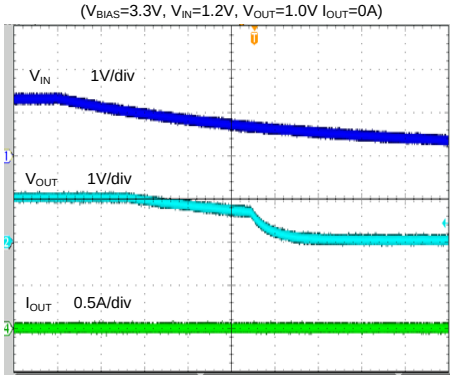
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=0A)



Time (800us/div)

Shutdown from V_{IN}

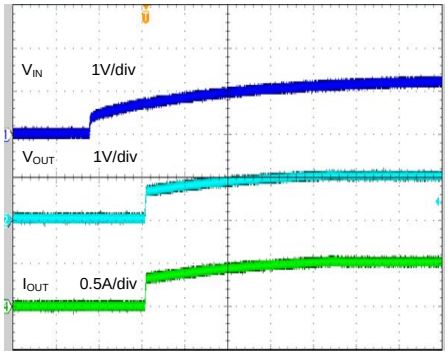
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=0A)



Time (800us/div)

Startup from V_{IN}

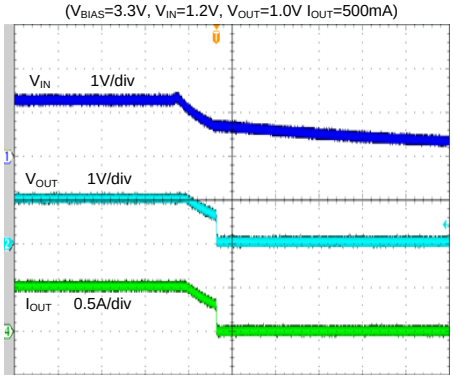
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=500mA)



Time (800us/div)

Shutdown from V_{IN}

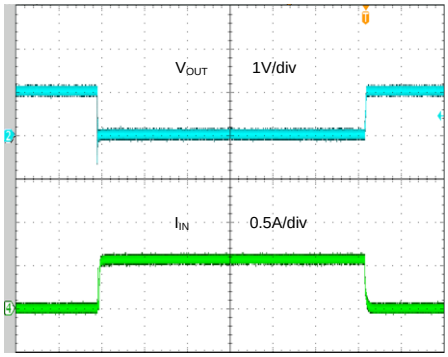
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=500mA)



Time (800us/div)

Hard Short Protection

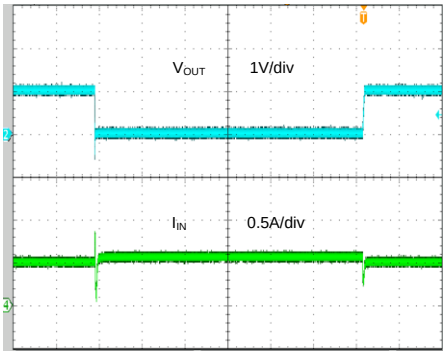
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=0A to short)



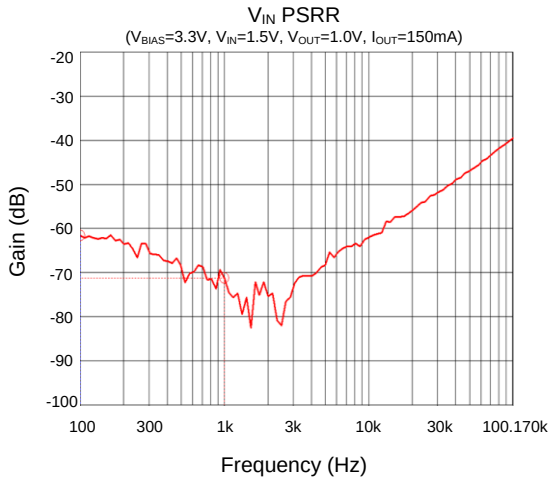
Time (800us/div)

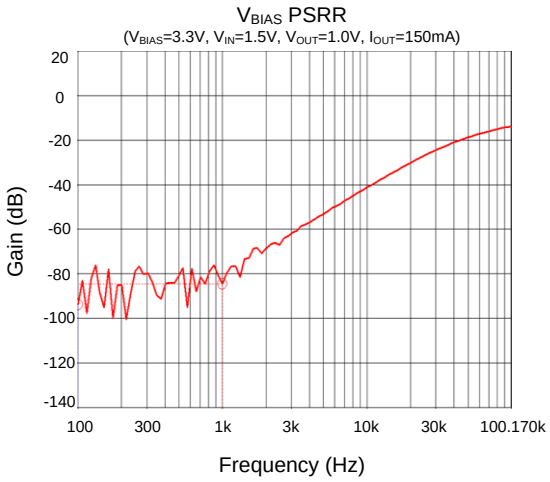
Hard Short Protection

(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=0.5A to short)



Time (800us/div)





Application Information

The SY20733B is a low dropout LDO regulator with a compact DFN1.2×1.2-6 package, capable of delivering up to 500mA output current.

Input Capacitor C_{IN}:

A 1μF decoupling capacitor is recommended between the input and ground pins. A typical X5R or better grade ceramic capacitor with a 6V rating is recommended for most applications.

Output Capacitor C_{OUT}:

The SY20733B is designed to operate using low equivalent series resistance (ESR) ceramic capacitors. This forms a zero to provide phase lead which is required for loop stability. A 2.2μF input capacitor with 10mΩ to 50mΩ ESR range can be used in this application. Higher capacitance values help to improve transient response.

Place the input and output capacitors as close as practical to the input and output pins to ensure stable operation.

Bias Capacitor C_{Bias}:

A 0.1μF decoupling capacitor is recommended between the bias and GND pins. Place the capacitor as close as practical to the device to achieve the best decoupling performance.

No Load Stability:

The device will remain stable and in regulation with no external load. This is especially important in CMOS RAM keep-alive applications.

Dropout Voltage:

Keep V_{Bias} higher than V_{OUT} +1.4V. Decrease V_{IN} until V_{OUT} starts to decrease. The value for V_{IN}-V_{OUT} is defined as V_{IN} dropout voltage. The V_{IN} dropout voltage is the regulator's minimum V_{IN}-V_{OUT}:

$$V_{DROPOUT} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT}$$

Current Limit:

The internal current-limit circuit protects the LDO against transient high-load current faults. During an overload event, the minimum current limit is 500mA.

Short-Circuit Protection:

The current through the device increases very rapidly during a short circuit event. When a short circuit is detected by comparing the current through the device with the current limit threshold, the current is reduced to approximately 0.5A. Operating in current limit can trigger the integrated thermal shutdown protection circuit. The output turns on and off when thermal shutdown is reached until the temperature drops below $T_{SD} - T_{HYS}$.

Thermal Considerations:

The SY20733B can source a current of up to 500mA over the full operating junction temperature range. However, the maximum output current must be derated at a higher ambient temperature to limit junction temperature to a maximum of 125℃. The junction temperature must be within the operating range specified under all operating conditions. The LDO power dissipation depends on the input-to-output voltage difference and load current.

The dissipated power, P_D, can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT})I_{OUT}$$

The operating junction temperature can be estimated by using the following formula:

$$P_{DMAX} = (T_{J(MAX)} - T_A)/\theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum junction temperature of die (125℃) and T_A is the maximum ambient temperature.

PCB Layout Guide

Good board layout practices must be used for stable operation, and a large PCB copper area can improve the thermal performance. The input and output capacitors must be directly connected to the device's input, output and ground pins using traces with no other currents flowing through them. Place C_{IN} and C_{OUT} near the device with short traces to the IN, OUT, and ground pins.

Below is the recommended PCB layout example:

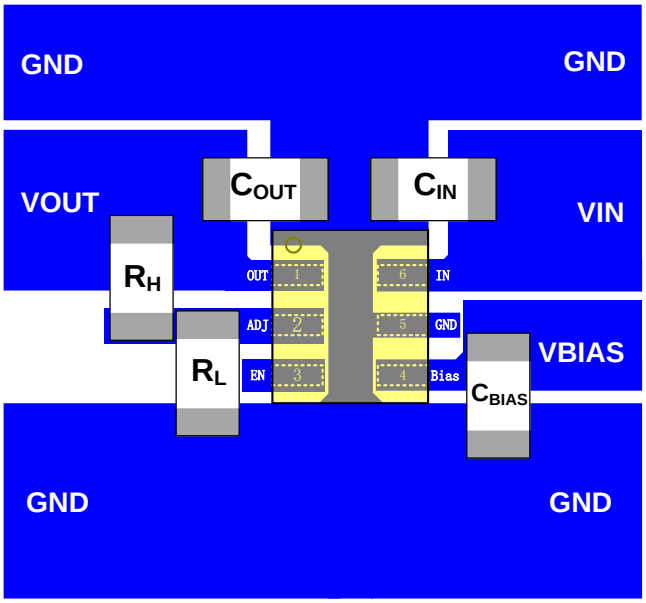
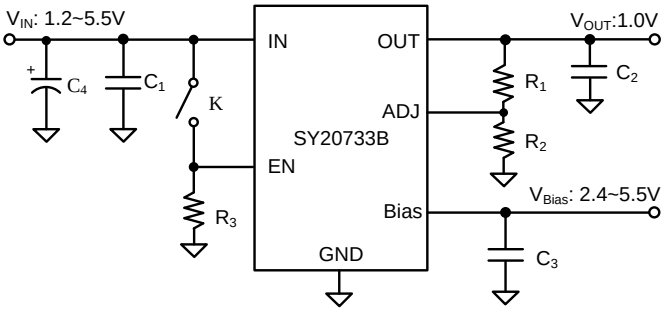


Figure 4. PCB Layout Example

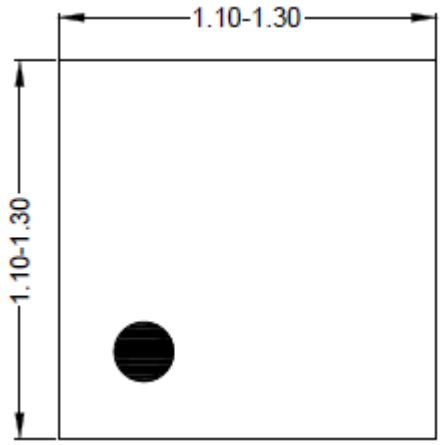
Application Schematic (V_{OUT} = 1.0V)



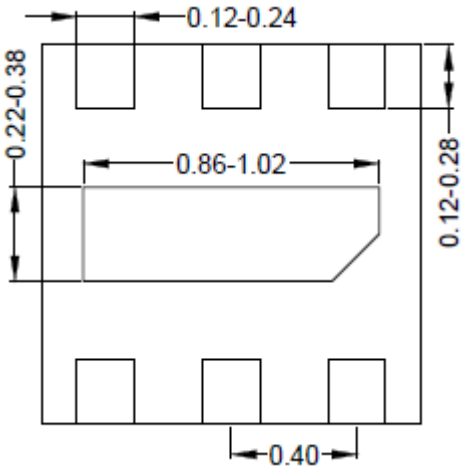
BOM List

Reference Designator	Description	Part Number	Manufacturer
C_1	1.0μF/25V, 0603, X5R	C1608X5R1E105K	TDK
C_2	2.2μF/16V, 0603, X5R	C1608X5R1C225K	TDK
C_3	0.1μF/50V, 0603, X5R	C1608X5R1H104K	TDK
C_4	100μF/16V (electrolytic capacitor)		
R_1	49.9kΩ, 1%, 0603		
R_2	200kΩ, 1%, 0603		
R_3	1MΩ, 0603		

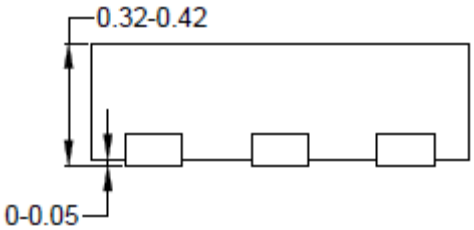
DFN1.2×1.2-6 Package Outline Drawing



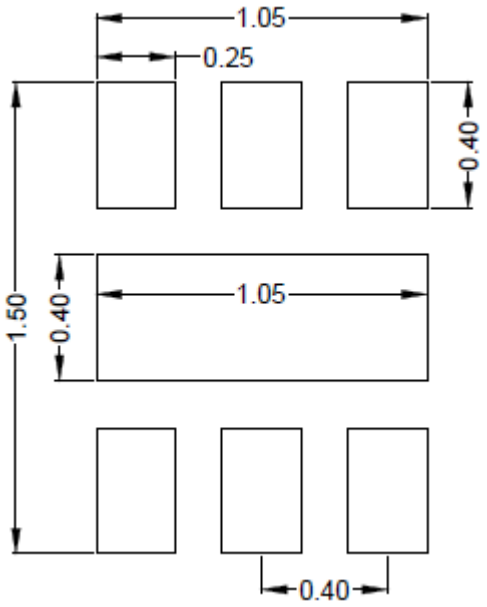
Top View



Bottom View



Side View

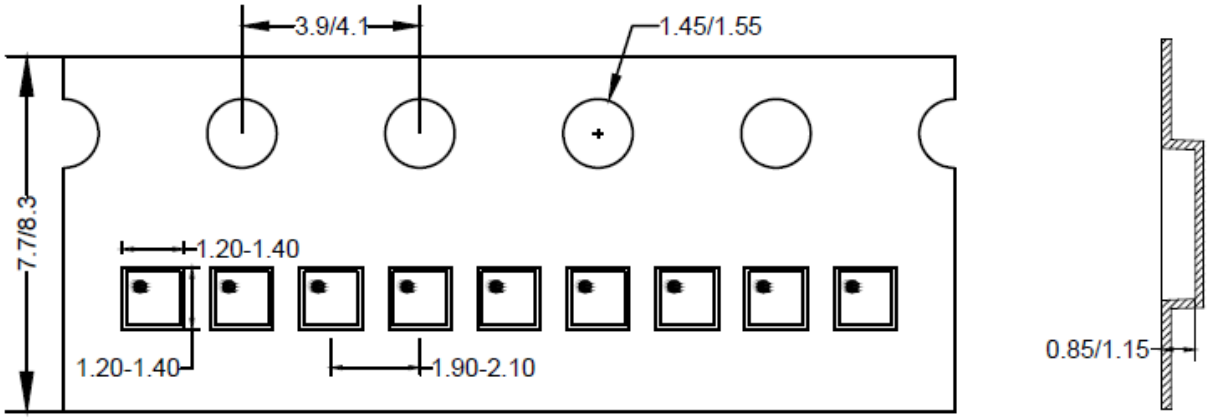


Recommended PCB Layout (Reference Only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

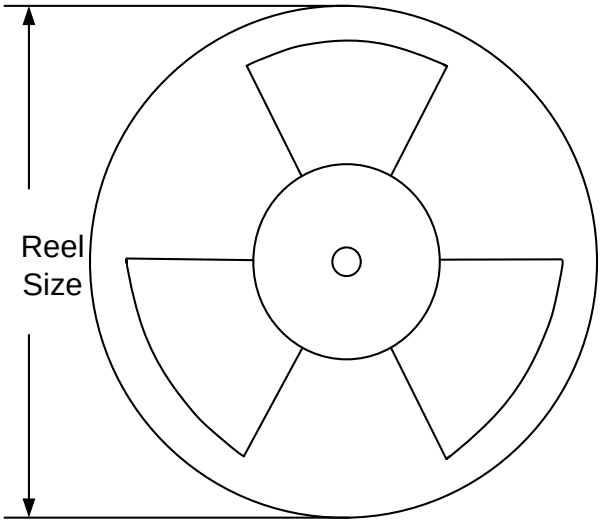
Taping & Reel Specification

1. DFN1.2×1.2 Taping Orientation



Feeding direction ⟶

2. Carrier Tape & Reel Specification for Packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN1.2×1.2	8	2	7"	400	160	5000

3. Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warranted. Please reference the latest revision.

Date	Revision	Change
Sep. 25, 2023	Revision 1.0	Language improvements for clarity.
Mar. 21, 2019	Revision 0.9B	Qty per reel change from 10000 to 5000
Mar. 20, 2018	Revision 0.9A	1. Update in "Absolute Maximum Ratings" a. Change from "All pins ---------- 6.0V" to "IN, OUT, Bias, EN, ADJ ---------- -0.3V to 6.0V". b. Change from "Junction Temperature Range ---------- 150°C" to "Junction Temperature Range --------- -40°C to 150°C". 2. Update in "Recommended Operating Conditions" Add "IN ---------- 0.8V to 5.5V OUT ---------- 0.8V to VBias-1.4V". 3. Update in "Dropout Voltage" in Page9 Change from "When V_{Bias} is high enough" to "Keep V_{Bias} is higher than V_{OUT} +1.4V".
Apr. 25, 2017	Revision 0.9	Initial Release

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