SY20739DAC

Low Input/Low dropout, 2A LDO with Enable

General Description

The SY20739DAC is a high-performance positive voltage regulator designed for applications which require very low input voltage and very low dropout voltage at up to 2A output. It operates with a V_{IN} as low as 1.5V, with output voltage programmable as low as 0.5V. The SY20739DAC features ultra-low dropout, ideal for applications where V_{OUT} is very close to V_{IN}. Additionally, it has an enable pin to further reduce power dissipation while shut down. The device provides excellent regulation over variations in line, load and temperature.

The SY20739DAC has an adjustable output which can be set by two external resistors. The SY20739DAC is available in the DFN3×3-8 package.

Ordering Information

Ordering Number	Package Type	Note
SY20739DAC	DFN3×3-8	--

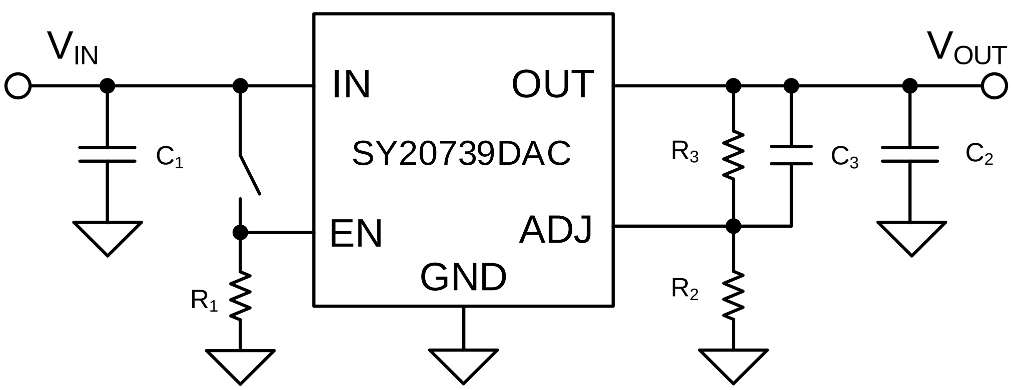
Features

- Input Voltage as Low as 1.5V
- 400mV Dropout @ 2A
- Adjustable Output from 0.5V
- 0.9ms Internal Soft-start Minimizes Inrush Current
- 10μA Quiescent Current in Shutdown
- Over Current and Over Temperature Protection
- Enable Control: Default High
- Reverse Blocking from Output to Input
- Full Industrial Temperature Range
- RoHS Compliant and Halogen Free
- Package: DFN3×3-8

Applications

- Telecom/Networking Cards
- Motherboards/Peripheral Cards
- Industrial Applications
- Wireless Infrastructure
- Set Top Box
- Medical Equipment
- Notebook Computers
- Battery Powered Systems

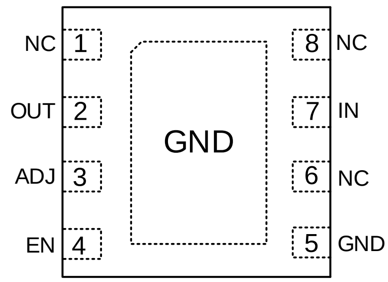
Typical Applications



$$V_{OUT}=0.5\times\left(\frac{R_3+R_2}{R_2}\right)$$

Figure1. Schematic Diagram

Pinout (top view)



(DFN3×3-8)

Top Mark: ERFxyz (Device code: ERF; ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
NC	1, 6, 8	NO internal connection.
OUT	2	Output pin. A minimum of 22μF capacitor should be placed directly at this pin.
ADJ	3	Feedback voltage input. If external feedback resistors are used, the output voltage will be determined by the resistor ratio.
EN	4	Enable control input (Active-High). Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. The device will be enabled if this pin is left open.
GND	5, Exposed Pad	Ground pin. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
IN	7	Input supply pin. For regulation at full load, the input to this pin must be between (V_{OUT} + 0.4V) and 6V. Minimum input voltage is 1.5V. A large bulk capacitance should be placed closely to this pin to ensure that the input supply does not sag below 1.5V. Also, a minimum of 10μ F ceramic capacitor should be placed directly at this pin.

Block Diagram

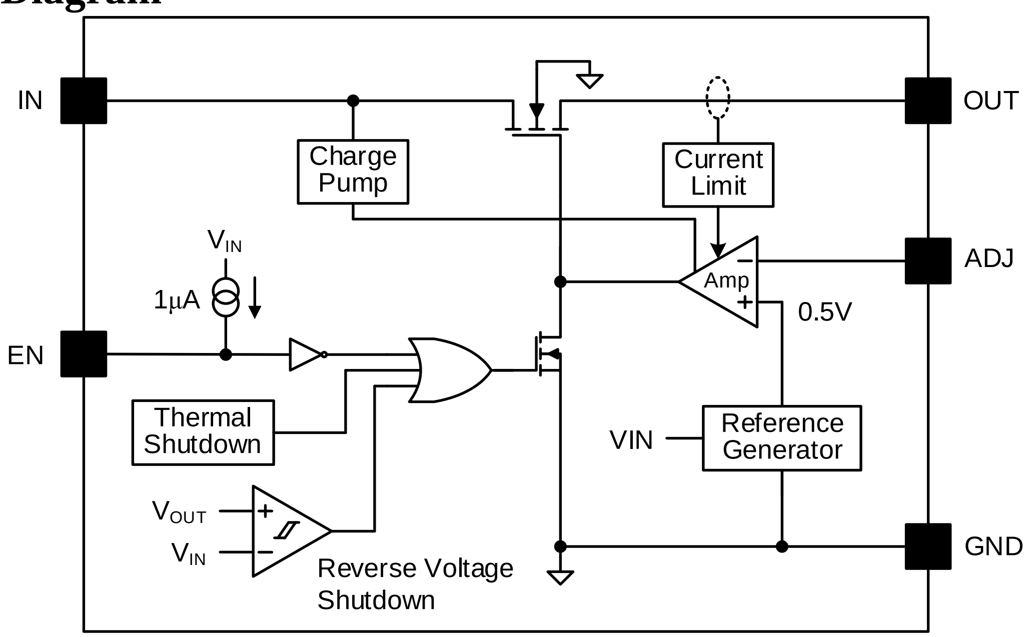


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

IN, EN, OUT, ADJ -- -0.3V to 7V
Power Dissipation, P_D @ T_A = 25°C-- 2.439W
Package Thermal Resistance (Note 2)
θ_{JA} -- 41°C/W
θ_{JC} -- 5°C/W
Junction Temperature Range -- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range --- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN -- 1.5V to 6V
Maximum Output Current -- 2A
Junction Temperature Range -- -40°C to 125°C

Electrical Characteristics

(V_{IN} =V_{EN} =1.5 to 6V; V_{OUT}=V_{ADJ} =0.5V; I_{OUT} =10µA to 2A, C_{IN} = 10µF; C_{OUT} = 22µF; T_J= –40°C to +125°C. Typical values are at T_J = 25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Test Conditions		T_J	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}			-40°C ~125°C	1.5		6	V
Reference Accuracy	V_{REF}	V_{IN} = 3.3V, I_{OUT} =10mA		25°C	0.495	0.5	0.505	V
				-40°C ~125°C	0.49	0.5	0.51	
		1.5V<V_{IN}<6V, 10mA<I_{OUT}<2A		-40°C ~125°C	0.485	0.5	0.515	
Line Regulation		I_{OUT} = 10mA		25°C		0.2		%/V
Load Regulation		10mA≤I_{OUT}≤2A		25°C		0.3		%/A
Shutdown Current	I_{SD}	V_{IN} = 6.0V, V_{EN} =0V		-40°C ~125°C		10	50	µA
Ground pin current	I_{GND}	V_{IN} = 3.3V, I_{OUT} = 0A		-40°C ~125°C			3	mA
Dropout Voltage	V_{DO}	I_O =1A	1.5V ≤ V_{IN} < 1.6V	-40°C ~125°C		90	400	mV
			1.6V≤V_{IN} ≤ 6V	-40°C ~125°C			200	
		I_O =1.5A	1.5V ≤ V_{IN} < 1.6V	-40°C ~125°C		200	500	
			1.6V ≤ V_{IN} ≤ 6V	-40°C ~125°C			300	
		I_O =2A	1.5V ≤ V_{IN} < 1.6V	-40°C ~125°C		300	600	
			1.6V ≤ V_{IN} ≤ 6V	-40°C ~125°C			400	
Minimum Load Current	$I_{O,MIN}$			-40°C ~125°C			10	µA
Output Current Limit	I_{LIMIT}	V_{IN}=3.3V		-40°C ~125°C	2.1	3	4.4	A
Feedback Pin Current	I_{FB}	V_{IN}=V_{REF}		-40°C ~125°C		80	200	nA
EN High Level	$V_{EN(HI)}$	V_{IN}=3.3V		-40°C ~125°C	1.2			V
EN Low Level	$V_{EN(LO)}$	V_{IN}=3.3V		-40°C ~125°C			0.4	V
Enable pin current	I_{EN}	EN = 0 V, V_{IN} = 3.3 V		-40°C ~125°C		1.5	10	µA
Soft-start Time (Note 4)	t_{SS}			-40°C ~125°C	0.35	0.9		ms
Power Supply Rejection	PSRR	V_{IN} = 5.0V V_{OUT} = 3.3V I_{OUT} = 100mA	f=100Hz	25°C		50		dB
			f=100kHz	25°C		30		
Thermal Shutdown Threshold	T_{SD}					150		°C
Thermal Shutdown Hysteresis	T_{HYS}					20		°C

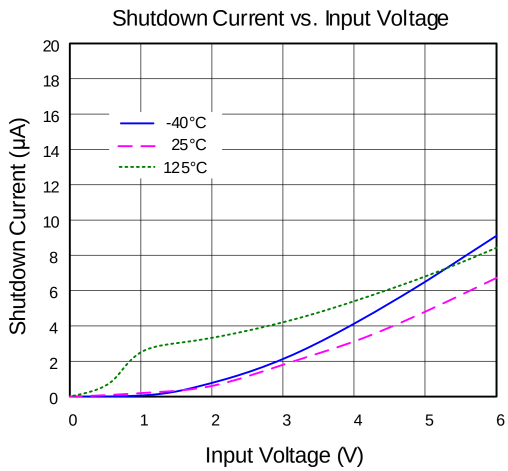
Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

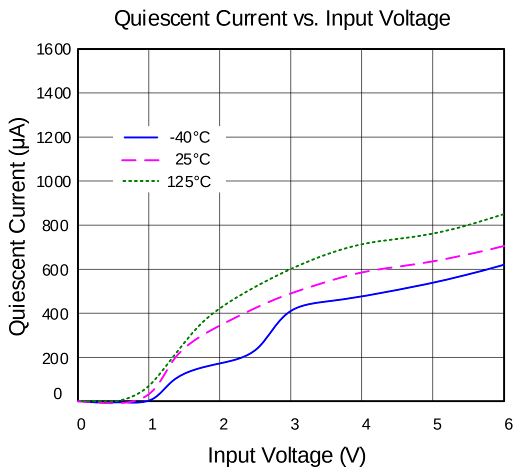
Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a Silergy evaluation board. Exposed Pad of DFN3×3-8 package is the case position for θ_{JC} measurement.

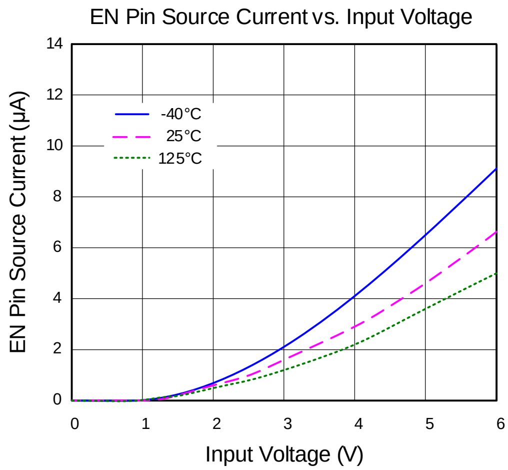
Note 3: The device is not guaranteed to function outside its operating conditions.

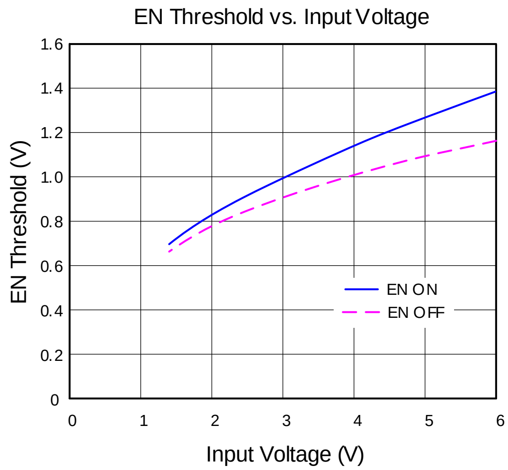
Note4: Time taken for the output to rise from 10% to 90% of the programmed output voltage.

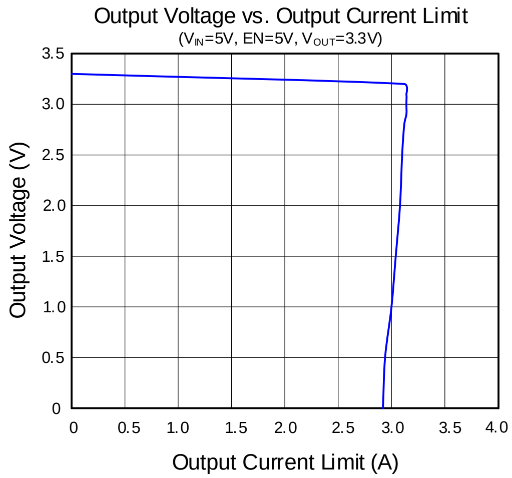
Typical Performance Characteristics

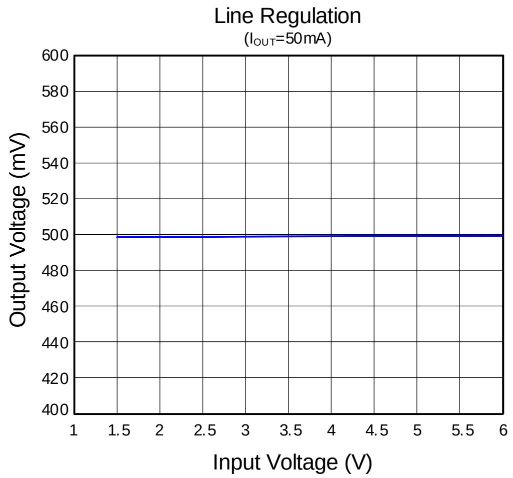




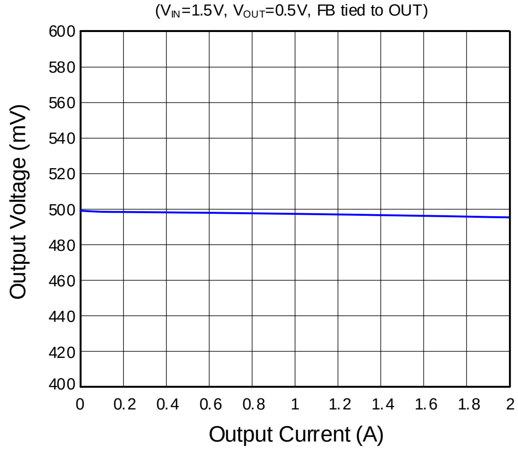




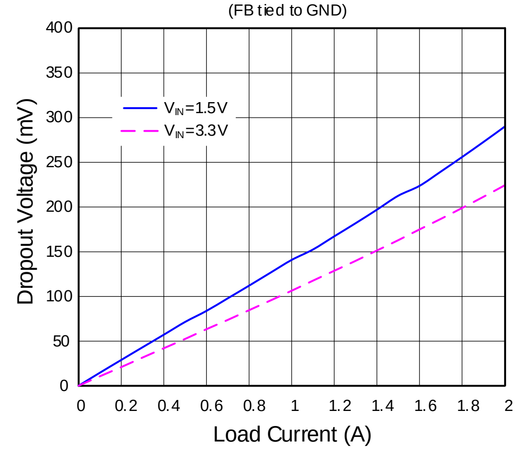




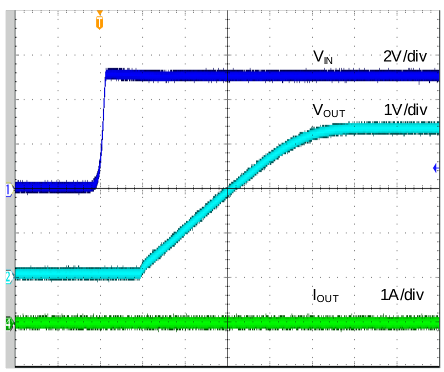
Load Regulation
(V_{IN}=1.5V, V_{OUT}=0.5V, FB tied to OUT)



Dropout Voltage vs. Load Current
(FB tied to GND)

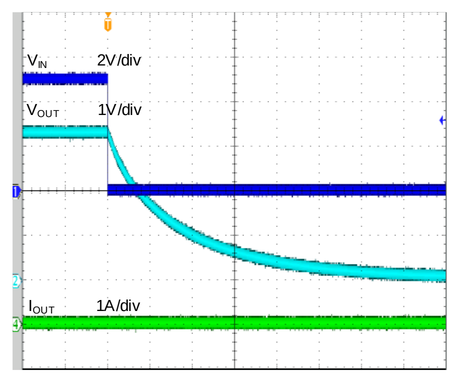


Startup from V_{IN}
(V_{IN}=5V, V_{OUT}=3.3V, C_{IN}=10µF, C_{OUT}=22µF, Null Load)



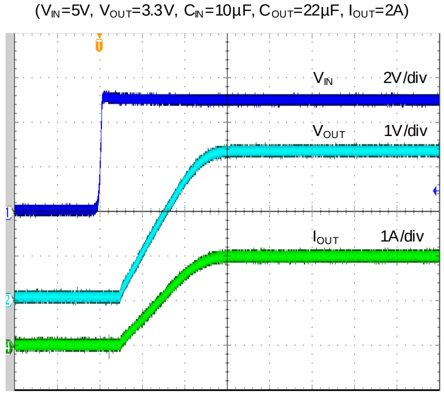
Time (200µs/div)

Shutdown from V_{IN}
(V_{IN}=5V, V_{OUT}=3.3V, C_{IN}=10µF, C_{OUT}=22µF, Null Load)



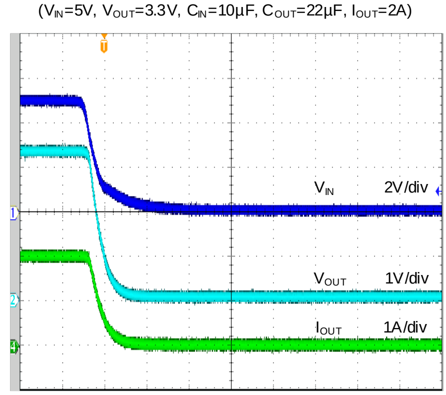
Time (1s/div)

Startup from V_{IN}
(V_{IN}=5V, V_{OUT}=3.3V, C_{IN}=10µF, C_{OUT}=22µF, I_{OUT}=2A)



Time (400µs/div)

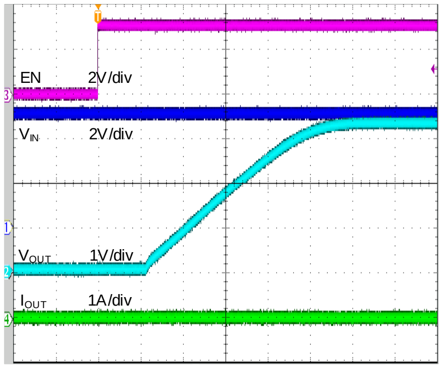
Shutdown from V_{IN}
(V_{IN}=5V, V_{OUT}=3.3V, C_{IN}=10µF, C_{OUT}=22µF, I_{OUT}=2A)



Time (200µs/div)

Startup from EN

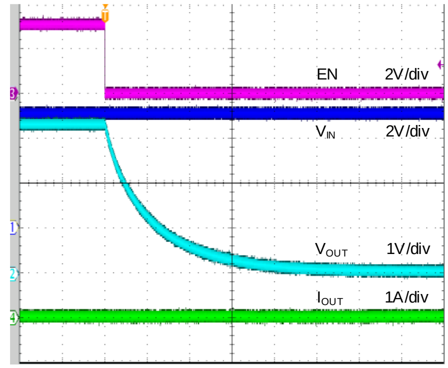
(V_{IN}=5V, V_{OUT}=3.3V, C_{IN}=10μF, C_{OUT}=22μF, Null Load)



Time (200μs/div)

Shutdown from EN

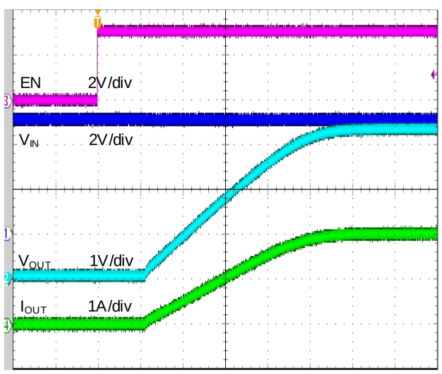
(V_{IN}=5V, V_{OUT}=3.3V, C_{IN}=10μF, C_{OUT}=22μF, Null Load)



Time (400ms/div)

Startup from EN

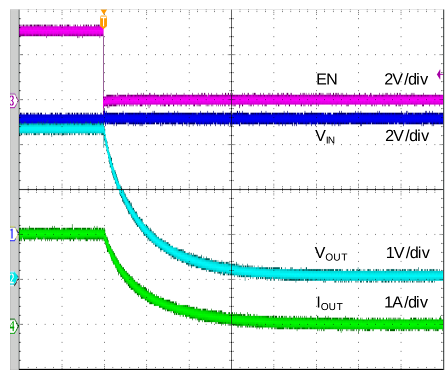
(V_{IN}=5V, V_{OUT}=3.3V, C_{IN}=10μF, C_{OUT}=22μF, I_{OUT}=2A)



Time (200μs/div)

Shutdown from EN

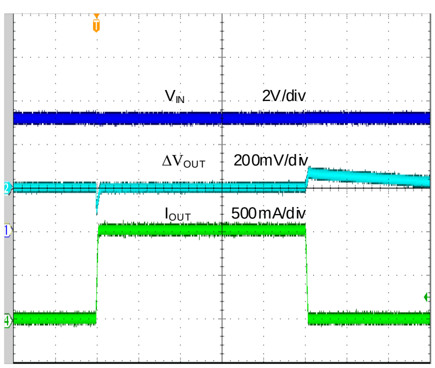
(V_{IN}=5V, V_{OUT}=3.3V, C_{IN}=10μF, C_{OUT}=22μF, I_{OUT}=2A)



Time (40μs/div)

Load Transient

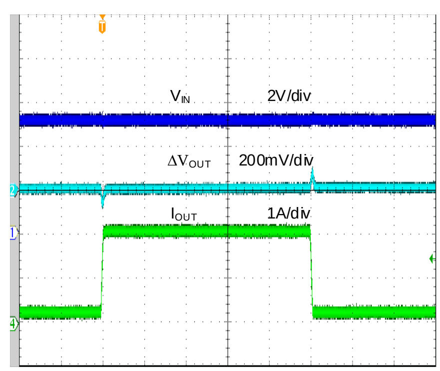
(V_{IN}=5V, V_{OUT}=3.3V, C_{OUT}=22μF, I_O=Null→1A →Null)



Time (800μs/div)

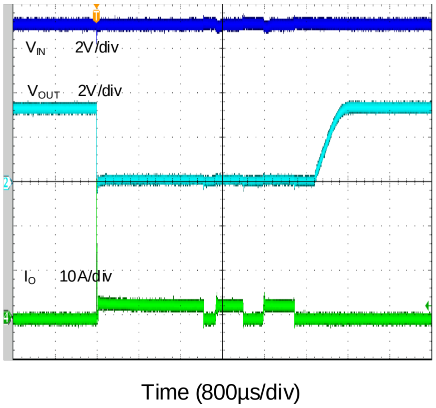
Load Transient

(V_{IN}=5V, V_{OUT}=3.3V, C_{OUT}=22μF, I_O=0.2A→2A →0.2A)

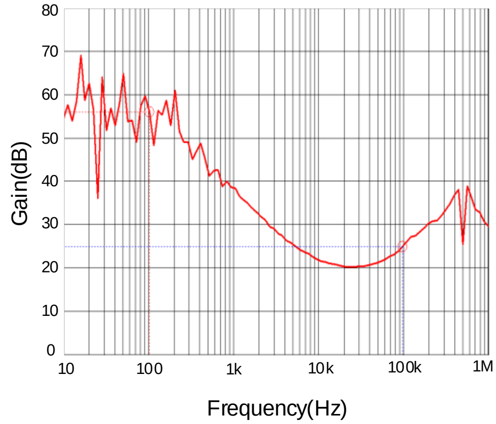


Time (800μs/div)

Short Protect
(V_{IN}=7V, V_{OUT}=3.3V)



PSRR
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=100mA)



Operation

The SY20739DAC is a high-performance positive voltage regulator designed for applications which require very low input voltage and very low dropout voltage at up to 2A output. It operates with a VIN as low as 1.5V, with output voltage programmable as low as 0.5V.

The SY20739DAC features ultra-low dropout, ideal for applications where VOUT is very close to VIN. Additionally, it has an enable pin to further reduce power dissipation while shut down. The device provides excellent regulation over variations in line, load, and temperature.

Applications Information

Input Capacitor CIN:

To minimize the potential noise problem and improve power-supply rejection ratio (PSRR) and transient response, place a typical X5R or better grade ceramic capacitor close to the IN and GND pins. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins. In this case, a 10µF low ESR ceramic capacitor is recommended.

Output Capacitor COUT:

For stable operation over the full temperature range, a 22µF low-ESR ceramic capacitor is recommended. Use 22µF to reduce noise, improve load-transient response and PSRR.

Feedback Resistor Dividers R3 and R2:

Choose R_3 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_3 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{OUT} is 3.3V, R_3=56kΩ is chosen, then using following equation, R_2 can be calculated to be 10kΩ:

$$R_2 = \frac{0.5V}{V_{OUT} - 0.5V} \times R_3$$

Over Current Protection:

The device includes over current protection. The current limitation circuit regulates the output current to its limitation threshold to protect IC from damage. Under over current condition, the power loss of the IC is relatively high. And that may trigger the thermal protection.

Enable Protection:

The enable pin for the SY20739DAC is active high. The output voltage is enabled when the enable pin voltage is greater than $V_{EN(HI)}$ and disabled with the enable pin voltage is less than $V_{EN(LO)}$. If independent control of the output voltage is not needed, then connect the enable pin to the input.

Thermal Considerations:

The SY20739DAC can deliver a current of up to 2A over the full operating temperature range. However, the maximum output current must be derated at higher ambient temperature. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$P_D=(V_{IN}-V_{OUT})\times I_{OUT}+V_{IN}\times I_{GND}$

The final operating junction temperature for any set of condition can be estimated by the following thermal equation:

$P_{D(MAX)}=(T_{J(MAX)}-T_A)/\theta_{JA}$

Where $T_{J(MAX)}$ is the maximum junction temperature of die (125 ℃) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA}) footprint is 41℃/W for DFN package.

PCB Layout Guide:

For best performance of the SY20739DAC, the following guidelines must be strictly followed:

1) Keep all Power traces (VIN / OUT / GND) as short and wide as possible and use at least 2-ounce copper for all Power traces.

2) Place a ground plane under all circuitry to lower both resistance and inductance and improve DC and transient performance.

3) Input and output capacitors should be placed closed to the SY20739 and connected to ground plane to reduce noise coupling.

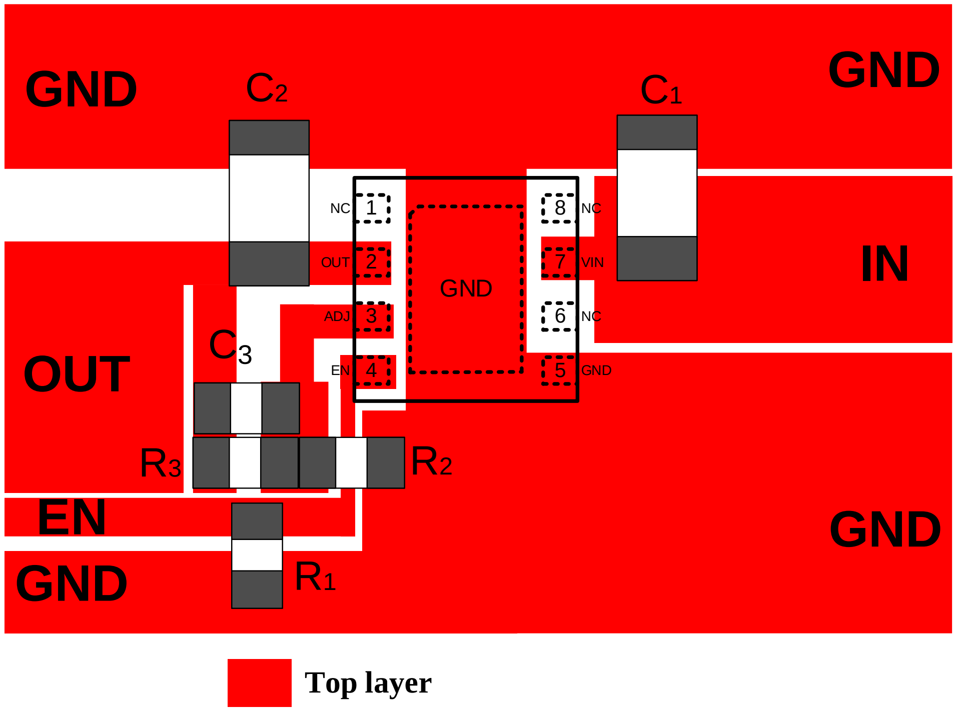
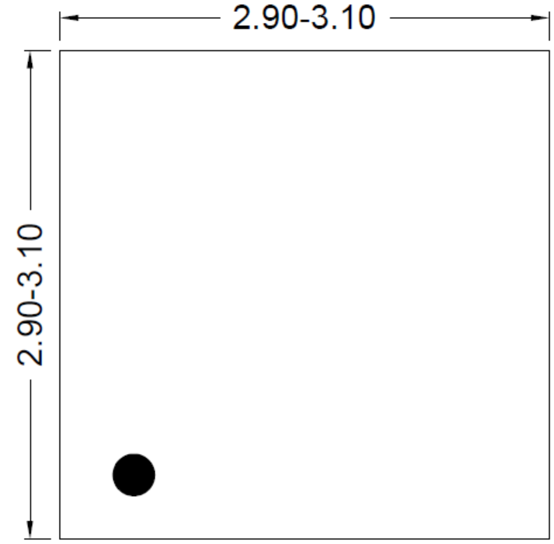
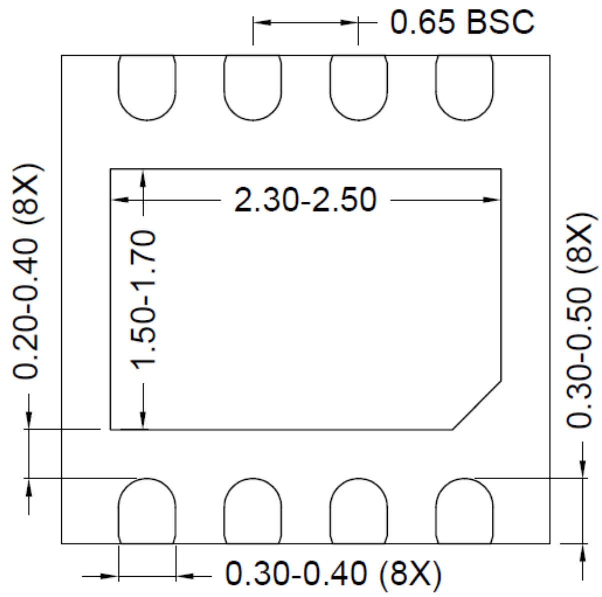


Figure3. PCB Layout Suggestion

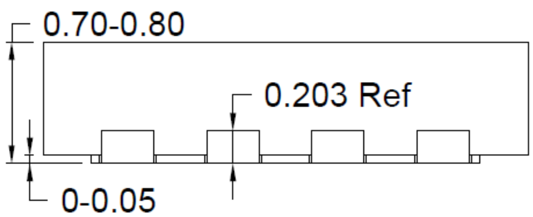
DFN3×3-8 Package Outline Drawing



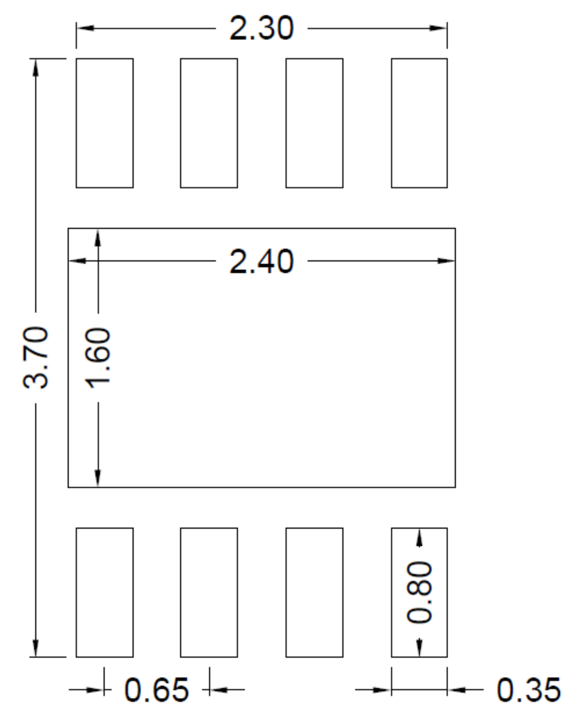
Top view



Bottom view



Front view

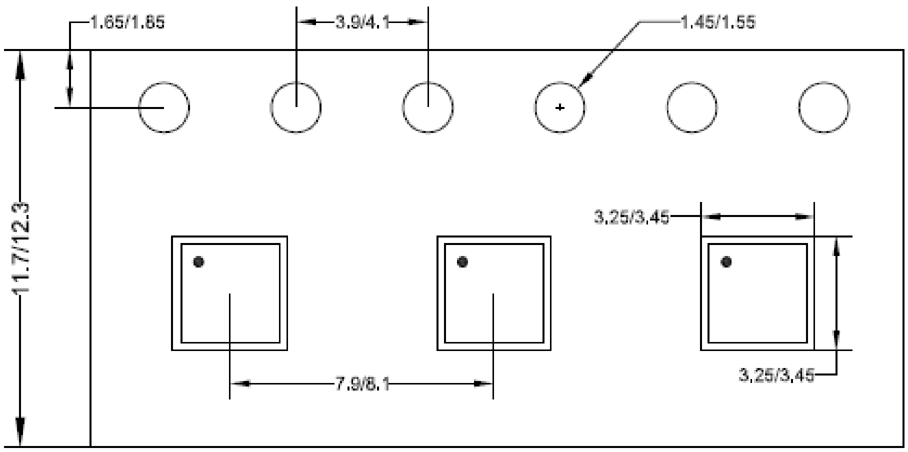


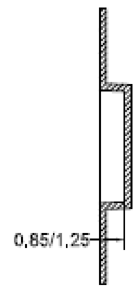
Recommended PCB layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

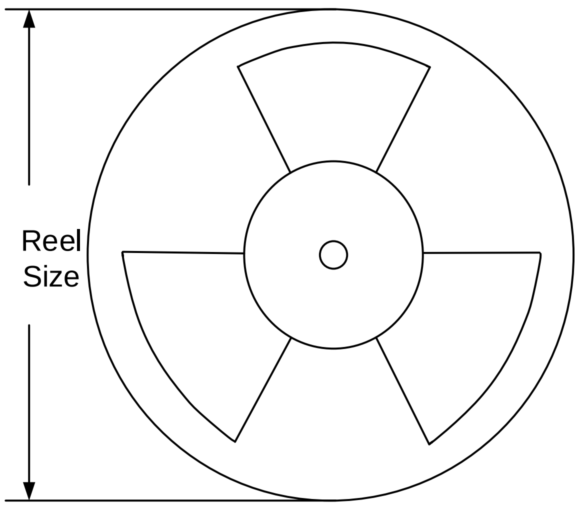
1. DFN3×3 taping orientation





Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
DFN3×3	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.21, 2024	Revision 1.0	Initial Production Release
Mar.25, 2024	Revision 0.9B	Update the package outline drawing (page11)
June 23, 2022	Revision 0.9A	θ_{JC} changed from 32℃/W to 5℃/W, updated the Note2.
Apr.21, 2022	Revision 0.9	Initial Release

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