



SILERGY

# SY20739FCC

## Low Input/Low dropout, 2A LDO with Enable

### General Description

The SY20739FCC is a high-performance positive voltage regulator designed for applications which require very low input voltage and very low dropout voltage at up to 2A output. It operates with a  $V_{IN}$  as low as 1.5V, with output voltage programmable as low as 0.5V. The SY20739FCC features ultra-low dropout, ideal for applications where  $V_{OUT}$  is very close to  $V_{IN}$ . Additionally, it has an enable pin to further reduce power dissipation while shut down. The device provides excellent regulation over variations in line, load, and temperature.

The SY20739FCC has an adjustable output which can be set by two external resistors. The SY20739FCC is available in the SO8E (Exposed Die Pad) package.

### Features

- Input Voltage as Low as 1.5V
- 400mV Dropout @ 2A
- Adjustable Output from 0.5V
- 0.9ms Internal Soft-start Minimizes Inrush Current
- 10µA Quiescent Current in Shutdown
- Over Current and Over Temperature Protection
- Enable Control: Default High
- Reverse Blocking from Output to Input
- Full Industrial Temperature Range
- RoHS Compliant and Halogen Free
- Packages: SO8E

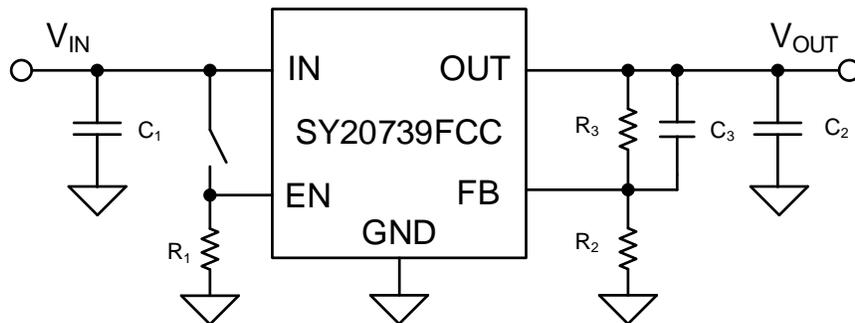
### Ordering Information

Ordering Number	Package Type	Note
SY20739FCC	SO8E	--

### Applications

- Telecom/Networking Cards
- Motherboards/Peripheral Cards
- Industrial Applications
- Wireless Infrastructure
- Set Top Box
- Medical Equipment
- Notebook Computers
- Battery Powered Systems

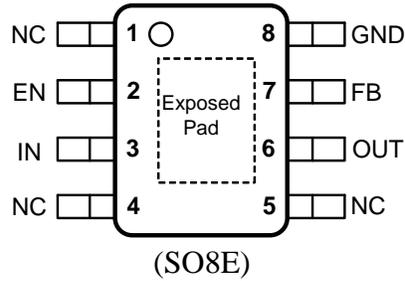
### Typical Applications



$$V_{OUT} = 0.5 \times \left( \frac{R_3 + R_2}{R_2} \right)$$

Figure1. Schematic Diagram

## Pinout (top view)



Top Mark: CYAxyz (Device code: CYA; x=year code, y=week code, z=lot number code)

Pin Name	Pin Name	Pin Description
NC	1, 4, 5	NO internal connection.
EN	2	Enable control input (Active-High). Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. The device will be enabled if this pin is left open.
IN	3	Input supply pin. For regulation at full load, the input to this pin must be between ( $V_{OUT} + 0.4V$ ) and 6V. Minimum input voltage is 1.5V. A large bulk capacitance should be placed closely to this pin to ensure that the input supply does not sag below 1.5V. Also, a minimum of 10 $\mu$ F ceramic capacitor should be placed directly at this pin.
OUT	6	Output pin. A minimum of 22 $\mu$ F capacitor should be placed directly at this pin.
FB	7	Feedback voltage input. If external feedback resistors are used, the output voltage will be determined by the resistor ratio.
GND	8	Ground pin.
Exposed Pad	/	The exposed pad should be connected to ground plane for better thermal performance.

## Block Diagram

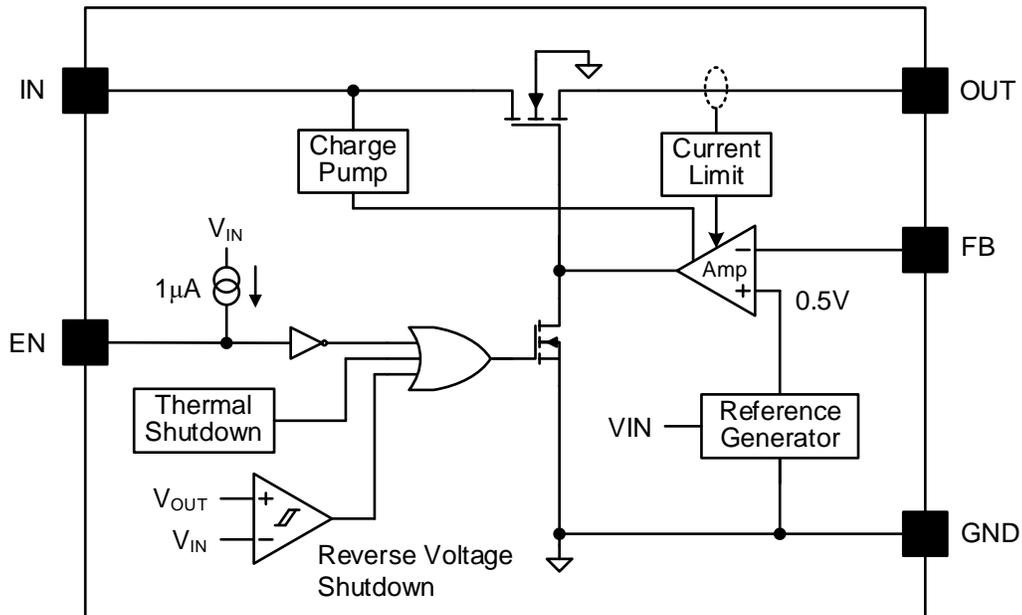


Figure2. Block Diagram



# SY20739FCC

## Absolute Maximum Ratings (Note 1)

IN, EN, OUT, FB	-0.3V to 7V
Power Dissipation, $P_D$ @ $T_A = 25^\circ\text{C}$	2.7W
Package Thermal Resistance (Note 2)	
$\theta_{JA}$	37°C/W
$\theta_{JC}$	3.9°C/W
Junction Temperature Range	40°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C

## Recommended Operating Conditions (Note 3)

IN	1.5V to 6V
Maximum Output Current	2A
Junction Temperature Range	-40°C to 125°C

## Electrical Characteristics

( $V_{IN}=V_{EN}=1.5$  to  $6V$ ;  $V_{OUT}=V_{FB}=0.5V$ ;  $I_{OUT}=10\mu A$  to  $2A$ ,  $C_{IN}=10\mu F$ ;  $C_{OUT}=22\mu F$ ;  $T_J=-40^{\circ}C$  to  $+125^{\circ}C$ . Typical values are at  $T_J=25^{\circ}C$ , unless otherwise specified. The values are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Test Conditions	$T_J$	Min	Typ	Max	Unit	
Input Voltage Range	$V_{IN}$		$-40^{\circ}C \sim 125^{\circ}C$	1.5		6	V	
Reference Accuracy	$V_{REF}$	$V_{IN}=3.3V, I_{OUT}=10mA$	$25^{\circ}C$	0.495	0.5	0.505	V	
			$-40^{\circ}C \sim 125^{\circ}C$	0.49	0.5	0.51		
		$1.5V < V_{IN} < 6V, 10mA < I_{OUT} < 2A$	$-40^{\circ}C \sim 125^{\circ}C$	0.485	0.5	0.515		
Line Regulation		$I_{OUT}=10mA$	$25^{\circ}C$		0.2		%/V	
Load Regulation		$10mA \leq I_{OUT} \leq 2A$	$25^{\circ}C$		0.3		%/A	
Shutdown Current	$I_{SD}$	$V_{IN}=6.0V, V_{EN}=0V$	$-40^{\circ}C \sim 125^{\circ}C$		10	50	$\mu A$	
Ground pin current	$I_{GND}$	$V_{IN}=3.3V, I_{OUT}=0A$	$-40^{\circ}C \sim 125^{\circ}C$			3	mA	
Dropout Voltage	$V_{DO}$	$I_O=1A$	$1.5V \leq V_{IN} < 1.6V$	$-40^{\circ}C \sim 125^{\circ}C$		90	400	mV
			$1.6V \leq V_{IN} \leq 6V$	$-40^{\circ}C \sim 125^{\circ}C$			200	
		$I_O=1.5A$	$1.5V \leq V_{IN} < 1.6V$	$-40^{\circ}C \sim 125^{\circ}C$		200	500	
			$1.6V \leq V_{IN} \leq 6V$	$-40^{\circ}C \sim 125^{\circ}C$			300	
		$I_O=2A$	$1.5V \leq V_{IN} < 1.6V$	$-40^{\circ}C \sim 125^{\circ}C$		300	600	
			$1.6V \leq V_{IN} \leq 6V$	$-40^{\circ}C \sim 125^{\circ}C$			400	
Minimum Load Current	$I_{O,MIN}$		$-40^{\circ}C \sim 125^{\circ}C$			10	$\mu A$	
Output Current Limit	$I_{LIMIT}$	$V_{IN}=3.3V$	$-40^{\circ}C \sim 125^{\circ}C$	2.1	3	4.4	A	
Feedback Pin Current	$I_{FB}$	$V_{IN}=V_{REF}$	$-40^{\circ}C \sim 125^{\circ}C$		80	200	nA	
EN High Level	$V_{EN(HI)}$	$V_{IN}=3.3V$	$-40^{\circ}C \sim 125^{\circ}C$	1.2			V	
EN Low Level	$V_{EN(LO)}$	$V_{IN}=3.3V$	$-40^{\circ}C \sim 125^{\circ}C$			0.4	V	
Enable pin current	$I_{EN}$	$EN=0V, V_{IN}=3.3V$	$-40^{\circ}C \sim 125^{\circ}C$		1.5	10	$\mu A$	
Soft-start Time (Note 4)	$t_{SS}$		$-40^{\circ}C \sim 125^{\circ}C$	0.35	0.9		ms	
Power Supply Rejection	PSRR	$V_{IN}=5.0V$ $V_{OUT}=3.3V$ $I_{OUT}=100mA$	$f=100Hz$	$25^{\circ}C$		50	dB	
			$f=100kHz$	$25^{\circ}C$		30		
Thermal Shutdown Threshold	$T_{SD}$				150		$^{\circ}C$	
Thermal Shutdown Hysteresis	$T_{HYS}$				20		$^{\circ}C$	

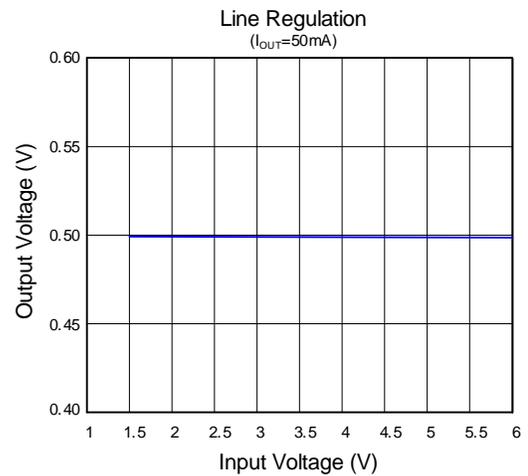
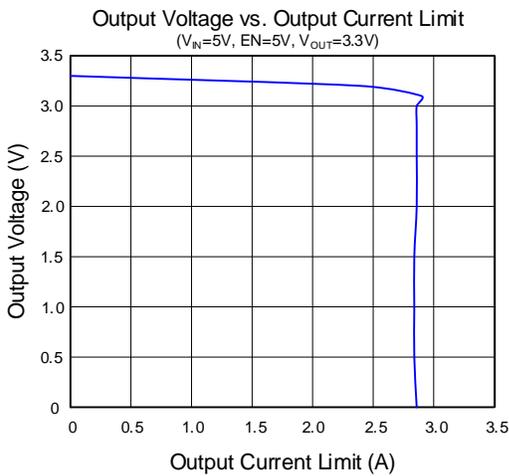
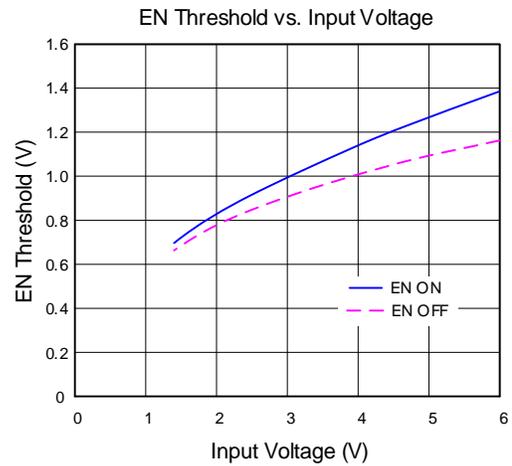
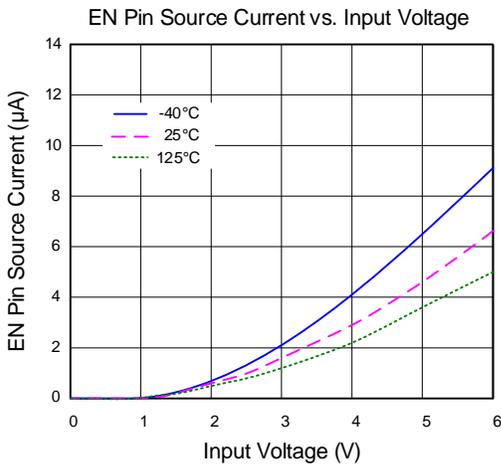
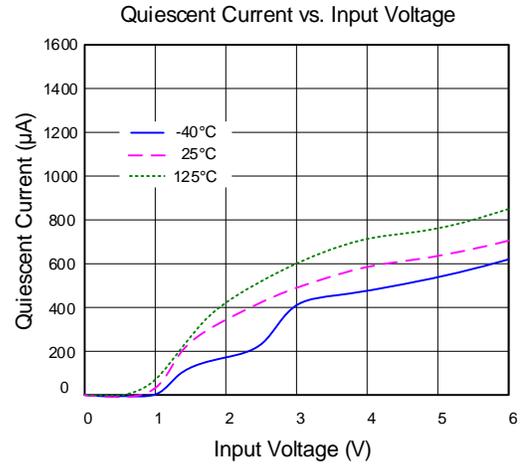
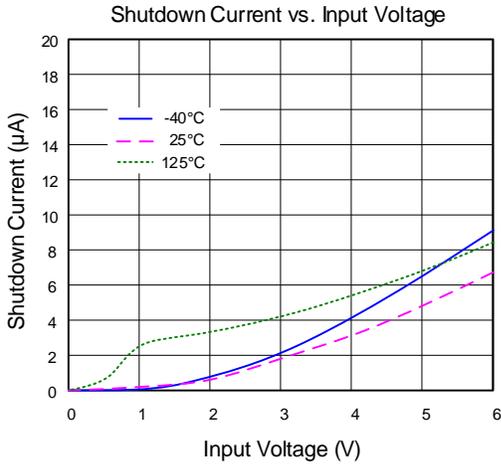
**Note 1:** Stresses beyond “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

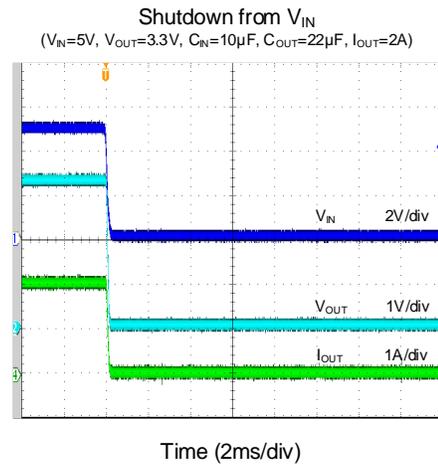
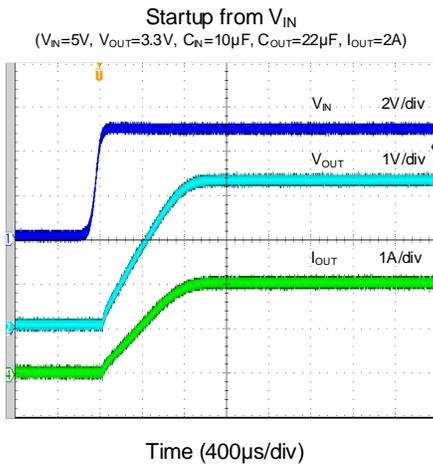
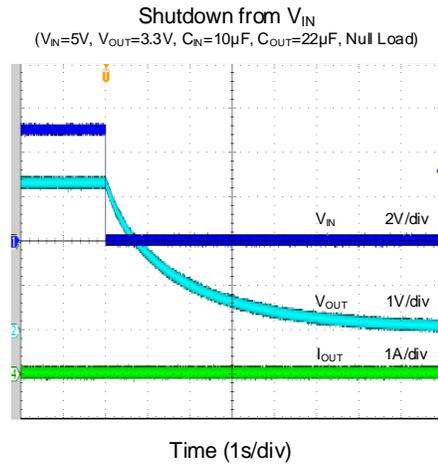
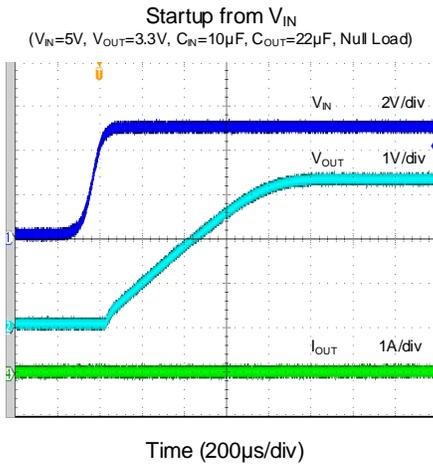
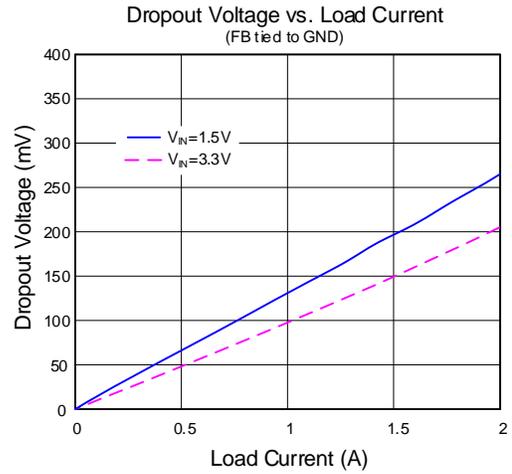
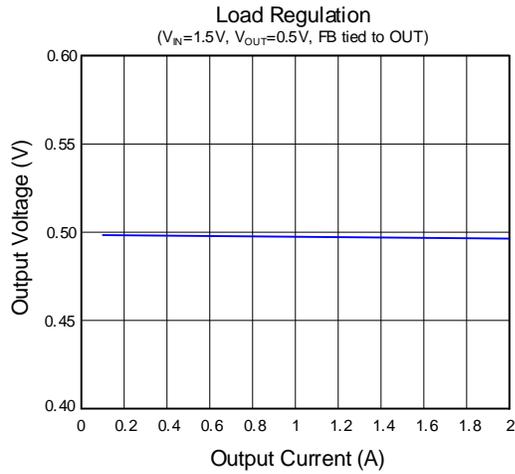
**Note 2:**  $\theta_{JA}$  is measured in the natural convection at  $T_A=25^{\circ}C$  on a Silergy evaluation board. Exposed Pad of SO8E package is the case position for  $\theta_{JC}$  measurement.

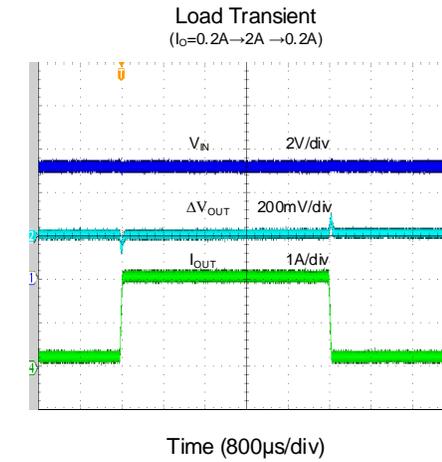
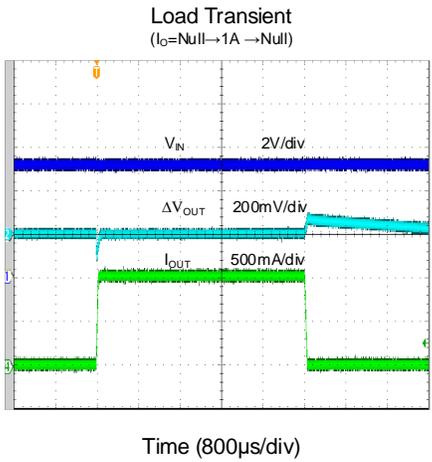
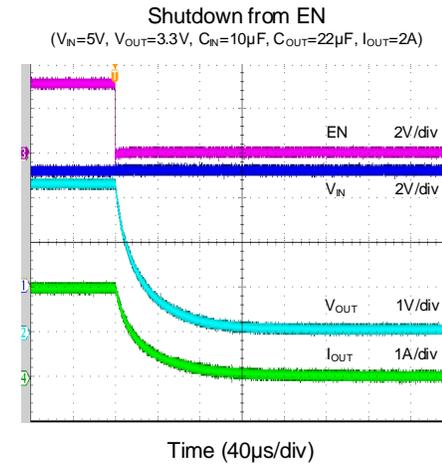
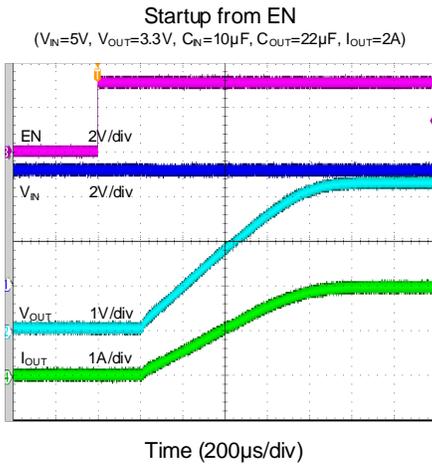
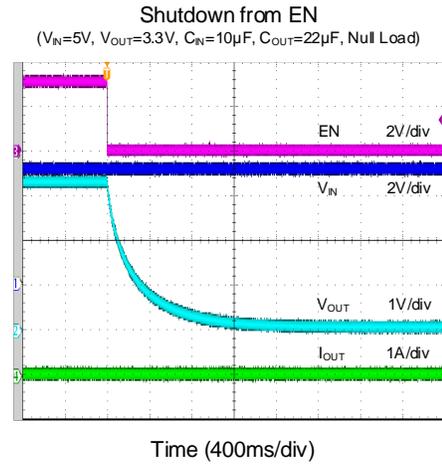
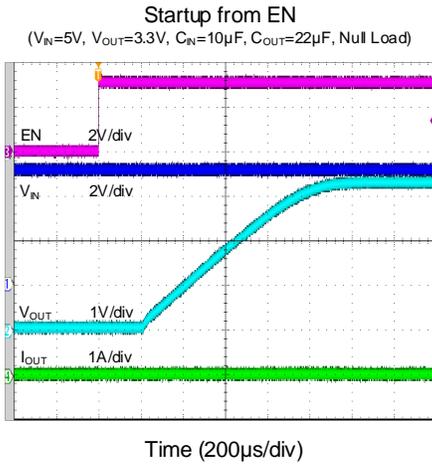
**Note 3:** The device is not guaranteed to function outside its operating conditions.

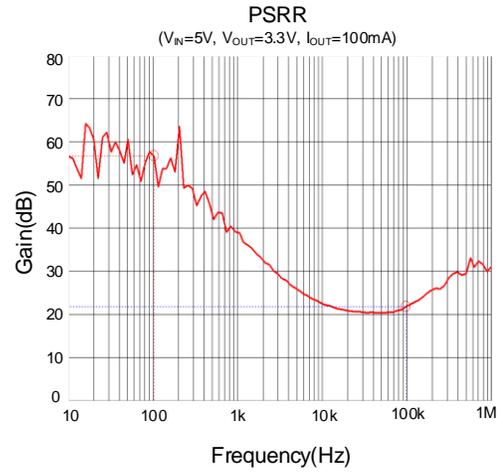
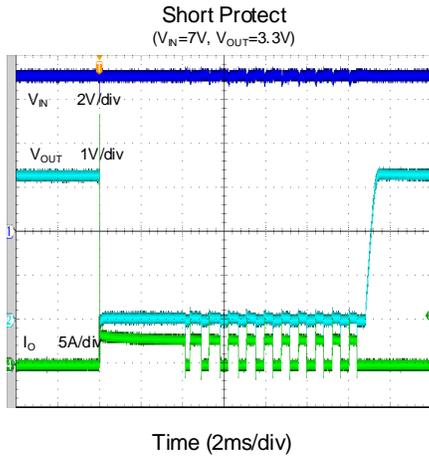
**Note 4:** Time taken for the output to rise from 10% to 90% of the programmed output voltage.

## Typical Performance Characteristics









## Operation

The SY20739FCC is a high-performance positive voltage regulator designed for applications which require very low input voltage and very low dropout voltage at up to 2A output. It operates with a VIN as low as 1.5V,

with output voltage programmable as low as 0.5V. The SY20739FCC features ultra-low dropout, ideal for applications where VOUT is very close to VIN. Additionally, it has an enable pin to further reduce power dissipation while shut down. The device provides excellent regulation over variations in line, load, and temperature.

## Applications Information

### Input Capacitor CIN:

To minimize the potential noise problem and improve power-supply rejection ratio (PSRR) and transient response, place a typical X5R or better grade ceramic capacitor close to the IN and GND pins. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins. In this case, a 10μF low ESR ceramic capacitor is recommended.

### Output Capacitor COUT:

For stable operation over the full temperature range, a 22μF low-ESR ceramic capacitor is recommended. Use 22μF to reduce noise, improve load-transient response and PSRR.

### Feedback Resistor Dividers R3 and R2:

Choose R3 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R3 and R2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If VOUT is 3.3V, R3=56kΩ is chosen, then using the following equation, R2 can be calculated to be 10kΩ:

$$R_2 = \frac{0.5V}{V_{OUT} - 0.5V} \times R_3$$

### Over Current Protection:

The device includes over current protection. The current limitation circuit regulates the output current to its limitation threshold to protect IC from damage. Under over current condition, the power loss of the

IC is relatively high. And that may trigger the thermal protection.

### Enable Protection:

The enable pin for the SY20739FCC is active high. The output voltage is enabled when the enable pin voltage is greater than VEN(HI) and disabled with the enable pin voltage is less than VEN(LO). If independent control of the output voltage is not needed, then connect the enable pin to the input.

### Thermal Considerations:

The SY20739FCC can deliver a current of up to 2A over the full operating temperature range. However, the maximum output current must be derated at higher ambient temperature. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

The final operating junction temperature for any set of condition can be estimated by the following thermal equation:

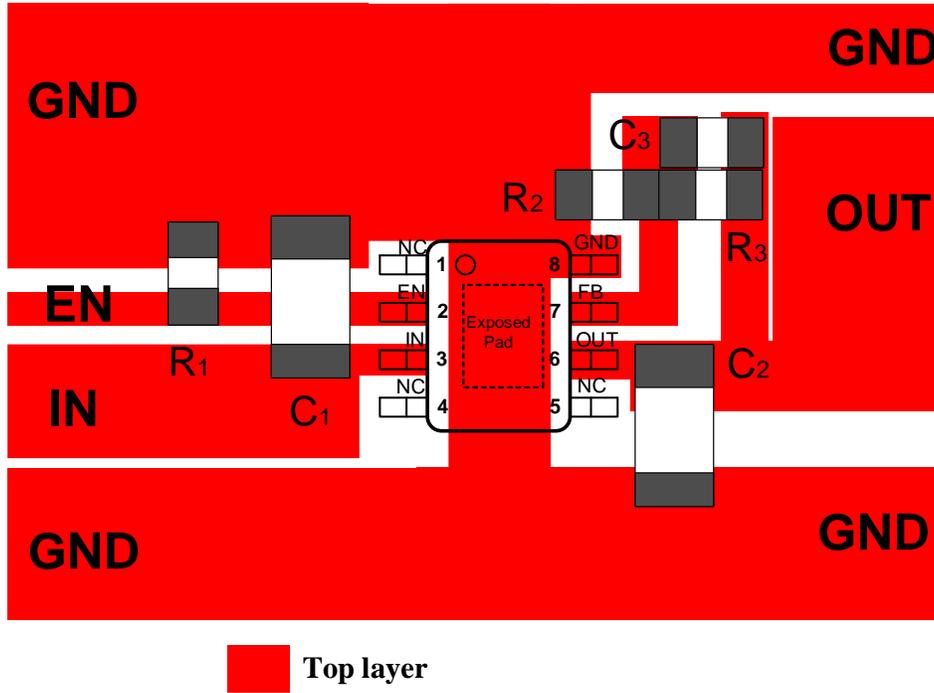
$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where TJ(MAX) is the maximum junction temperature of die (125 °C ) and TA is the maximum ambient temperature. The junction to ambient thermal resistance (θJA) footprint is 37 °C /W for SO8E package.

### PCB Layout Guide:

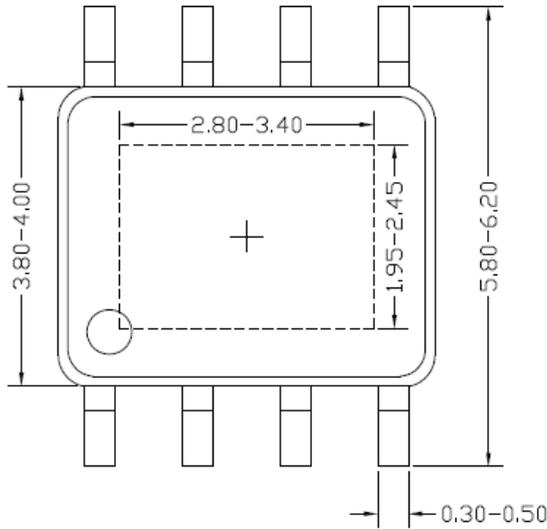
For best performance of the SY20739FCC, the following guidelines must be strictly followed:

- 1) Keep all Power traces (IN / OUT / GND) as short and wide as possible and use at least 2-ounce copper for all Power traces.
- 2) Place a ground plane under all circuitry to lower both resistance and inductance and improve DC and transient performance.
- 3) Input and output capacitors should be placed closed to the SY20739FCC and connected to ground plane to reduce noise coupling.

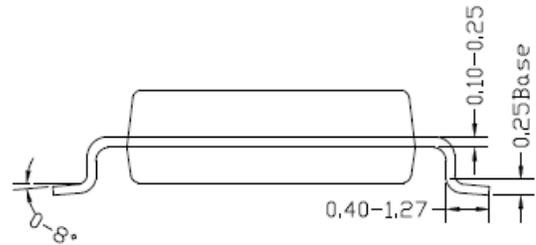


**Figure3. PCB Layout Suggestion**

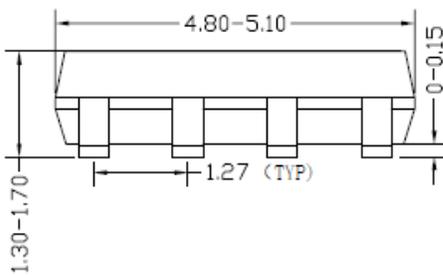
**SO8E Package Outline & PCB Layout**



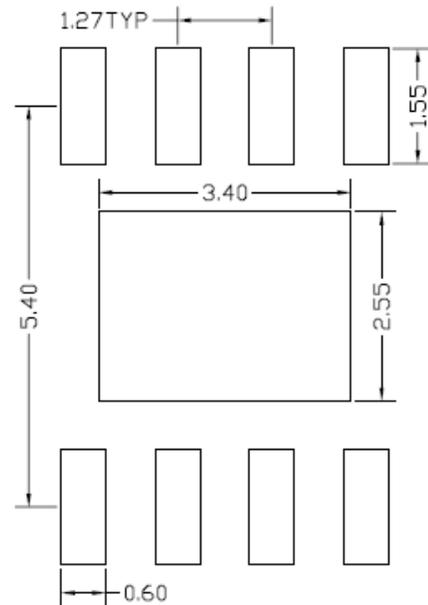
**Top view**



**Side view**



**Front view**



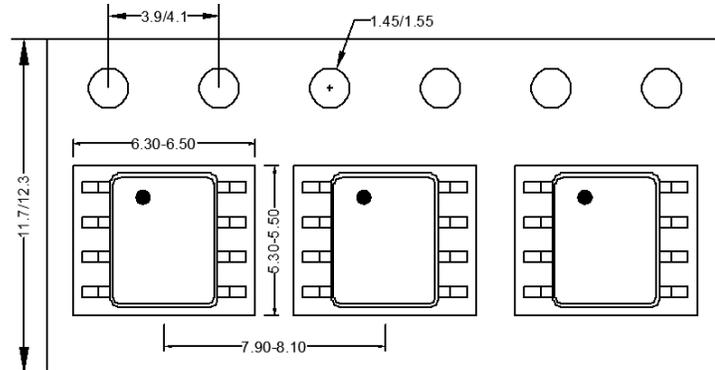
**Recommended PCB Layout  
(Reference Only)**

**Notes: All dimension in millimeter and exclude mold flash & metal burr.**

## Taping & Reel Specification

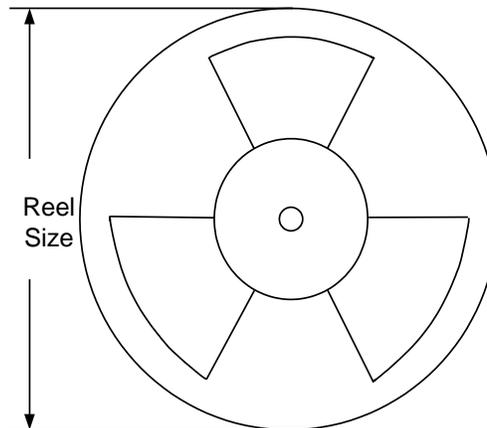
### 1. Taping orientation

**SO8E**



Feeding direction →

### 2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SO8E	12	8	13"	400	400	2500

**Others: NA**

## Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.21, 2023	Revision 1.0	Initial Production Release
June 23, 2022	Revision 0.9A	$\theta_{JC}$ changed from 50.5°C/W to 3.9°C/W, updated the Note2.
Apr.21, 2022	Revision 0.9	Initial Release



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