SY20754

Wide Input, High Current, Bi-Directional Regulator for Single Cell Li-ion Battery Power Bank Applications

General Description

The SY20754 is a 4.0-13.5V input voltage range, bi-directional regulator for Li-Ion battery power bank applications. It utilizes advanced bi-directional energy flow control with automatic input power source detection, enabling seamless switching between battery charging and suppling power to external devices.

When connected to an external power supply, the SY20754 operates in battery charge mode, offering comprehensive protection functions. Without an external power supply, it switches to battery power supply mode, capable of delivering an output current of up to 3A.

The SY20754 has an integrated reverse blocking MOSFET to prevent current leaking from the system or battery side to the input side and an integrated linear switch to enable overvoltage and overcurrent protection on the system side.

The device uses a half-bridge architecture with a quasi-fixed 0.5MHz switching frequency, for efficient power conversion in both battery charging and power supply modes. The half-bridge utilizes N-channel MOSFETs with a 16V rating and extremely low RDS(ON), enhancing efficiency and extending the battery life.

The small size and simple application schematic make SY20754 a good candidate for single cell battery power banks and other battery backup applications.

The device is available in a compact QFN4x4 package.

Features

- Integrated N-channel MOSFETs with 16V Voltage Rating and Extremely Low $R_{DS(ON)}$
- 500 KHz Switching Frequency
- Constant Current / Constant Voltage /Trickle Current Charging Modes
- Maximum 5A Battery Charging Current
- Maximum 3A System Current in Battery Power Supplement Mode
- USB Port Identifier for Various Input Current Limits
- Automatic Input Power Source Detection
- I^2C Controls
  - Selectable Battery Charge Voltage
  - Programmable Constant Charge Current
  - Programmable Overcurrent Limit for SYS Load
  - Programmable Battery Charging Timeout
  - Programmable Input Current DPM
  - Programmable Input Voltage DPM
- Charging Shutdown Control
- Charging Mode CV Tolerance +/-0.5%
- DO+/DO- Divider Mode Compliant
- Host Enable Control for Standby Mode
- Overtemperature Protection
- Charge Status Indication
- Light Load Status Indication

Applications

- Single-Cell Li-Ion Power Banks
- Portable Devices with Single Cell Battery Packs

Typical Application

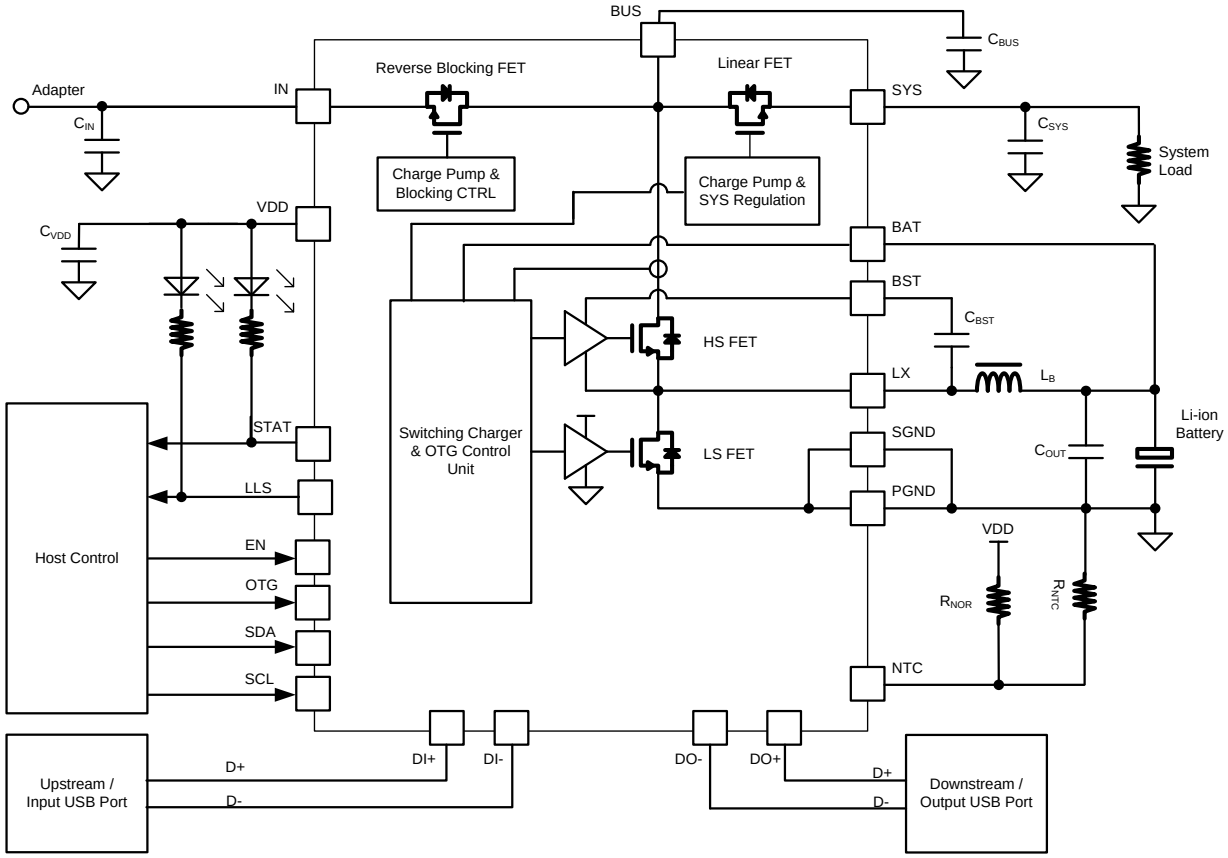


Figure 1. Schematic Diagram

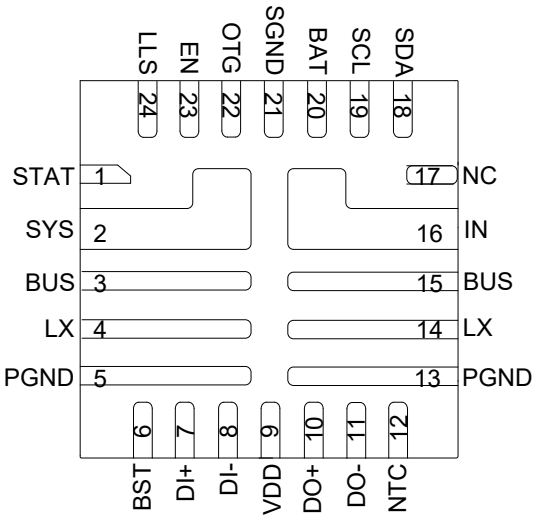
Ordering Information

SY20754□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package Type	Top Mark
SY20754QCC	QFN4x4-24	**BGW*xyz***

Device code: **BGW**
x=year code, y=week code, z= lot number code

Pinout (Top view)



(QFN4x4-24)

Pin Name	Pin Number	Pin Description
STAT	1	Charging status indication pin. It is an open-drain output and can be used for turning on a LED to indicate a charge in process. When the charge is done, the LED will turn off. STAT pin will be pulled low for about 200μs when DI+, DI-, DO+, DO- pins handshake is done.
SYS	2	System load pin. Connect an MLCC from this pin to the ground to decouple the high frequency noise.
BUS	3,15	Connection point for reverse blocking MOSFET and bypass linear switch. Connect an MLCC from this pin to the ground to decouple the high frequency noise.
LX	4,14	Switch node pin. Connect an external inductor from this pin to the BAT pin.
PGND	5,13	Power ground pin.
BST	6	Bootstrap pin. Connect an MLCC from this pin to LX.
DI+	7	Host USB D+ connection. For USB input identification.
DI-	8	Host USB D- connection. For USB input identification.
VDD	9	Internal Linear regulator output. VDD is the output of a 3.3V linear regulator. The LDO is active when EN is high. Connect a 1μF ceramic capacitor from VDD to GND.
DO+	10	USB D+ for system connection. Supports divider mode and BC1.2 handshake.
DO-	11	USB D- for system connection. Supports divider mode and BC1.2 handshake.
NTC	12	Thermal protection and battery detection pin. In charging mode, the UTP threshold is 65% of VDD, and the OTP threshold is about 35% of VDD. In discharging mode, the UTP threshold is about 81% of VDD, and the OTP threshold is about 30% of VDD.
IN	16	Positive power supply input pin. V_{IN} ranges from 4V to 13.5V during normal operation and up to 16V transients. Connect an MLCC from this pin to the ground to decouple high frequency noise.
NC	17	Not Connect.
SDA	18	I^2C Interface data.
SCL	19	I^2C Interface clock.
BAT	20	Battery positive sense pin.
SGND	21	Signal ground pin.

OTG	22	Enable control pin for system power supply. If the external power source is present, pull down OTG to shut down the linear FET. If the external power source is absent, pull down OTG to shut down the linear FET and the sync-Boost converter to save the leakage power from the battery.
EN	23	Device enable pin. When EN is high, operation is enabled
LLS	24	System light load indicator. Open-drain output pin, can be used to turn on an LED to indicate the light system load condition lower than 50mA/200mA (configured by I^2C).

Absolute Maximum Ratings (Note 1)

IN, LX, BUS, BAT, SYS ---------- -0.5~18V
STAT, SCL, SDA, DI+, DI-, DO+, DO-, EN, OTG, LLS ---------- -0.5~18V
VDD, BST-LX ---------- -0.5~ 4V
NTC ---------- -0.5~ 5V
Power Dissipation, P_D @ T_A = 25°C, ---------- 2.5 W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 40 °C/W
θ_{JC} ---------- 20 °C/W
Junction Temperature Range ---------- -40°C to +150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 125°C

Recommended Operating Conditions (Note 3)

IN, LX, BUS, BAT, SYS ---------- 0~16V
STAT, SCL, SDA, DI+, DI-, DO+, DO-, EN, OTG, LLS ---------- 0~16V
VDD, BST-LX ---------- 0~ 3.6V
NTC ---------- -0.5~5V
Junction Temperature Range ---------- -20°C to 100°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(T_A=25°C, T_A=T_J, V_{IN}=5V, GND=0V, C_{IN}=20μF, L_B=2.2μH, C_{OUT}=20μF, C_{BUS}=20μF, C_{SYS}=10μF, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Quiescent Current						
Battery Leakage Current	I_{BAT}	EN and OTG pull down		5	10	μA
Input Quiescent Current	I_{IN}	EN=OTG=High, NTC=0V		1		mA
Boost Null-load Battery Discharge Current	I_{BOOST}	V_{BAT}=4.35V,Vsys=5V, I_{SYS}=0V, Converter switching		2		mA
Input Power Supply						
Input Supply Voltage for Battery Charging	V_{IN}		4.5		13.5	V
Input Voltage UVLO Threshold	V_{INUVLO}		3.8	4	4.1	V
Input Voltage UVLO Hysteresis	V_{UVHYS}	Falling edge		200		mV
Input Voltage OVP Threshold in LV Mode	V_{INOVP_LV}	Rising edge	6.7			V
Input Voltage OVP Hysteresis in LV Mode	$V_{INOVPHYS\_LV}$	Falling edge		0.35		V
Input Voltage OVP Threshold in HV Mode	V_{INOVP_HV}	Rising edge	13.8			V
Input Voltage OVP Hysteresis in HV Mode	$V_{INOVPHYS\_HV}$	Falling edge		0.7		V
LDO Output						
VDD Voltage	V_{VDD}	V_{BUS}=5V		3.3		V
VDD Short Limit Current	I_{SHORT_VDD}	V_{VDD}=0V	50	110	170	mA
Linear FET						
$R_{DS(ON)}$ of The Linear NFET	R_{LNFT}			30		mΩ
System Current Limit Tolerance in Boost Mode	$I_{SYSLIMIT}$		-8		12	%
System Clamp Voltage Tolerance	V_{SYSMAX}	DCP mode	5.65	5.8	5.95	V
		HVDCP mode	12.7	13	13.3	V
Blocking FET						
$R_{DS(ON)}$ of Reverse Blocking NFET	R_{BKFT}			35		mΩ
Half-bridge in Buck Mode						
Voltage and Current Bias						
BUS Supply Voltage for Battery Charging	V_{BUS}		4.5		13.5	V
BUS Voltage OVP Threshold in LV Mode	$V_{BOVP\_LV\_BK}$	Rising edge	7.4	7.75	8.1	V
BUS Voltage OVP Hysteresis in LV Mode	$V_{BOVPHYS\_LV\_BK}$	Falling edge		0.55		V
BUS Voltage OVP Threshold in HV Mode	$V_{BOVP\_HV\_BK}$	Rising edge	13.4	13.75	14.2	V
BUS Voltage OVP Hysteresis in HV Mode	$V_{BOVPHYS\_HV\_BK}$	Falling edge		1		V

Switching Frequency						
Buck Switching Frequency	f_{SWBK}			0.5		MHz
Min on Time for Charging Mode, HS FET	$T_{ONMINHS}$			100		ns
Max on Time for Charging Mode, HS FET	$T_{ONMAXHS}$	In low dropout mode		7		µs
Battery Charging						
Battery CV Voltage Tolerance	V_{CV}	Voltage on BAT pin	-0.5		0.5	%
Battery Voltage Threshold Hysteresis for Recharge	ΔV_{RCH}	Falling edge		100		mV
Battery Trickle Charging Mode Voltage Threshold	V_{TRK}	Rising edge	2.7	2.8	2.9	V
Charging Current Accuracy for Constant Current Mode Charging Current Accuracy for Constant Current Mode	I_{CC}	REG03[2:0]=011,I_{CC}=2A, V_{BAT}=3.5V	-8		12	%
		REG03[2:0]=111,I_{CC}=5A, V_{BAT}=3.5V	-8		12	%
Termination Current Tolerance	I_{TERM}	V_{IN}=5V, REG03[2:0]=011. REG01[0]=0, I_{TERM}=100mA	-25		+25	%
		V_{IN}=5V, REG03[2:0]=001. REG01[0]=0, I_{TERM}=50mA	-45		+45	%
Battery Voltage OVP Threshold	V_{BTOVP}		105%	110%	115%	V_{CV}
Battery Short Circuit Protection						
Battery Short Circuit Protection Threshold	$V_{SHORTBT}$			2		V
Dynamic Input Power Management						
Input Current Limit Tolerance	I_{DPM}	REG02[7:5]=011,IDPM=1.5A	-12		+12	%
Input Voltage Regulation During Input Voltage Dynamic Power Management	V_{DPM}	LV mode	-2		+2	%
		HV mode	-2.5		+2.5	%
USB Port Identification and Current Limit Reference						
Input Current Limit Tolerance While Input is SDP	I_{SDP}	Input is SDP, IDPM=0.5A	-15		+15	%
Input Current Limit Tolerance While Input is DCP	I_{DCP}	Input is DCP, IDPM=1.5A	-12		+12	%
Half-bridge in Boost Mode						
Voltage and Current Bias						
Battery Depletion Voltage Tolerance	V_{BATDEP}	Falling edge	2.5	2.6	2.7	V
Battery Depletion Voltage	$V_{BATDEPHYS}$	Rising edge		0.28		V
BUS Voltage OVP Threshold in LV Mode	$V_{BOVPHYS\_LV\_BT}$	Rising edge	7.4	7.75	8.1	V
BUS Voltage OVP Hysteresis in LV Mode	$V_{BOVPHYS\_LV\_BT}$	Falling edge		0.55		V
BUS Voltage OVP Threshold in HV Mode	$V_{BOVP\_HV\_BT}$	Rising edge	13.4	13.75	14.2	V

BUS Voltage OVP Hysteresis in HV Mode	$V_{BOVPHYS\_HV\_BT}$	Falling edge		1		V
SYS Voltage Tolerance	V_{SYS}		-2%		+2%	V_{SYS}
OTG Light Load Threshold	I_{SYS_LOW}	REG02[1:0]=10,ISYS_LOW=50mA, falling edge	20	50	75	mA
		REG02[1:0]=11,ISYS_LOW=200mA , falling edge	155	200	255	mA
Switching Frequency						
Boost Switching Frequency	f_{SWBST}			0.5		MHz
Min on Time for Discharging Mode, LS FET	T_{ONMINL}			200		ns
Other General Parameters						
Battery Thermal Protection NTC						
Battery Removed	Battery Detection	Rising edge	88%			V_{DD}
Under Temperature Protection	UTP_CHG	Rising edge, charging mode	63%	65%	67%	
Under Temperature Protection Hysteresis		Falling edge, charging mode		5%		
Over Temperature Protection	OTP_CHG	Falling edge, charging mode	33%	35%	37%	
Over Temperature Protection Hysteresis		Rising edge, charging mode		2%		
Under Temperature Protection	UTP_DCHG	Rising edge, discharging mode	79%	81%	83%	
Under Temperature Protection Hysteresis		Falling edge, discharging mode		5%		
Over Temperature Protection	OTP_DCHG	Falling edge, discharging mode	28%	30%	32%	
Over Temperature Protection Hysteresis		Rising edge, discharging mode		2%		
Power MOSFET						
$R_{DS(ON)}$ of High-side NFET	R_{HSFT}			15		mΩ
$R_{DS(ON)}$ of Low-side NFET	R_{LSFT}			10		mΩ
Half Bridge FET Current Limit in Buck Mode	I_{PEAK_BK}		6.5			A
Half Bridge FET Current Limit in Boost Mode	I_{PEAK_BT}		9			A
Logic Level and Timing						
EN, OTG,SCL,SDA Low Level Threshold	V_{LOW}				0.4	V
EN, OTG,SCL,SDA Low Level Threshold	V_{HIGH}		1.3			V

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

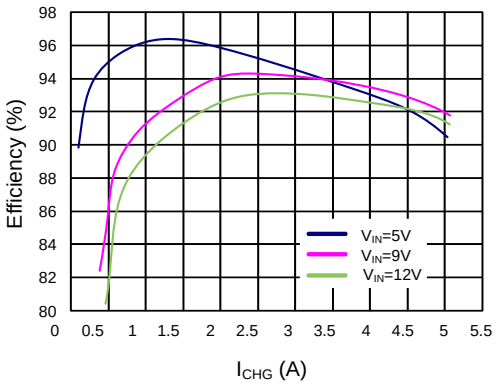
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

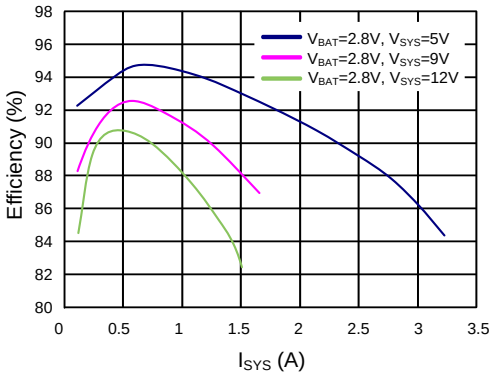
Typical Performance Characteristics

(T_A=25°C, V_{IN}=5V, unless otherwise specified.)

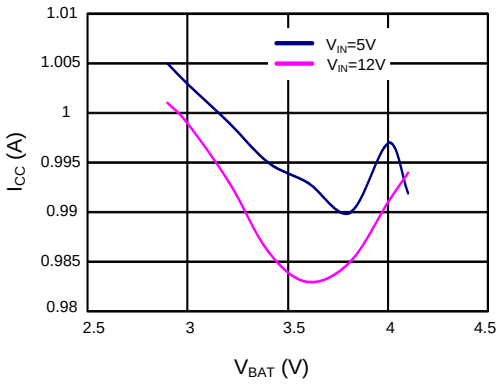
Efficiency (Buck CV Mode)



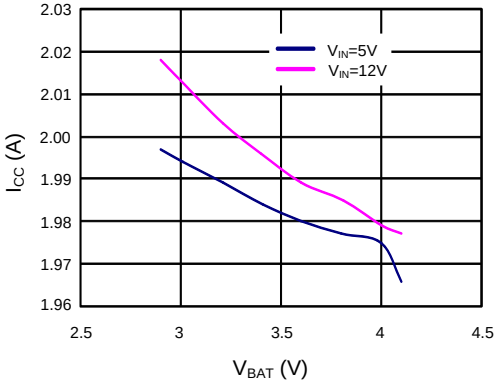
Efficiency (Boost CV Mode)



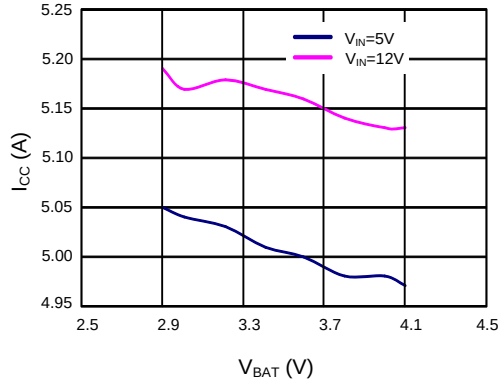
I_{CC} vs. V_{BAT} (I_{CC_SET}=1A)



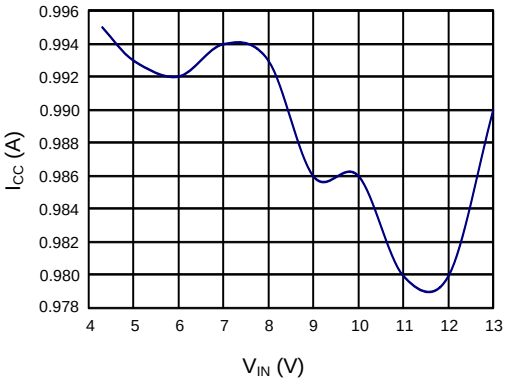
I_{CC} vs. V_{BAT} (I_{CC_SET}=2A)



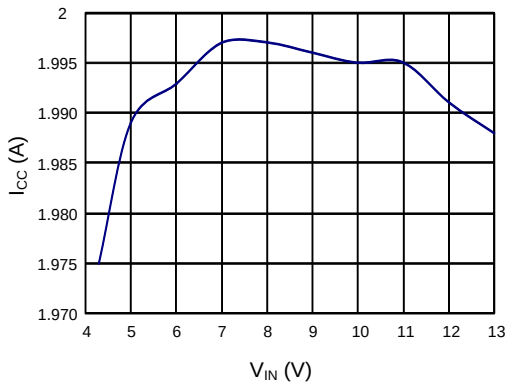
I_{CC} vs. V_{BAT} (I_{CC_SET}=5A)



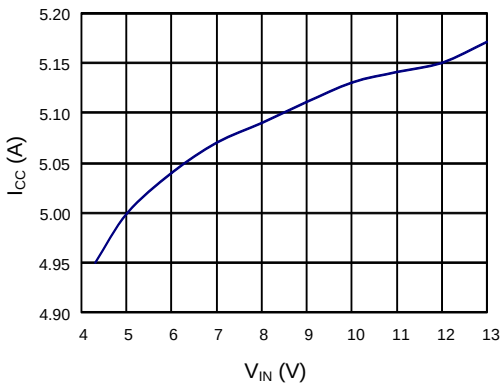
I_{CC} vs. V_{IN} (V_{BAT}=3.7V, I_{CC_SET}=1A)



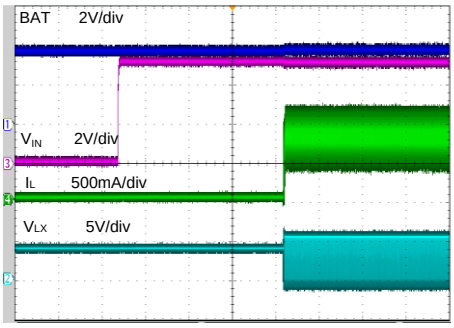
I_{CC} vs. V_{IN} (V_{BAT}=3.7V, I_{CC_SET}=2A)



I_{CC} vs. V_{IN} (V_{BAT}=3.7V, I_{CC_SET}=5A)

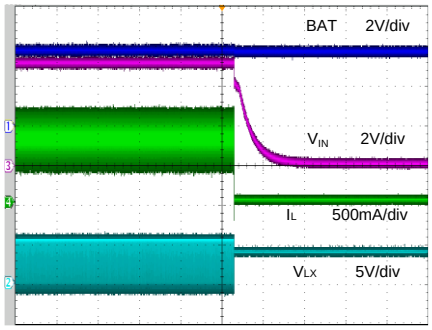


5V V_{IN} Power ON(Adapter)



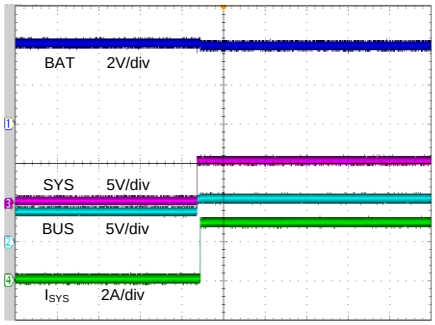
Time (200ms/div)

5V V_{IN} Power OFF(Adapter)



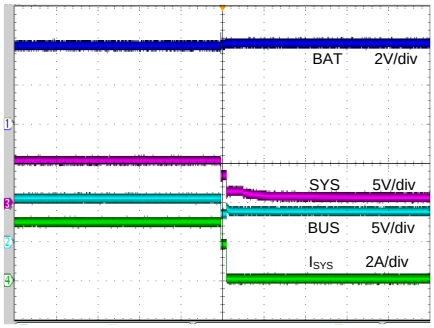
Time (200ms/div)

5V Boost Mode OTG ON by I^2C



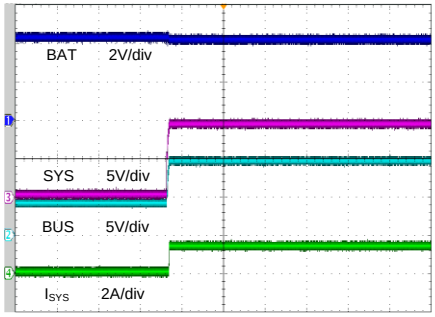
Time (200ms/div)

5V Boost Mode OTG OFF by I^2C



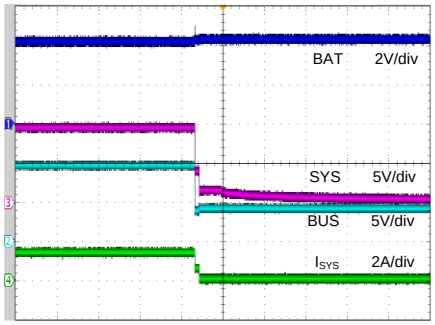
Time (200ms/div)

9V Boost Mode OTG ON by I²C



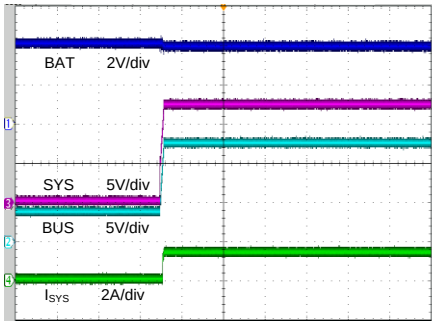
Time (200ms/div)

9V Boost Mode OTG OFF by I²C



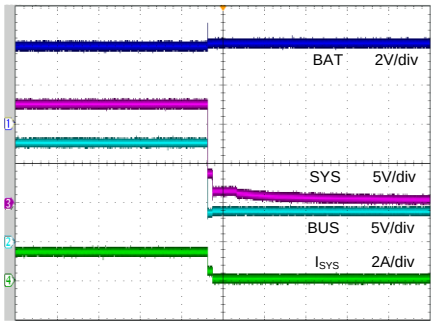
Time (200ms/div)

12V Boost Mode OTG ON by I²C



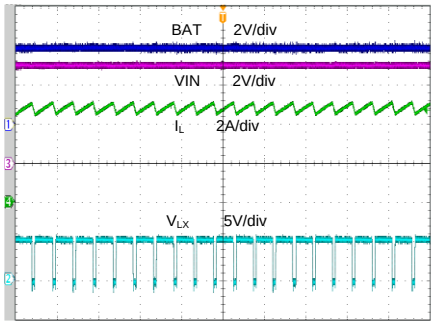
Time (200ms/div)

12V Boost Mode OTG OFF by I²C



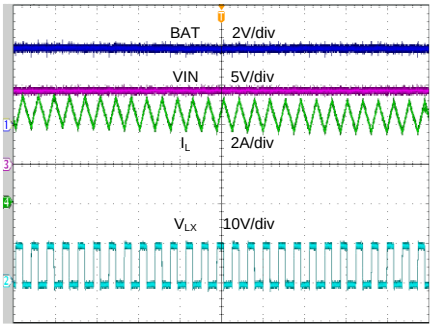
Time (200ms/div)

5V Buck Steady State



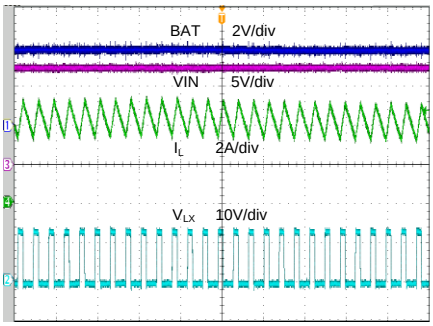
Time (4μs/div)

9V Buck Steady State



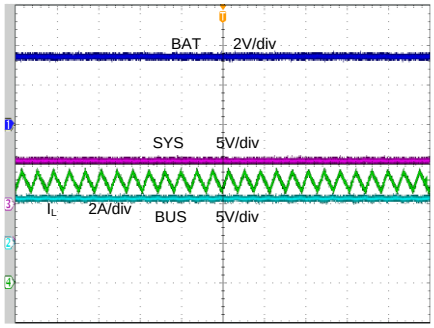
Time (4μs/div)

12V Buck Steady State



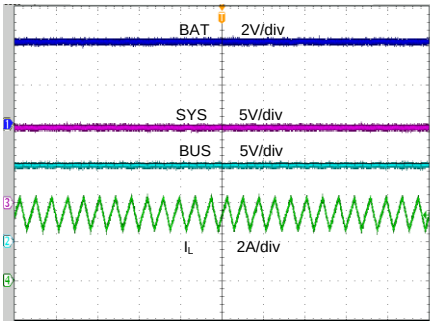
Time (4μs/div)

5V Boost Steady State



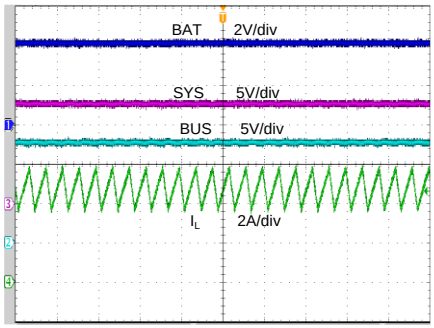
Time (4μs/div)

9V Boost Steady State



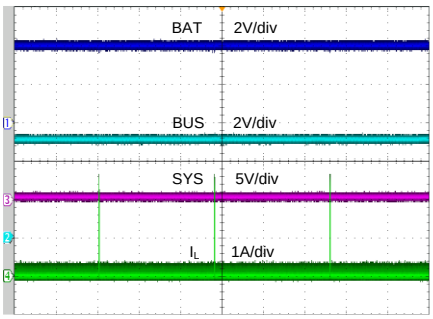
Time (4μs/div)

12V Boost Steady State



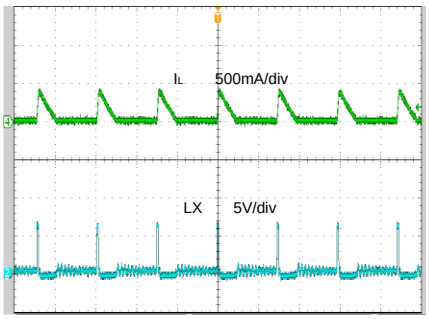
Time (4μs/div)

Boost SYS Short



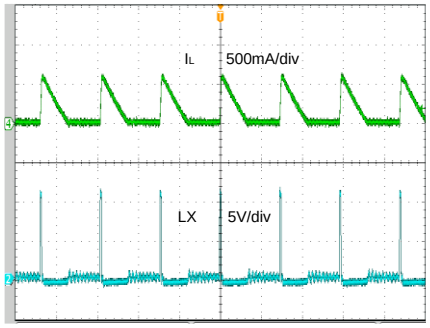
Time (200ms/div)

Battery Short in 5V Charging Mode



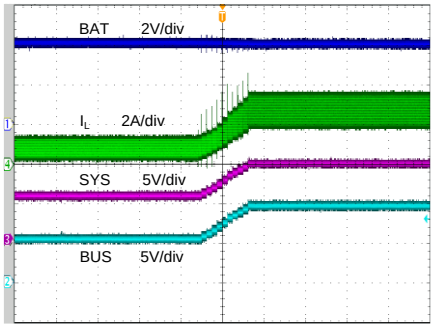
Time (4μs/div)

Battery Short in 12V Charging Mode



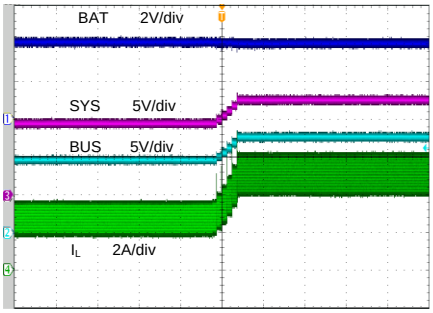
Time (4μs/div)

Boost 5V to 9V



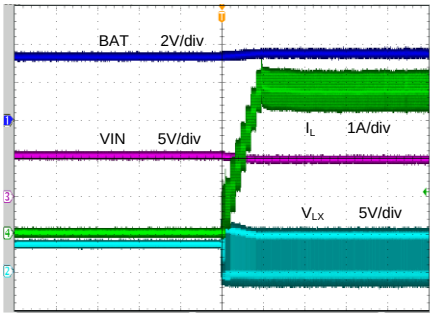
Time (10ms/div)

Boost 9V to 12V



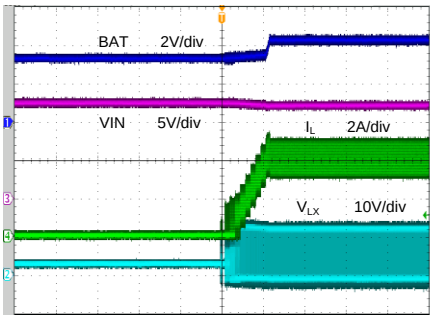
Time (10ms/div)

Inductor Current Soft Start in 5V Charging Mode



Time (10ms/div)

Inductor Current Soft Start in 12V Charging Mode



Time (10ms/div)

Operating Modes

Charging Mode: When an input voltage is present, the SY20754 operates in battery charging mode. The half-bridge operates in buck mode with I_{DPM}/V_{DPM}/CV/CC loop control.

Bypass Mode: When the input voltage is present and OTG mode is enabled, the SY20754 will operate in charging mode and supply power to SYS simultaneously.

Supplement Mode: In bypass mode, an increase in the SYS current load can cause the SY20754 control loop to reduce the battery charging current. When the PWM duty cycle of the buck converter reduces to zero and the system current continues to rise, the SY20754 will transition into supplement mode. In this mode, the half bridge of the SY20754 switches from buck to boost mode, supplying power to the SYS from both the input and the battery. The supplement mode is enabled using REG01[6].

Discharging Mode/Boost Mode: When the input voltage is absent, V_{BAT} will be higher than V_{BATDEP}, and the SY20754 operates in discharging mode/boost mode.

Automatic Input Power Supply Detection:

The SY20754 features automatic input power supply detection, employing an internal current source with a maximum capability of 10mA to discharge the IN pin for 100ms once the V_{IN} exceeds the UVLO threshold. If an external power supply is present, VIN should remain higher than the input voltage UVLO threshold even after the 100ms discharge period. When VIN is present and above the threshold, the REG00[0] register will be set to 1.

Input Power UP:

After the automatic input power supply detection is done and V_{IN} is present, the SY20754 will enable BC1.2 detection automatically. After BC1.2 detection, an INT(200µs low pulse) will be generated, and the input USB type will be recorded in REG05[1:0]. The MCU can monitor the USB type to set the appropriate values for the charging current, input current limit and input VDPM. After BC1.2 detection is completed, the SY20754 will start charging if no fault conditions are detected.

The SY20754 can set the DI+/DI- output voltage using the REG05[7:4] configuration bits and monitor the DI- input voltage using the REG06[3] bit.

After the input power up sequence, the input voltage range should be 4.2V-6.7V to ensure the normal operation. For higher input voltage operation, REG06[4] HV_V_{IN}_EN should be set to 1, and REG05[3:2] should be set to 9V or 12V to adjust the OVP and VDPM thresholds for SY20754.

Charging Mode Enable Control:

When V_{IN} is present, the charger can be enabled using the I^2C REG01 [7] bit.

INT Signal to MCU:

The SY20754 will generate an INT signal (200µs low pulse) when the following conditions are true:

1. Upstream D+/D- detection is complete.
2. Downstream D+/D- detection is complete.
3. Downstream D+/D- voltage level changes after the detection.

Programmable Input Current Dynamic Power Management:

The input current limit is programmable using the I^2C REG02[7:5] bits. When the input current reaches the I_{DPM} threshold, it will be limited to I_{DPM} by regulating the duty cycle of the buck converter.

Programmable Input Voltage Dynamic Power Management:

The input voltage limit is programmable using the REG03[7:5] bits. When the input voltage drops below V_{DPM}, the voltage control loop changes the duty cycle to maintain the target value.

REG00[1] will be set to 1 while the SY20754 operates in the VDPM state.

SYS Current Limit:

SYS current limit is programmed using the REG02[4:2] bits.

In Boost mode, when the SYS current exceeds the I_{SYS_Limit} programmed value, it will be limited to I_{SYS_Limit} by regulating the duty cycle of the Boost converter.

In Buck mode, when SYS current exceeds I_{SYS_Limit}, the LNFET operates in LDO mode and regulates SYS current to I_{SYS_Limit}.

Programmable Charging Current:

Charging current is programmed using the REG03[2:0] bits.

Programmable Termination Current:

Termination current can be set to 5% of I_{CC} and 10% of I_{CC} using the REG01[0] bit.

Programmable Charging Voltage:

Charging voltage is programmed using the REG03[4:3] bits.

OTG Light Load Indicator

When the SYS current is lower than the value programmed using REG02[1:0] bits (50mA or 200mA), the LLS open-drain will be pulled down to indicate an OTG light load. The OTG light load state can be determined reading the REG00[3] bit.

OTG Function:

When VIN is 5V, both the OTG pin and REG01[5] are active, and the OTG function is enabled to turn on LNFET. When VIN is 12V, the OTG mode can turn on LNFET using the following I²C configuration steps:

- **Step 1:** Pull OTG pin high and write a 1 to the OTG_Enable bit (REG01[5] = 1);
- **Step 2:** Write a "11" to the Input_Voltage_Set bits (REG05[3:2] = 11) ;
- **Step 3:** Write a 1 to High_VIN_EN (REG06[4] =1);
- **Step 4:** Write a 1 to High_VIN_EN (REG06[4] =0);
- **Step 5:** Write a 1 tp High_VIN_EN (REG06[4] =1);

When V_{IN} is absent, both the OTG pin and REG01[5] will be active, and the OTG function will be enabled to turn on the boost converter and LNFET.

Downstream Output Voltage Control:

In default mode, REG_State_Con REG06[5] is 0. In this mode, the REG06[7:6] bits are read-only. The voltage that downstream requests are recorded in REG06[7:6]. When REG_State_Con REG06[5] is set to 1 REG06[7:6] will be readable and writable. The SYS output voltage will change to the one set by REG06[7:6] in boost mode.

OTG Reset Condition:

REG01[5] will be reset to 0 (OTG is disabled) when one of the following faults happen:

1. BAT OVP
2. UTP/OTP
3. Thermal shutdown
4. BAT depletion

Charging Status Indication:

- **Charging-in-Process**: Pull and keep STAT pin low.
- **Charging Done**: High-Impedance.
- **Fault Mode**: Output toggles high/low with 10Hz frequency. The fault mode includes V_{IN} OVP, BAT OVP, BAT SCP, BAT UTP/OTP, and charging timeout conditions.

Connect an LED from VDD to the STAT pin.

- LED on indicates charging-in-process.
- LED off indicates charging is done.
- LED flashing indicates fault mode.

Charging status is available using the REG00[5:4] bits.

Protection Features:

Thermal Protection: Thermal protection for the battery is achieved through the NTC pin in charging and discharging modes. The basic scheme is shown in the application information. The device will return to normal operation when the temperature returns to normal range. The charging timer stops and maintains its value during thermal protection.

Short-Circuit Protection: The SY20754 is designed with BAT and SYS short-circuit protection features. When V_{SYS} is lower than $V_{SHORTSYS}$, the linear FET will modulate the current to be a sawtooth shape from 0A to 2.5A for short-circuit protection recovery. The SY20754 tries recovery for a period of 5ms every 0.6s. In charging mode, when V_{BAT} is lower than $V_{SHORTBT}$, the inductor current will fold back to a very low value.

Overvoltage Protection: When V_{BUS} or V_{BAT} are higher than the overvoltage protection thresholds, the half bridge will immediately stop boost or buck operation. It will return to normal operation when the monitored voltages return to normal level. The device shuts down when the input voltage goes above or below the OVP and UVLO threshold respectively. The SY20754 returns to normal operation when the V_{IN} returns to the normal range.

Battery Over Discharge Protection: While in OTG mode, when the battery voltage falls below the V_{BATDEP} threshold, the device turns off the boost and the LNFET. REG01[5] bit will be reset to 0 at the same time.

Timeout Protection: Timeout time is set by REG01[2:1]. When timeout occurs, the device stops the charge operation and latch off. Only recycling the input power source can reset the latch logic and restart the normal charging.

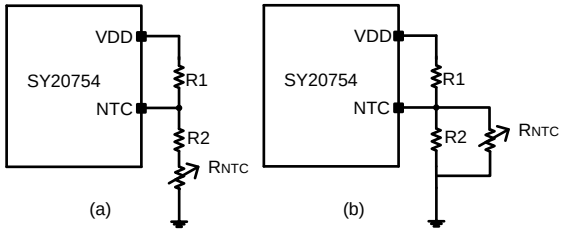
Application Information

The SY20754 is a highly integrated device designed for power bank applications. The following paragraphs provide information for the selection of the components shown in the schematic diagram, as required by the target application: input capacitor C_{IN}, BUS capacitor C_{BUS}, battery capacitor C_{BAT}, inductor L and the NTC resistors R1 and R2.

NTC Resistors:

The SY20754 monitors the battery temperature by measuring the VDD and NTC voltages. The device will trigger the UTP or OTP when the rate of K (K= V_{NTC}/V_{VDD}) reaches the UTP (K_{UT}) or OTP (K_{OT}) thresholds. The supported temperature sensing networks are shown below:

(Choose R1 and R2 to program the proper UTP and OTP points.)



The calculation steps of figure (a) are:

1. Define K_{UT}, K_{UT} =65%
2. Define K_{OT}, K_{OT} =35%
3. Assume that the resistance of the battery NTC thermistor is R_{UT} at the UTP threshold and R_{OT} at the OTP threshold.
4. Calculate R2:

$$R2 = \frac{K_{OT}(1-K_{UT})R_{UT} - K_{UT}(1-K_{OT})R_{OT}}{K_{UT}\text{-}K_{OT}}$$

5. Calculate R1:

$$R1 = (1/K_{OT} - 1)(R2 + R_{OT}) :$$

For the typical values (K_{UT} =65% and K_{OT}=35%) the equations can be simplified to:

$$R2 = 0.408R_{UT} - 1.408R_{OT}$$
$$R1 = 1.857(R2 + R_{OT})$$

Input Capacitor C_{IN}:

The input capacitor reduces the surge current drawn from the input rail and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent a high frequency switching current from passing to the input.

To minimize noise, a typical X7R or better grade ceramic capacitor should be placed close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and the IN/GND pins. A ceramic capacitor with a value above 20μF is recommended for most applications.

BUS Capacitor C_{BUS}:

1. Buck mode

The capacitor acts as the input capacitor for the buck converter. The input current ripple RMS value is larger than:

$$I_{CIN\_MIN} = I_{CHG}\sqrt{D(1-D)}$$

Where: I_{CHG} is the charge current and D is the duty cycle.

2. Boost mode

C_{BUS} is the output capacitor for the Boost converter. C_{BUS} reduces the BUS voltage ripple and ensures the stability of Boost. The output current ripple RMS value is :

$$I_{CBUS\_RMS} = \frac{\Delta I}{2\sqrt{3}}$$

Where: ΔI is the current ripple of inductor.

A ceramic capacitor with a value above 20μF is recommended for most applications.

Battery Capacitor C_{BAT}:

1. Buck mode

The battery capacitor acts as the output capacitor of the buck converter. C_{BAT} is selected to handle the output ripple voltage requirements. Both steady-state ripple and transient requirements must be considered when selecting this capacitor. For the best performance, it is recommended to use an X7R or a better-grade ceramic capacitor. The output voltage ripple is calculated as below:

$$V_{Ripple\_BAT\_Buck} = \frac{(1-D)\times V_{BAT}}{8C_{BAT}F_{SW}{}^2L}$$

Where: F_{SW} is the switching frequency and D is the duty-cycle.

2. Boost mode

C_{BAT} acts as the input capacitor for Boost converter operation. The input voltage ripple is calculated as below:

$$V_{Ripple\_BAT\_Boost} = \frac{D\times V_{BAT}}{8C_{BAT}F_{SW}{}^2L}$$

Where: F_{SW} is the switching frequency.

A ceramic capacitor with a value above 20μF is recommended for most applications.

Inductor L:

Inductor selection trades off between cost, size, and efficiency. A lower inductance value corresponds with smaller size but results in higher ripple currents, higher magnetic hysteretic losses, and higher output capacitances. A higher inductance value results in lower ripple current and smaller output filter capacitors but

results in higher inductor DC resistance (DCR) loss. An inductor must not saturate under the worst-case condition.

1. Buck mode

1) Choose the inductance to provide the desired ripple current. The ripple current is suggested to be approximately 40% of the average input current. The inductance is calculated as follows:

$$L = \frac{V_{BAT}(1 - V_{BAT}/V_{IN,MAX})}{F_{SW} \times I_{CHG,MAX} \times 40\%}$$

Where: F_{SW} is the switching frequency and $I_{CHG,MAX}$ is the maximum charge current.

The SY20754 is tolerant of different ripple current amplitudes. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{CHG,MAX} + \frac{V_{BAT}(1 - V_{BAT}/V_{IN,\ MAX})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirements.

2. Boost mode

1) Choose the inductance to provide the desired ripple current. The ripple current is suggested to be about 40% of the average input current. The inductance is calculated as follows:

$$L = \frac{V_{BAT}(1 - V_{BAT}/V_{BUS\_MAX})}{F_{SW} \times I_{DIS,MAX} \times 40\%}$$

Where: F_{SW} is the switching frequency, and $I_{DIS,MAX}$ is the maximum discharge current.
The SY20754 is tolerant of different ripple current amplitudes. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{DIS,MAX} + \frac{V_{BAT}(1 - V_{BAT}/V_{BUS\_MAX})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement.

The internal compensation circuits for the device limit the inductor choice. Using an inductor within the 0.68µH to 3.3µH range is recommended.

Schematic

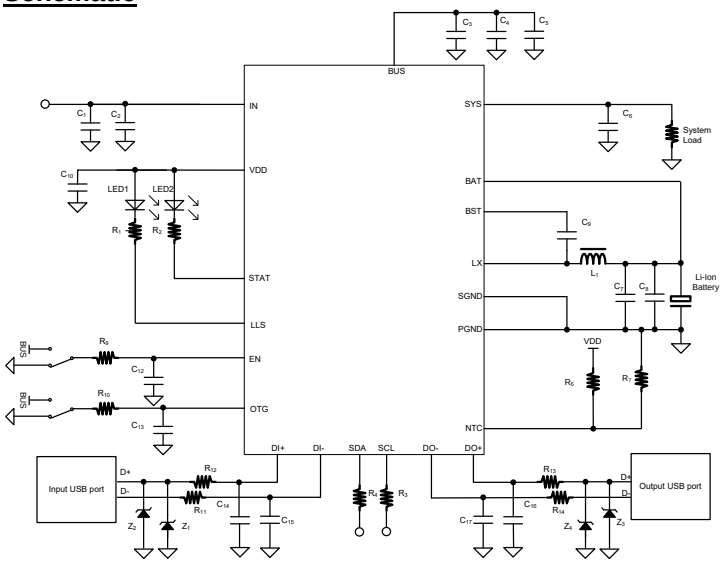


Figure 1. Schematic Diagram

BOM List

Designator	Description	Part Number	Manufacturer
U1	Charger	SY20754QCC	Silergy
L1	INDUCTOR 2.2uH 8.2A	SPM6530T-2R2M	TDK
C9	16V/100nF,0603,X7R	C1608X7R1C104K	TDK
C1,C2,C4,C5, C6, C7,C8	16V/10uF,1206,X7R	C3216X7R1C106K	TDK
C3, C10, C12, C13	16V/1uF,0603,X7R	C1608X7R1C105K	TDK
C14, C15, C16, C17	NULL		
LED1,LED2	Chip LED, 0603		
R6, R7, R9, R10	10kΩ, 0603, 1%		
R11, R12, R13, R14	0kΩ, 0603, 1%		
R3, R4	1kΩ, 0603, 1%		
Z1,Z2,Z3,Z4	6V Zener		

PCB Layout Guide:

For best performance of the SY20754, the following guidelines must be followed:

1) Enhance thermal and noise performance by maximizing the PCB copper area connected to the GND pin. If the board space allows, it is recommended to use a ground plane.
2) For the best efficiency and to minimize system noise, the following components should be placed close to the device: C_{IN}, C_{BUS}, C_{SYS}, L_B.
3) Place C_{IN} close to the IN and GND pins. Place C_{BUS} close to the BUS and GND pins. The loop area formed by C_{IN} and IN/GND pins , and C_{BUS} and GND must be as small as possible.
4) Minimize the PCB copper area connected to the LX pin to reduce EMI.
5) In high current applications, a RC snubber circuit should be placed between LX and GND to reduce EMI.

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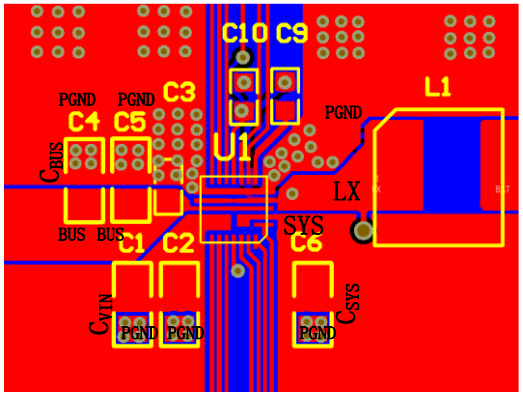


Figure 2. PCB Layout Suggestion

Register Description

I2C Register Map

The SY20754 supports seven battery-charger registers that can be accessed using either Write-Byte or Read-Byte commands, as summarized in Table 1. The register 04H is “read-only” and can be used to identify the SY20754.

Table 1. Battery Charger Register Summary

Register Address	Register Name	Read/Write	Default
00H	Status/Control Register	Read or Write	00H
01H	Control Register	Read or Write	84H
02H	Current Register	Read or Write	FBH
03H	Charge Register	Read or Write	89H
04H	Vendor/PN/Rev Register	Read	BxH
05H	Upstream USB type Register	Read or Write	xxH
06H	Downstream USB type Register	Read or Write	xxH

Table 2. Status/Control Register (00H)

Bit	Bit Name	R/W	Description
7	Reset	R/W	Write 1 to reset all the parameters, auto clear.
6	Boost	R	1: In Boost mode 0: Not in Boost mode
5:4	Status	R	00: Ready 01: Charge in progress 10: Charge done 11: Fault
3	BST_LLOAD	R	0: I_{SYS}> I_{SYS_L} 1: I_{SYS}< I_{SYS_L}, Boost mode light load.
2	BAT_DPL	R	0: V_{BAT}> V_{BATDEP} 1: V_{BAT}< V_{BATDEP}
1	VDPM_STATE	R	1: In VDPM state. 0: Not in VDPM state.
0	V_{IN}_PRES	R	1: V_{IN} present. 0: V_{IN} absent.

Table 3. Control Register (01H)

Bit	Bit Name	R/W	Description
7	Charge_Enable	R/W	0: Disable charger 1: Enable charger (default)
6	Supplement_Enable	R/w	0: Disable charge supplement mode (default) 1: Enable charge supplement mode

5	OTG_Enable	R/W	0: Disable OTG mode(default) 1: Enable OTG mode Set OTG pin high and OTG bit high to enable OTG function.
4	Reserved	NA	
3	V_{SYS} comp	R/W	System output voltage compensation in 5V mode. 1: 5.25V 0: 5.125V (default).
2:1	Timer	R/W	Charge timeout protection. 00: 5h 01: 10h 10: 20h (default) 11: Disable timer
0	ITERM_Current	R/W	0: 5%×ICC (default) 1:10%×ICC

Table 4. Current Register (02H)

Bit	Bit Name	R/W	Description
7:5	IDPM	R/W	Input current limit for 5/9/12V source. 001: 0.5A current limit 010: 1A current limit 011: 1.5A current limit 100: 2A current limit 101: 2.5A current limit 110: 3A current limit 111: Disable input current limit (default)
4:2	ISYS_Limit	R/W	SYS current limit for 5/9/12V SYS voltage. 000: 1/0.5/0.5A 001: 1.4/0.7/0.7A 010: 1.8/0.9/0.9A 011: 2.2/1.1/1.1A 100: 2.6/1.3/1.3A 101: 3/1.5/1.5A 110: 3.4/1.7/1.7A (default) 111: 3.4/1.7/1.7A
1	OTG_Lightload_EN	R/W	0: Disable OTG_Lightload detection 1: Enable OTG_Lightload detection (default)
0	OTG_Lightload	R/W	0:50mA 1:200mA (default)

Table 5. Voltage Register (03H)

Bit	Bit Name	R/W	Description
7:5	VDPM	R/W	V_{IN} threshold for input current limit. The offset is 0.35V based on 5V,0.55V based on 9V or 12V. For example, V_{DPM}=5x (1-bit[7:5])-0.35 for 5V_{IN}. The VDPM need to be clamped upon UVLO threshold. 000: 0 001: -1%

			010: -2% 011: -3% 100: -4% (default) 101: -5% 110: -6% 111: Disable VDPM
4:3	Charge_Voltage	R/W	1-cell charge voltage. 00: 4.10V charge voltage 01: 4.20V charge voltage (default) 10: 4.35V charge voltage 11: 4.4V charge voltage
2:0	Charge_Current	R/W	000: 0.5A charge current 001: 1A charge current (default) 010: 1.5A charge current 011: 2A charge current 100: 2.5A charge current 101: 3A charge current 110: 4A charge current 111: 5A charge current

Table 7. Vendor/PN/Rev Register (04H)

Bit	Bit Name	R/W	Description
7:5	Vendor_Code	R	101: Identify the supplied
4:3	PN	R	11: SY20754
2:0	Revision	R	001: Revision 1.0 010: Revision 1.1 011: Revision 1.2 ……

Table 8. Upstream USB type Register (05H)

Bit	Bit Name	R/W	Description
7:6	DI+_Output_Voltage	R/W	11: Floating 10: High 01: Low 00: 0V(default)
5:4	DI-_Output_Voltage	R/W	11: Floating 10: High 01: Low 00: 0V(default)
3:2	Input_Voltage_Set	R/W	11:12V 10: 9V 0x: 5V(Default)
1:0	Upstream USB type	R	11: Nonstandard adapter 10: DCP

Bit	Bit Name	R/W	Description
			01: CDP 00: SDP

Table 9. Downstream USB type Register (06H)

Bit	Bit Name	R/W	Description
7:6	Downstream_Voltage	R/W	11: 12V 10: 9V 0x: 5V(Default)
5	Reg_State_Con	R/W	0: REG06[7:6] read only, indicate the voltage that downstream requests(default). 1: REG06[7:6] both read and write, output voltage is the same as REG06[7:6]
4	High_V_{IN}_EN	R/W	0: Doesn't accept high input voltage(default) 1: Accepts high input voltage
3	DIM_STAT	R	0: DIM>0.325V 1: DIM<0.325V.
2:0	Reserved	NA	

I²C Interface

The SY20754 uses an I²C-compatible interface for flexible charging parameter programming and instantaneous device status reporting. Only two I2C lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered controllers or peripherals when performing data transfers. A controller is the device that initiates a data transfer on the I2C bus and generates the clock signals to permit that transfer. At that time, any device addressed on the bus is considered a peripheral.

SY20754 operates as a peripheral device with address 6AH, receiving commands from the host controller, such as a microcontroller or a digital signal processor. (The device address should be left shift 1 bit for write and read operation; the new device address after left shift 1 bit is D4H). The I²C interface supports standard mode (up to 100kbits) and fast mode (up to 400kbits).

Both SDA and SCL are bi-directional lines connected to the positive supply voltage via a current source or a pull-up resistor. When the BUS is free, both lines are HIGH. The SDA and SCL pins are open-drain.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

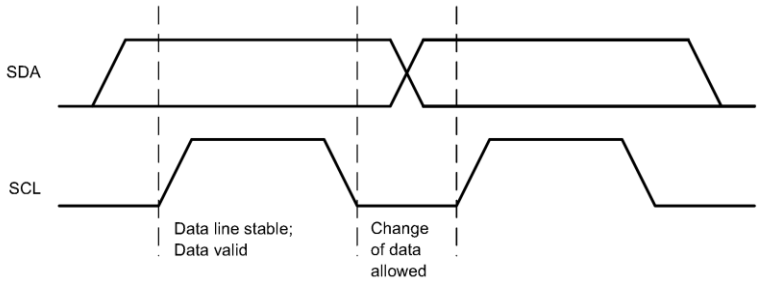


Figure 2. Bit Transfer on the I²C BUS

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line, while SCL is HIGH, defines a START condition. A LOW to HIGH transition on the SDA line, when the SCL is HIGH, defines a STOP condition.

START and STOP conditions are always generated by the controller. The BUS is considered busy after the START condition, and free after the STOP condition.

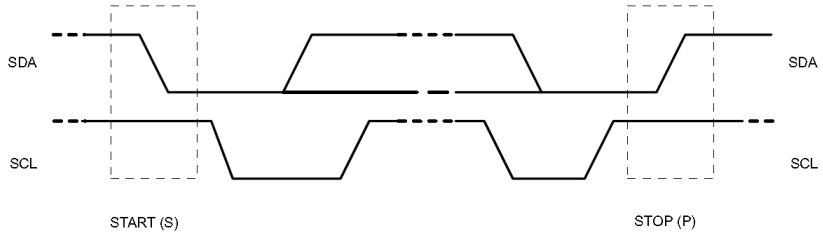


Figure 3. START and STOP Conditions

Byte Format

Every byte on the SDA line must be 8-bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an 'Acknowledge' bit. Data is transferred with the most significant bit (MSB) first. If a peripheral device cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the controller into a wait state (clock stretching). Data transfers continue when the peripheral is ready for another byte of data and releases the clock line SCL.

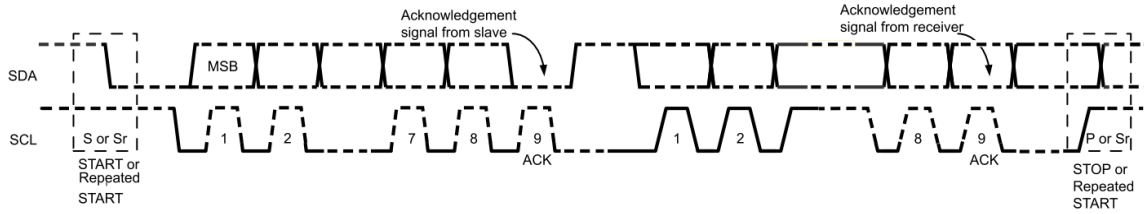


Figure 4. Data Transfer on the I²C BUS

Acknowledge (ACK) and Not Acknowledge (NACK)

The 'Acknowledge' takes place after every byte. The acknowledge bit lets the receiver signal to the transmitter that the byte was successfully received, and another byte may be sent. All clock pulses, including the 'Acknowledge' 9th clock pulse, are generated by the controller.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the 'Not Acknowledge' signal. The controller can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Peripheral Address and Data Direction Bit

After the START, a peripheral address is sent. This address is 7 bits long, followed by the eighth bit as a data direction bit (bit R/W). A "0" indicates a transmission (WRITE) and a "1" indicates a request for data (READ).

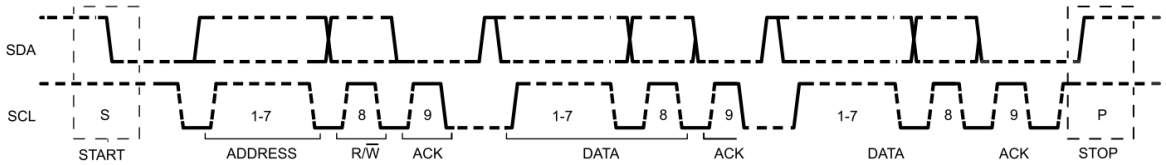


Figure 5. Complete Data Transfer

Single Read and Write

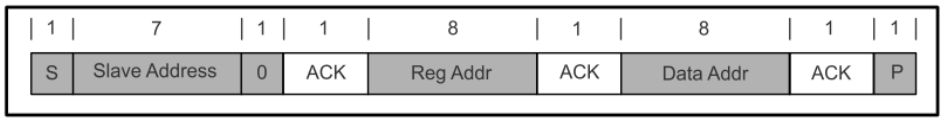


Figure 6. Single Write

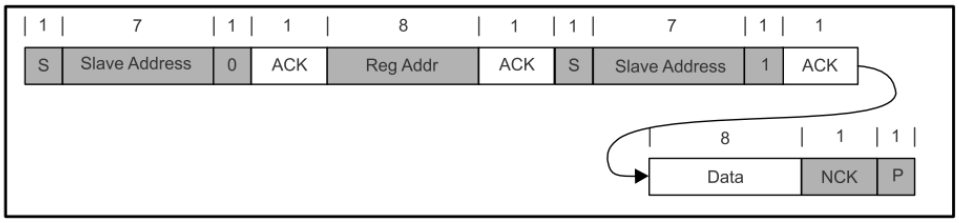
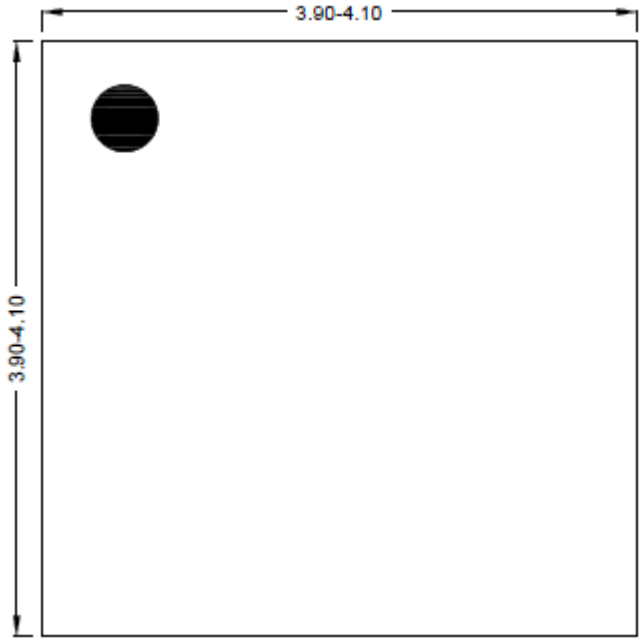


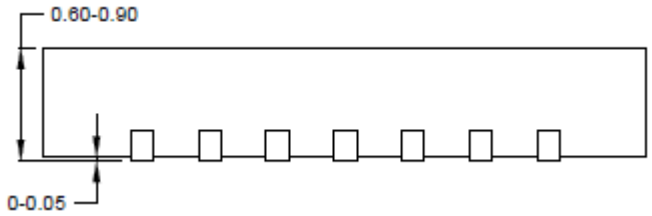
Figure 7. Single Read

If the register address is not defined, the peripheral device will send back NACK and return to the idle state.

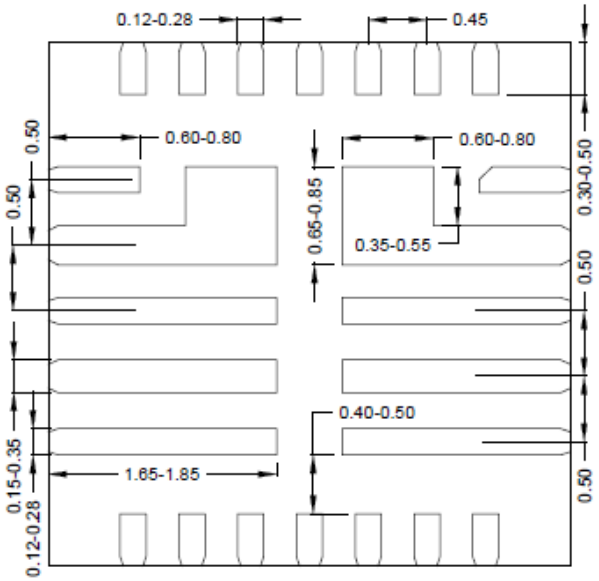
QFN4x4-24 Package Outline Drawing



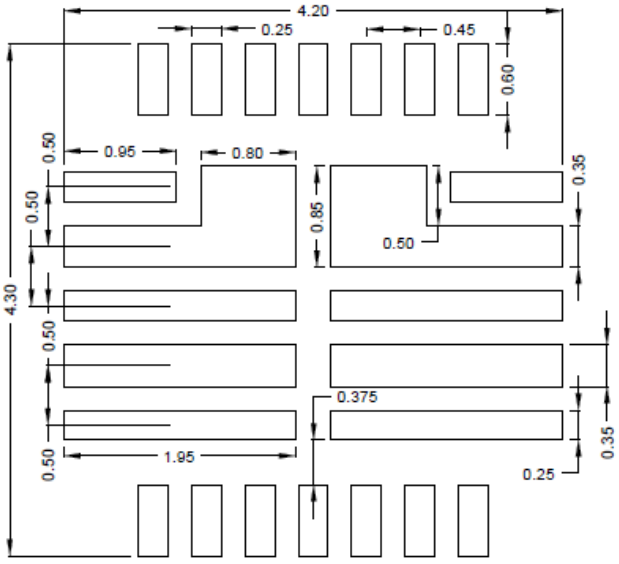
Top View



Side View



Bottom View

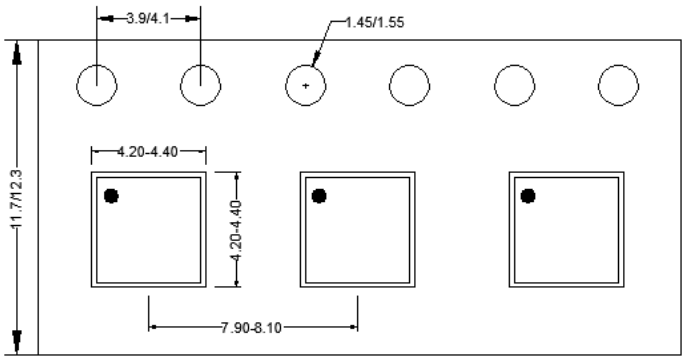


Recommended PCB Layout
(Reference Only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

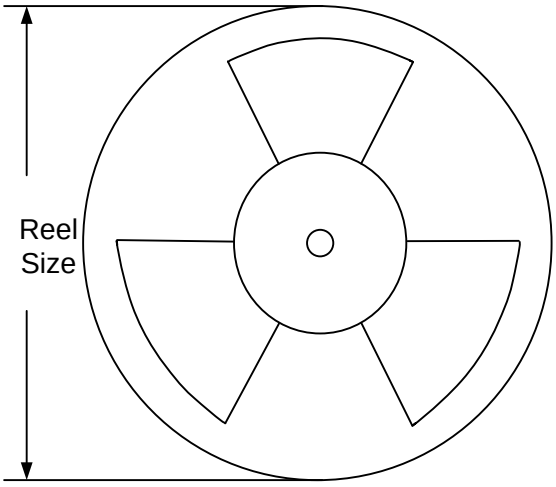
Taping & Reel Specification

QFN4x4 Taping Orientation



Feeding direction ⟶

Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
QFN4x4	12	8	13"	400	400	5000

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