SY20775B

Sink and Source DDR Termination Regulator

General Description

The SY20775B is a sink and source double data rate (DDR) regulator designed for use in low input voltage, low-cost, low-noise systems where space is a key consideration. It maintains a fast transient response and require a minimum ceramic output capacitance of only 10uF and all power requirement for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4 VTT bus termination. Additionally, The VO(VTT) current capability is ±2A peak. The device supports all of the DDR power states, putting VO(VTT) to High-Z in S3 state (suspend to RAM) and discharging VO(VTT) and VOSNS in S4 or S5 state (suspend to disk).

The SY20775B is available in the 10-Pin, DFN2mm×2mm thermal pad package, and it's rated both Green and Pb-free. It's specified from -40°C to 125°C.

Features

- Input Voltage: Supports 2.5V Rail and 3.3V Rail
- VLDOIN Voltage Range: 1.1V to 3.5V
- 2A Peak Sink and Source Current
- Sink and Source Termination Regulator Includes Droop Compensation
- Requires Minimum Ceramic Output Capacitance of 10uF for memory
- Support High-Z in S3 and Soft-Stop in S4 and S5 with S3 and S5 inputs
- Remote Sensing (VOSNS)
- ±10mA Buffered Reference (REFOUT)
- REFIN/2 ±1% Accuracy (REFOUT)
- Built-in Soft Start, UVLO, and OCL
- Thermal Shutdown
- Supports DDR, DDR2, DDR3, DDR3L, Low Power DDR3, DDR4 VTT Applications
- Packages: 10-Pin, DFN2mm×2mm With Thermal Pad

Application

- Memory Termination Regulator for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4
- Notebooks, Desktops, and Servers
- Base Stations

Typical Applications

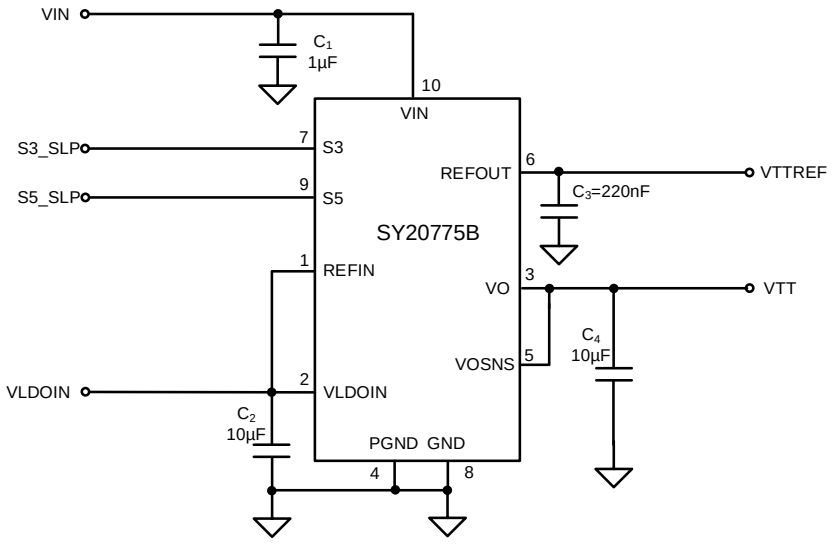


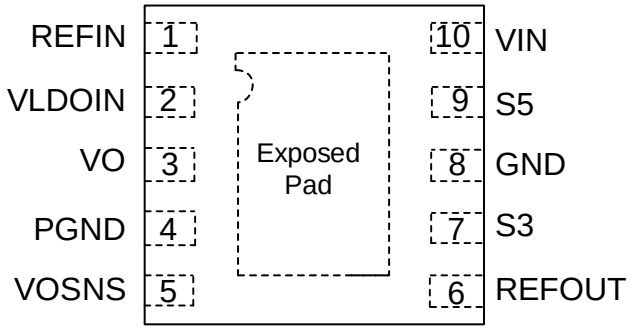
Figure 1. Schematic Diagram

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY20775BTDD	DFN2×2-10 RoHS Compliant and Halogen Free	**f5*xyz***

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Name	Pin Name	Pin Description
S3	7	S3 signal input
S5	9	S5 signal input
GND	8	Signal ground pin
PGND	4	Power ground pin for the LDO
REFIN	1	VLDOIN sense input, reference input for REFOUT
REFOUT	6	REFOUT buffered reference output. Need to connect 0.22μF or greater MLCC for stability
VIN	10	Input supply pin. A large bulk capacitance should be placed close to this pin to ensure that the input supply does not sag below the minimum VIN. A ceramic decoupling capacitor with a value between 1uF and 4.7μF is required.
VLDOIN	2	Supply voltage for the LDO
VO	3	Power output pin for the LDO, need to connect 10μF or greater MLCC for stability
VOSNS	5	Voltage sense input for the LDO. Connect to positive terminal of the output capacitor or load
Exposed Pad	/	The exposed pad should be connected to ground plane for better thermal performance

Block Diagram

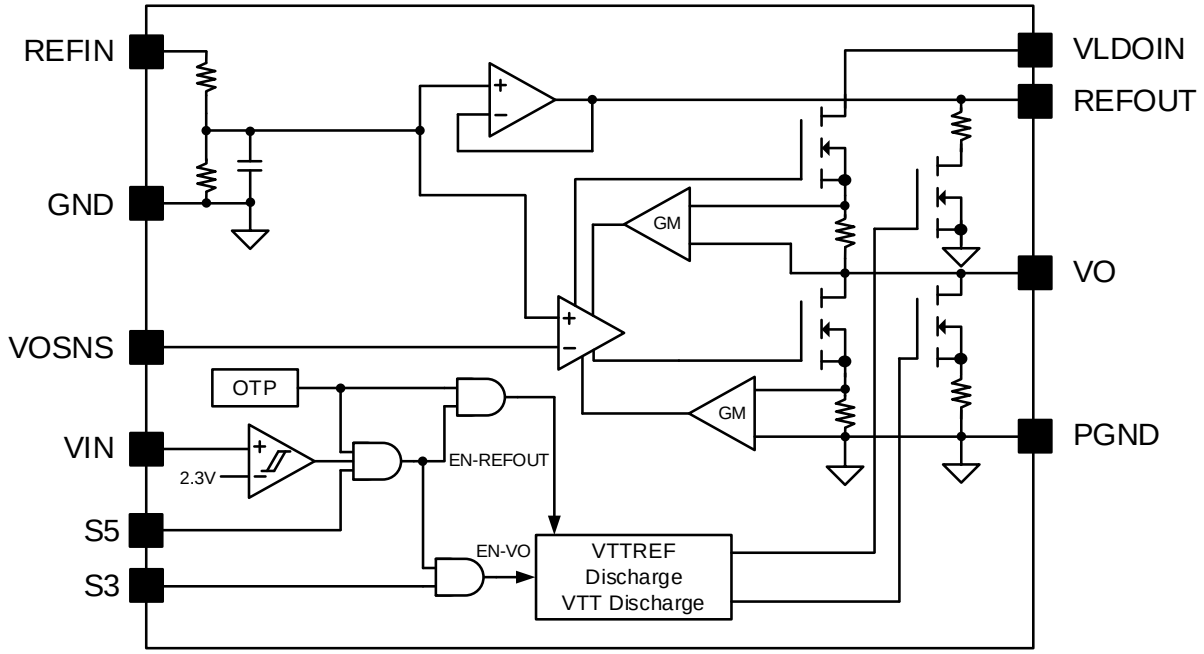


Figure 2. Block Diagram

Absolute Maximum Ratings (1)	Min	Max	Unit
VIN, REFIN, REFOUT, VO, VLDOIN , VOSNS	-0.3	3.6	V
S3, S5	-0.3	7	
GND, PGND	-0.3	0.3	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10sec.)		260	
Storage Temperature	-65	150	

Thermal Information (2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	50	°C/W
θ_{JC} Junction-to-case Thermal Resistance	45	
P_D Power Dissipation T_A=25°C	2	W

Recommended Operating Conditions (3)	Min	Max	Unit
VIN	2.375	3.5	V
S3, S5	-0.1	6.5	
REFIN, REFOUT, VO, VLDOIN, VOSNS	-0.1	3.5	
PGND	-0.1	0.1	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{VIN}=3.3V, V_{S3}=V_{S5}=3V, V_{LDOIN}= V_{REFIN} =1.8V, C_{IN}=1μF, C_{OUT}=10μF, T_J=-40°C to 125°C, typical values are T_J=25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SUPPLY CURRENT						
VIN Supply Current, in S0	$I_{IN(S0)}$	T_A=25 °C, No load, V_{S3}=V_{S5}=3V, V_{REFIN}=1.8V		0.7	1	mA
VIN Supply Current, in S3	$I_{IN(S3)}$	T_A=25 °C, No load, V_{S3}=0V, V_{S5}=3V, V_{REFIN}=1.8V		200	400	μA
VIN Shutdown Current, in S4 and S5	I_{VINSDN}	T_A=25 °C, No load, V_{S3}=V_{S5}=0V, V_{REFIN}=1.8V		2	5	μA
VLDOIN Supply Current, in S0	$I_{VLDOIN(S0)}$	T_A=25 °C, No load, V_{S3}=V_{S5}=3V, V_{VLDOIN}=1.8V		1	5	μA
VLDOIN Supply Current, in S3	$I_{VLDOIN(S3)}$	T_A=25 °C, No load, V_{S3}=0V, V_{S5}=3V, V_{VLDOIN}=1.8V		0.1	5	μA
VLDOIN Shutdown Current, in S4 and S5	$I_{VLDOINSDN}$	T_A=25 °C, No load, V_{S3}=V_{S5}=0V, V_{LDOIN}=1.8V			5	μA
VO OUTPUT						
Output Voltage	V_{VO}			V_{REFIN}/2		V
Output DC Voltage of VO	V_{VOSNS}	V_{REFIN} = 2.5 V(DDR1), I_{VO} = 0 A		1.25		V
			-15		15	mV
		V_{REFIN} = 1.8 V(DDR2), I_{VO} = 0 A		0.9		V
			-15		15	mV
		V_{REFIN} = 1.5 V(DDR3), I_{VO} = 0 A		0.75		V
			-15		15	mV
		V_{REFIN} = 1.35 V(DDR3L), I_{VO} = 0 A		0.675		V
			-15		15	mV
		V_{REFIN} = 1.2 V(DDR4), I_{VO} = 0 A		0.6		V
			-15		15	mV
Output Voltage Tolerance to V_{REFIN}/2	V_{VOTOL}	T_A=25 °C, -2 A< I_{VO} < 2 A	-25		25	mV
VO Source Current Limit	I_{VOSRCL}	V_{REFIN} = 1.8V, V_{VO} = V_{VOSNS} = 0.7V	2			A
VO Sink Current Limit	I_{VOSNCL}	V_{REFIN} = 1.8V, V_{VO} = V_{VOSNS} = 1.1V	2			A
Leakage Current	I_{VOLK}	T_A=25 °C, V_{S3}=0V, V_{S5}=3V, V_{VO}=V_{REFOUT} (Note 4)			5	μA
OUT Shutdown Discharge Resistance	R_{VODIS}	T_A=25 °C, V_{S3}=V_{S5}=V_{REFIN}=0V		14	25	Ω
REFIN INPUT						
REFIN Input Current	I_{REFIN}	V_{REFIN}=1.8V, V_{S3}=V_{S5} =3V		30		μA
REFOUT OUTPUT						
REFOUT Voltage	V_{REFOUT}			V_{REFIN}/2		V
REFOUT Voltage Tolerance to V_{REFIN}/2	$V_{REFOUTTOL}$	T_A=25 °C, -10mA< I_{REFOUT} < 10mA, 1.2V≤V_{REFIN} ≤1.8V	-12		12	mV
REFOUT Source Current Limit	$V_{REFOUTSRCL}$	V_{REFIN} = 1.8V, V_{REFOUT} = 0 V	10			mA
REFOUT Sink Current Limit	$V_{REFOUTSNCL}$	V_{REFIN} = 0V, V_{REFOUT} = 1.8 V	10			mA
REFOUT Shutdown Discharge Resistance	$R_{REFOUTDIS}$	V_{S3}=V_{S5}=V_{REFIN}=0V		90		Ω
UVLO/LOGIC THRESHOLD						
UVLO Threshold	$V_{VINUVVIN}$	Wake up	2.2	2.3	2.375	V
		Hysteresis		50		mV
S3 and S5 High-Level Input	V_{ENIH}	Enable	1.2			V

Electrical Characteristics (V_{VIN}=3.3V, V_{S3}=V_{S5}=3V, V_{LDOIN}= V_{REFIN} =1.8V, C_{IN}=1μF, C_{OUT}=10μF, T_J=-40°C to 125°C, typical values are T_J=25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Voltage						
S3 and S5 Low-Level Input Voltage	V_{ENIL}	Enable			0.3	
S3 and S5 Hysteresis Voltage	V_{ENYST}	Enable		0.1		
S3 and S5 Input Leakage Current	I_{ENLEAK}	Enable	-1		1	μA
OVER TEMPERATURE PROTECTION						
Thermal Shutdown Threshold	T_{SD}	(Note 4)		150		°C
Thermal Shutdown Hysteresis	T_{HYS}	(Note 4)		20		°C

Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

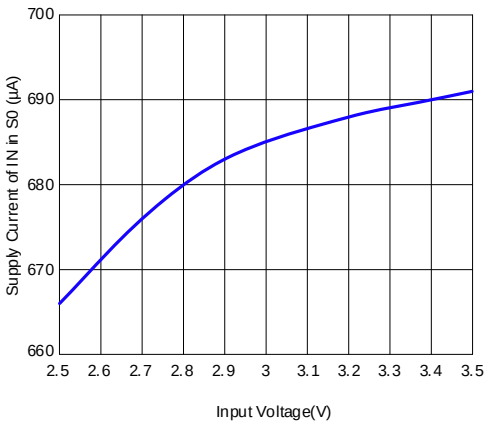
Note 2: θ_{JA} is simulated in the natural convection at T_A = 25°C on Silergy EVB test board.

Note 3: The device is not guaranteed to function outside its operating conditions.

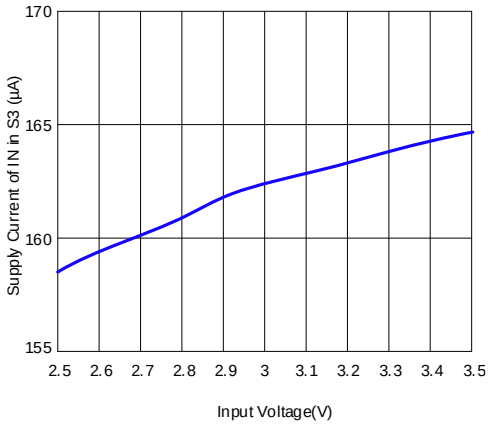
Note 4: Guaranteed by design, not subject to test.

Typical Operating Characteristics

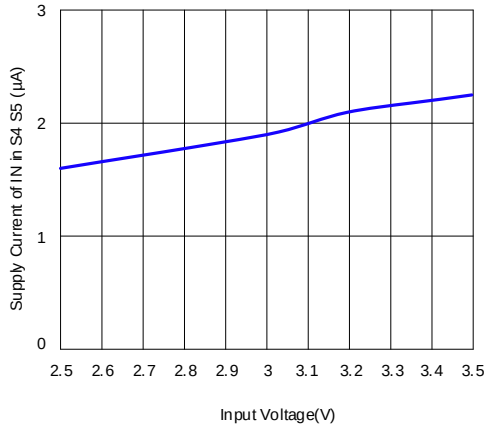
Supply Current of VIN in S0 vs. Input Voltage
(V_{S3}=V_{S5}=3V, V_{REFIN}=1.8V)



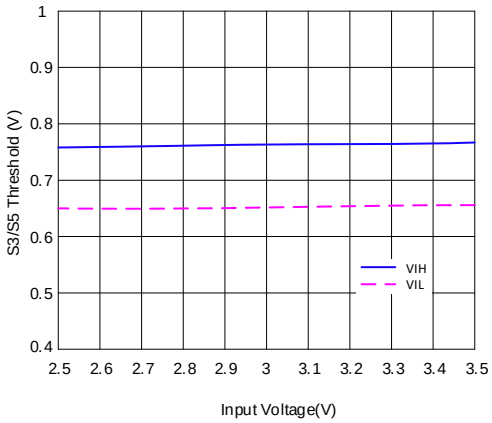
Supply Current of VIN in S3 vs. Input Voltage
(V_{S3}=0V, V_{S5}=3V, V_{REFIN}=1.8V)



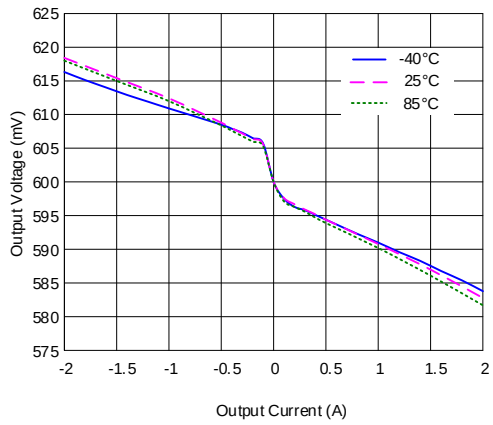
Supply Current of VIN in S4 S5 vs. Input Voltage
(V_{S3}=V_{S5}=0V, V_{REFIN}=1.8V)



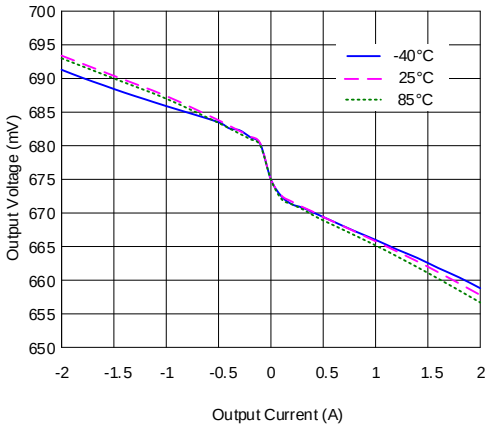
S3/S5 Threshold vs. Input Voltage
(V_{REFIN}=1.8V)



VO Load Regulation (0.6 V)
(V_{IN}=3.3V, V_{REFIN}=1.2V)

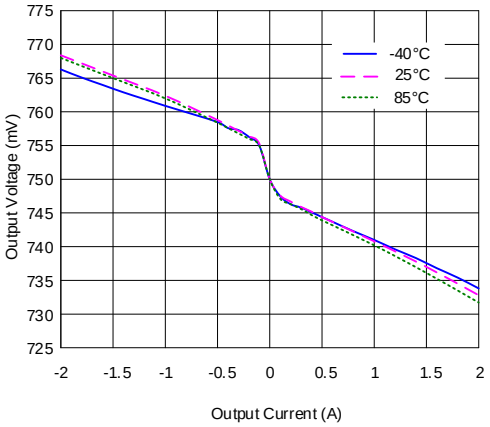


VO Load Regulation (0.675 V)
(V_{IN}=3.3V, V_{REFIN}=1.35V)



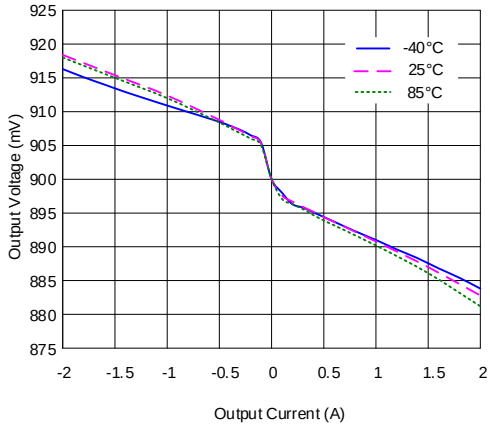
VO Load Regulation (0.75 V)

(V_{IN}=3.3V, V_{REFIN}=1.5V)



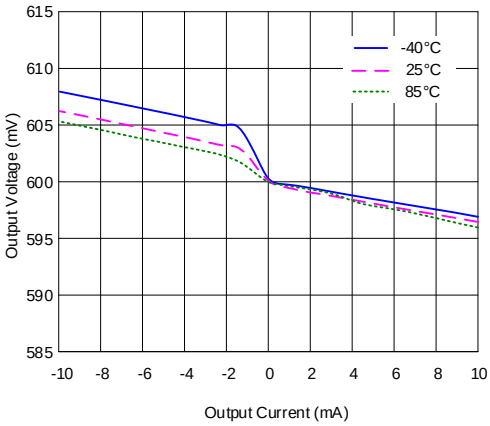
VO Load Regulation (0.9 V)

(V_{IN}=3.3V, V_{REFIN}=1.8V)



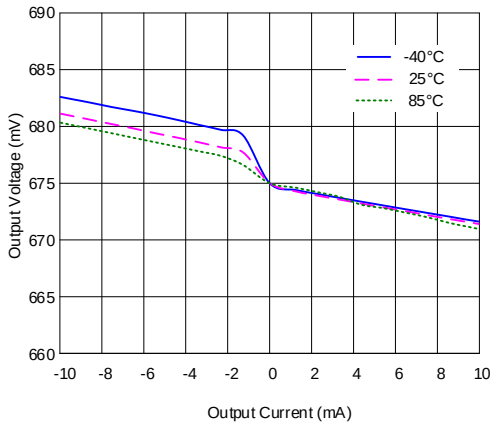
REFOUT Load Regulation (0.6 V)

(V_{IN}=3.3V, V_{REFIN}=1.2V)



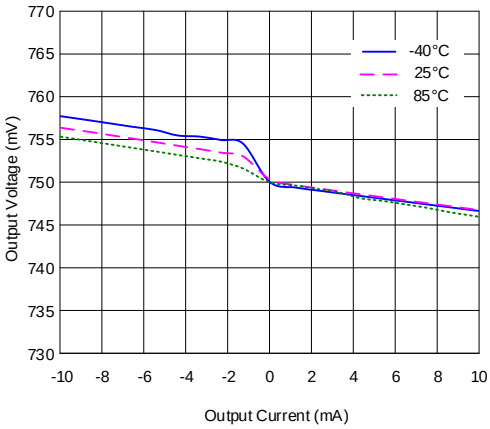
REFOUT Load Regulation (0.675 V)

(V_{IN}=3.3V, V_{REFIN}=1.35V)



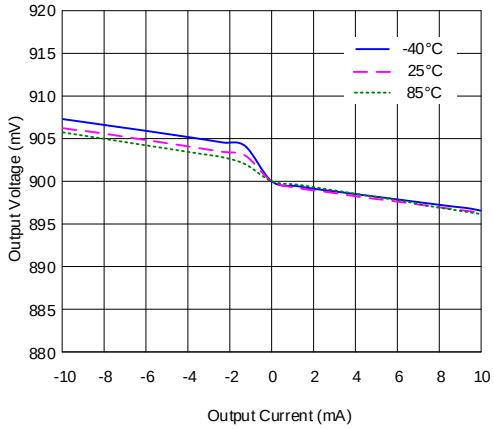
REFOUT Load Regulation (0.75 V)

(V_{IN}=3.3V, V_{REFIN}=1.5V)



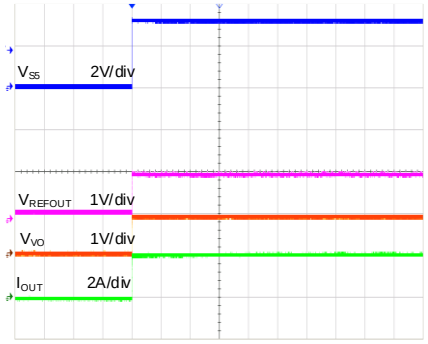
REFOUT Load Regulation (0.9 V)

(V_{IN}=3.3V, V_{REFIN}=1.8V)



Startup from S5

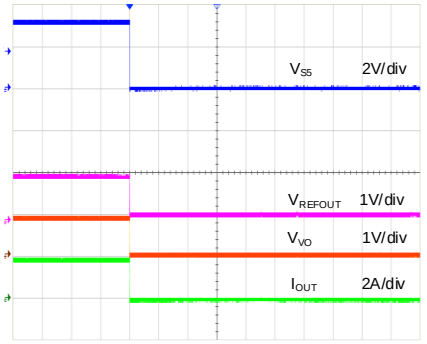
(V_{IN}=V_{S3}=3.3V, V_{REFIN}=1.8V, C_{VO}=10μF, S5 ON, 0.45Ω Load)



Time(10ms/div)

Shutdown from S5

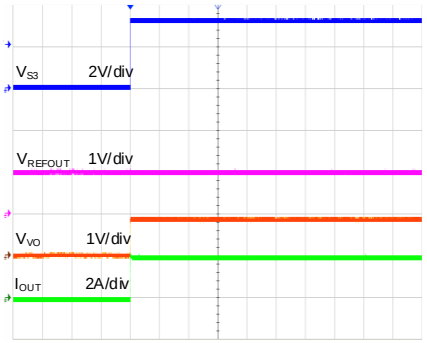
(V_{IN}=V_{S3}=3.3V, V_{REFIN}=1.8V, C_{VO}=10μF, S5 OFF, 0.45Ω Load)



Time(10ms/div)

Startup from S3

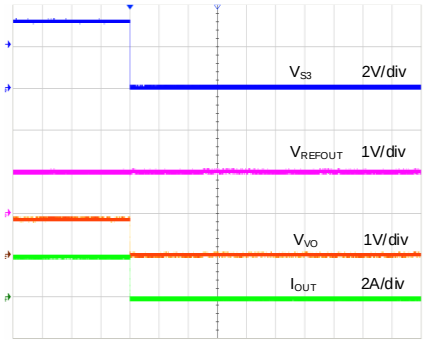
(V_{IN}=V_{S5}=3.3V, V_{REFIN}=1.8V, C_{VO}=10μF, S3 ON, 0.45Ω Load)



Time(10ms/div)

Shutdown from S3

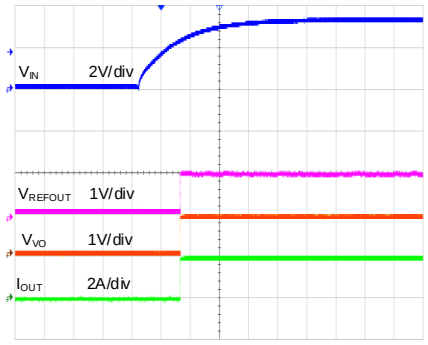
(V_{IN}=V_{S5}=3.3V, V_{REFIN}=1.8V, C_{VO}=10μF, S3 OFF, 0.45Ω Load)



Time(10ms/div)

Startup from V_{IN}

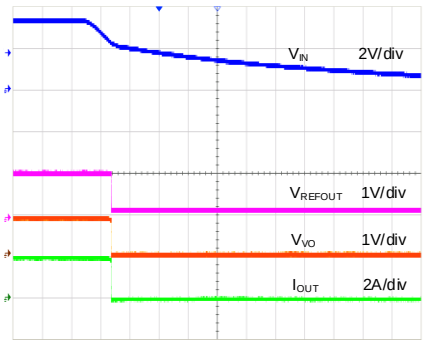
(V_{S3}=V_{S5}=3.3V, V_{REFIN}=1.8V, C_{VO}=10μF, V_{IN}=0V→3V, 0.45Ω Load)



Time(20ms/div)

Shutdown from V_{IN}

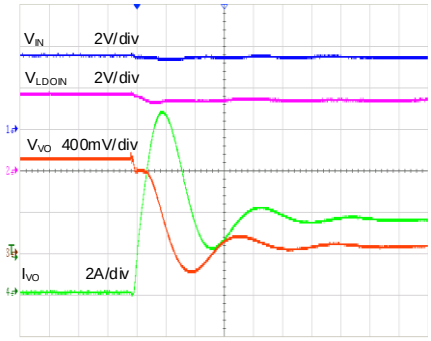
(V_{S3}=V_{S5}=3.3V, V_{REFIN}=1.8V, C_{VO}=10μF, V_{IN}=3V→0V, 0.45Ω Load)



Time(20ms/div)

Short Circuit Response

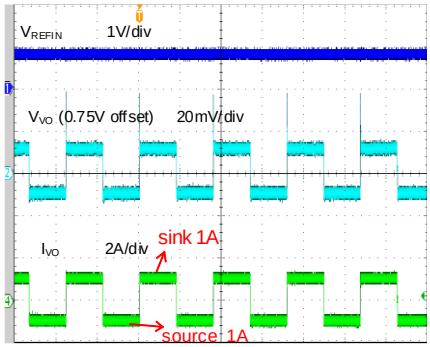
(V_{IN}=V_{LDOIN}=3.5V, V_{REFIN}=1.8V)



Time(2μs/div)

VO Load Transient Response (0.75 V)

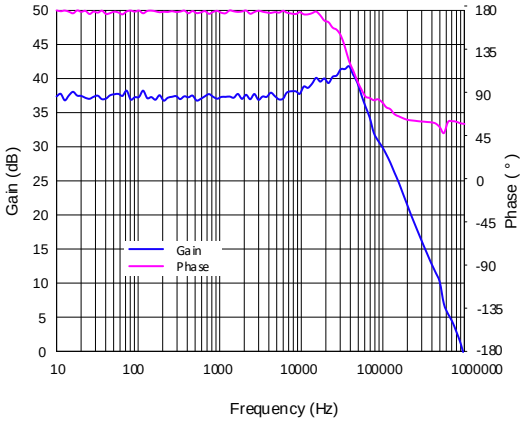
(V_{IN}=3.3V, V_{REFIN}=1.5V)



Time(4ms/div)

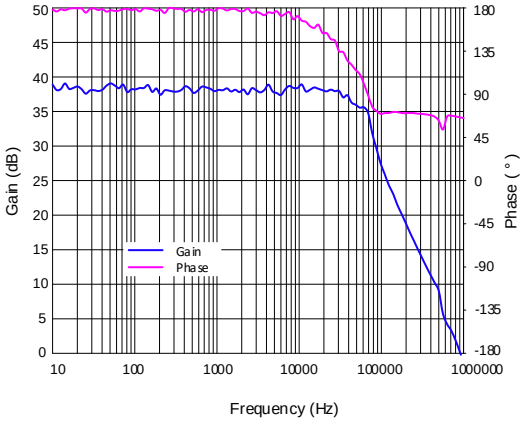
Bode Plot of VO Sink 1A

(V_{IN}=3.3V, V_{REFIN}=1.5V, sink 1A load)



Bode Plot of VO Source 1A

(V_{IN}=3.3V, V_{REFIN}=1.5V, source 1A load)



Application Information

1. OVERVIEW

The SY20775B is a sink or source tracking termination regulator specifically designed for low input voltage, low cost, and low external component count systems where space is a key application parameter. The SY20775B integrates a high-performance, low-dropout (LDO) linear regulator that has ultimate fast response to track ½ REFIN within 25 mV at all conditions, and its current capability is 2 A for both sink and source directions. A 10µF (or greater) ceramic capacitor(s) need to be attached close to the VO terminal for stable operation. A grade of X5R or better is recommended. To achieve tight regulation with minimum effect of trace resistance, the remote sensing terminal, VOSNS, should be connected to the positive terminal of the output capacitor(s) as a separate trace from the high current path from the VO pin.

The device has a dedicated pin, VLDOIN, for VO power supply to minimize the LDO power dissipation on user application.

2. REFOUT Output Function

The REFOUT pin includes 10 mA of sink or source current capability, and tracks ½ of REFIN with ±1%
accuracy. A 0.22µF ceramic capacitor needs to be attached close to the REFOUT terminal for stable operation; X5R or better grade is recommended.

3. VIN Under Voltage Lockout Protection

The SY20775B input voltage (VIN) includes under voltage lockout protection (UVLO). When the VIN pin voltage is lower than UVLO threshold voltage, VO and REFOUT are shut off. This is non-latch protection.

4. Over Temperature Protection

This device features internal temperature monitoring. If the temperature exceeds the threshold value, REFOUT is shut off. This is a non-latch protection.

5. Power State Control

The SY20775B has two input pins, S3 and S5, to provide simple control of the power state. Table 1 describes S3 and S5 terminal logic state and corresponding state of REFOUT and VO outputs. VO is turn-off and placed to high impedance (High-Z) state in S3. The VO output is floated and does not sink or source current in this state. When both S5 and S3 pins are LOW, the power state is set to S4 and S5. In S4 and S5 state, all the outputs are turn-off and discharged to GND.

Table1. S3 and S5 Control Table

STATE	S3	S5	REFOUT	VO(VTT)
S0	HI	HI	ON	ON
S4 and S5	HI	LO	OFF (Discharge)	OFF(Discharge)
S3	LO	HI	ON	OFF(High-Z)
S4 and S5	LO	LO	OFF (Discharge)	OFF(Discharge)

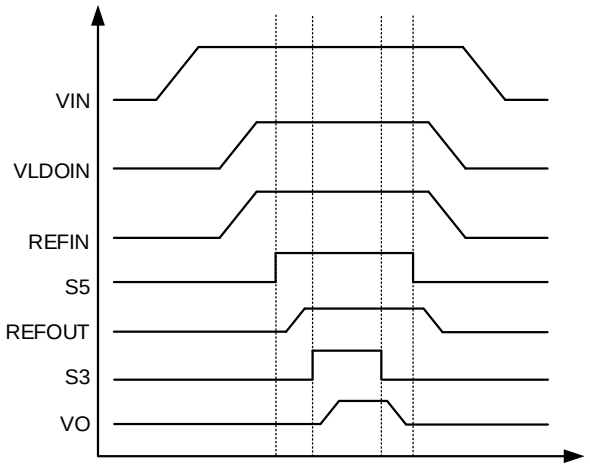


Figure 3. Typical Timing Diagram

6. Supply Filter Capacitor

Add a ceramic capacitor, with a value between 1µF and 4.7µF, placed close to the VIN pin, to stabilize the bias supply (2.5-V rail or 3.3-V rail) from any parasitic impedance from the supply.

7. VLDOIN Input Capacitor

Depending on the trace impedance between the VLDOIN bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VLDOIN input capacitor. Use a 10µF (or greater) ceramic capacitor to supply this transient charge.

8. Output Filter Capacitor

For stable operation, the capacitance of the VO output pin is recommended to use a-10µF (or greater). Attach a 10-µF ceramic capacitors to minimize the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL).

9. PCB Layout Guide

For best performance of the SY20775B, the following guidelines must be strictly followed:

1. Please solder the exposed pad on the system ground pad on the top-layer of PCBs. The ground pad must have wide size to conduct heat into the ambient air through the system ground plane and PCB as a heat sink.

2. Please place the input capacitors for VIN pin as close as possible for decoupling high-frequency ripples.

3. Please place the input capacitors as close to VLDOIN pin as possible with short and wide connection to minimize the impedance of the layout.

4. Please place the output capacitor as close to VO pin as possible with short and wide connection to minimize the impedance of the layout. If output capacitors need to be placed on the load side for excellent load transient response, please leave a ceramic capacitor with a value of at least 10μF near the VO pin as close as possible.

5. Connect the VOSNS pin to the positive node of output capacitors as a separate trace. In DDR VTT application, connect the VO sense trace to DIMM side to ensure the VTT voltage at DIMM side is well regulated.

6. Connect the GND pin and PGND pin to the thermal pad directly.

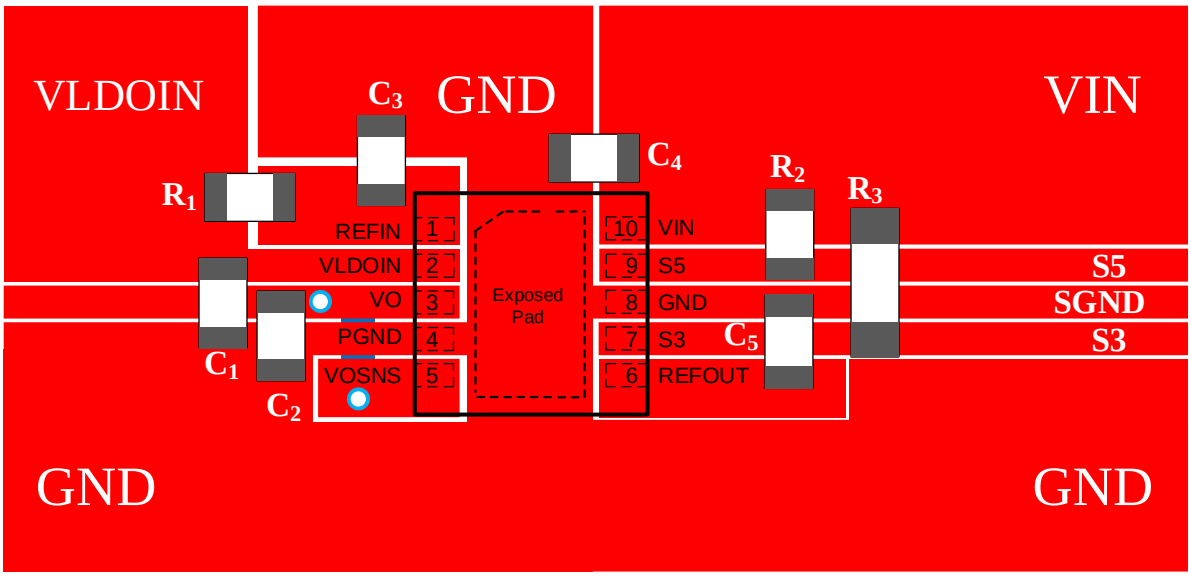
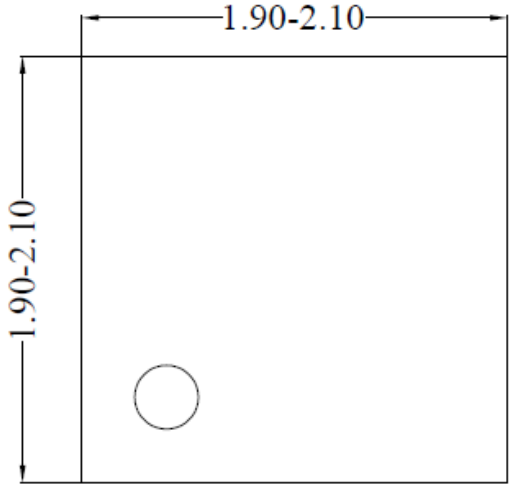
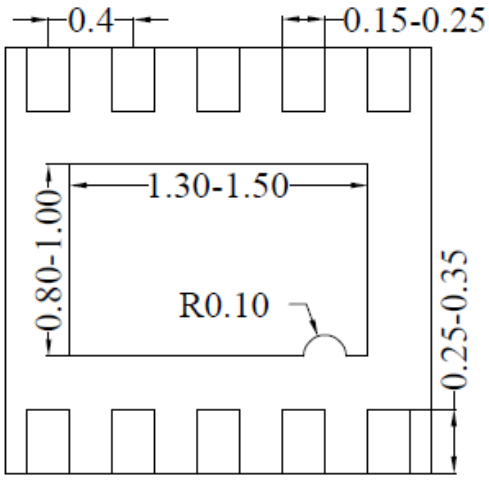


Figure 4. SY20775B PCB Layout Suggestion

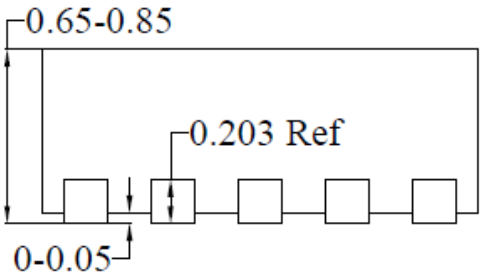
DFN2×2-10 Package Outline Drawing



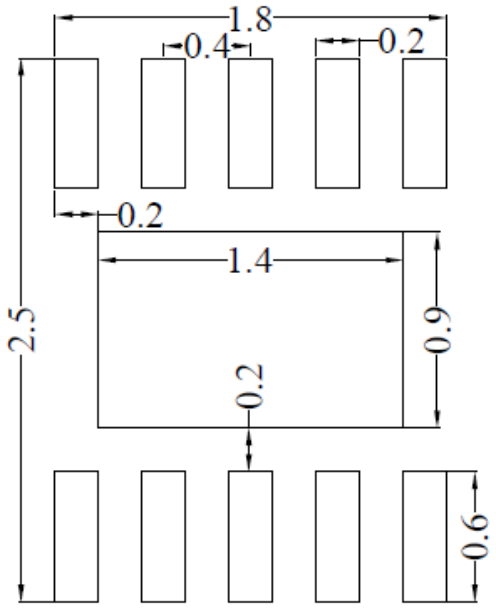
Top View



Bottom view



Front View



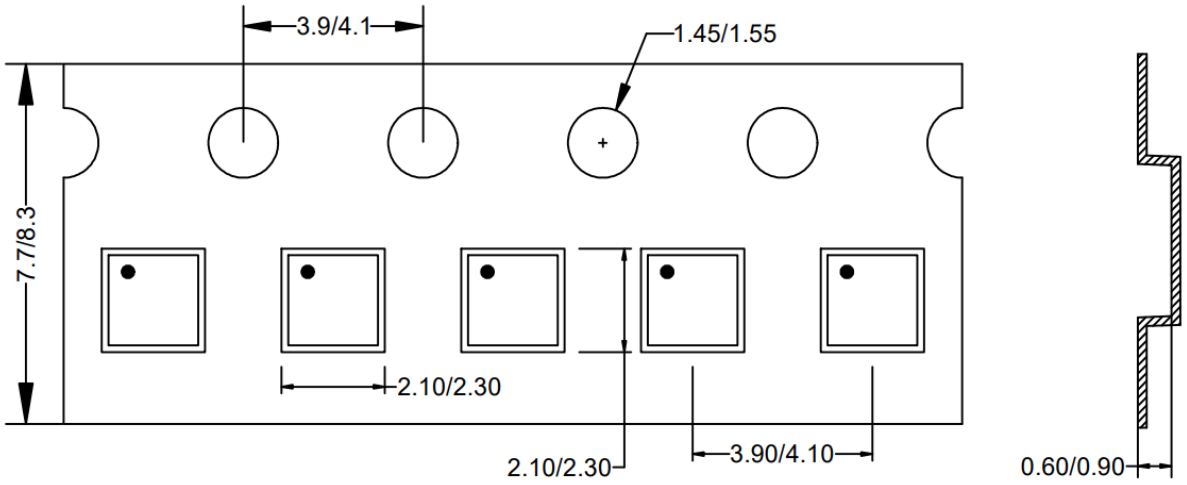
Recommended PCB layout
(only for reference)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

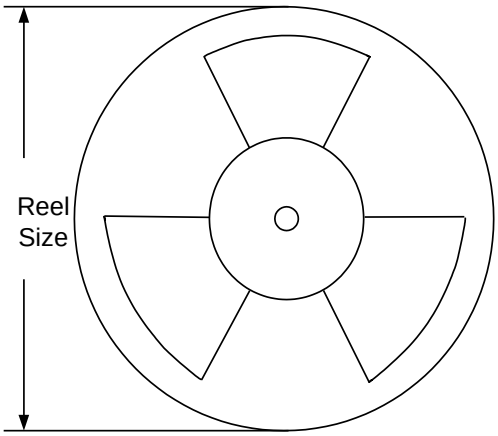
1. Taping orientation

DFN2×2



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
DFN2×2	8	4	7"	400	160	3000

Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
May 26, 2024	Revision 1.0	Initial Production Release
May 26, 2023	Revision 0.9	Initial Release

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